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Bias-Induced Instability of 4H-SiC CMOS

Yu-Xin Wen[1,a*], Bing-Yue Tsui[1,b]

[1]Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan, R.O.C.

[a]wennew.ee08@nycu.edu.tw, [b]bytsui@nycu.edu.tw

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Abstract. 4H-SiC complementary metal-oxide-semiconductor (CMOS) devices for control circuit applications have been reported extensively, however, the electrical stability, even with interface optimization processes, degrades significantly after bias stress. In this paper, we performed both positive and negative bias stress on planar SiC NMOSFETs and PMOSFETs fabricated with pure (non-diluted) and N_2-diluted NO post-oxidation annealing (POA) processes. The test results indicate the existence of positive hole traps might be the culprit that leads to electrical characteristics instability during operation and pure NO annealing is effective to reduce the instability.

Introduction

Silicon carbide (SiC), with the nature of wide bandgap, relative lower dielectric constant, and high thermal conductivity, has the potential to fabricate power devices operating at high power, high frequency and high temperature environment [1]. For high-frequency operation of the power system, the control circuit for the SiC power switch should be fabricated with SiC devices as well to reduce system volume size and parasitic power loss. Monolithic integration of both high-power device and control circuit is an effective way to reduce the volume of the power system and the power loss due to parasitic components between power device and control circuit. Several SiC CMOS circuits have been reported in literatures [2-6]. Recently, integration of both vertical power MOSFET and CMOS gate buffer on a single SiC chip has been reported [7, 8]. Though with normal switching operation controlled by low-voltage SiC CMOS devices, the reliability of the CMOS devices has not been disclosed.

Despite the promising material properties, SiC MOSFETs still suffer from low channel mobility and reliability concern due to high interface state density and carbon related defects which only exist in the SiO_2/SiC interface [9-11]. Previous studies reported the electrical stability of SiC-MOSFETs degrade greater and faster while recover back faster than observed in Si-MOSFETs [12, 13]. This phenomenon might due to defects with fast emission/slow capture time constant existed at the interface of the SiC trench MOSFETs. Recently, comprehensive reliability test on 4H-SiC N/PMOSFET under bias stress test had been conducted [14]. The results from negative bias on PMOSFET and positive bias on NMOSFET shows improved stability with thermal and ultrathin CVD oxide and diluted N_2O POA process. However, the large threshold voltage shift after bias stress suggests that the passivation of interface traps might be insufficient and the microscopic mechanism of the electrical characteristics drift still remains unknown. To clarify the mechanism behind and further improve the interface quality we performed bias stress on two gate oxides with different POA conditions.

Experimental Conditions

Fig. 1 (a) shows the schematic structure of the CMOS process. N- and P-channel MOSFETs were fabricated on n-type 4° off-axis (0001) 4H-SiC epi-wafers with epitaxial layer doping concentration and thickness of 1×10^{16} cm^{-3} and 5.5 μm respectively. Well and source/drain regions were then formed with Al and P ion implantations at 500 ℃, followed by a dopant activation annealing at 1700 °C for 30 min with carbon cap in Ar ambient. For device isolation, we employed LOCOSiC isolation structure through Ar ion implantation and a wet oxidation at 1100 °C for 5 hr [15, 16]. The gate oxide was grown by wet oxidation at 1200 ℃ for 30 min followed by two kinds of POA process:

pure (non-diluted) NO annealing or N_2-diluted NO annealing at 1200 ℃ for 15 min. The gate oxide thickness is about 20 nm from ellipsometer measurement. The main process flow is shown in Fig. 1 (b).

Conventional measure-stress-measure (MSM) test sequence is shown in Fig. 2. The test started with a pre-stress bias step before the first measurement to alleviate the effect from intrinsic defect. Then I-V sweep measurement and bias stress were the two steps that repeated.

Results and Discussion

After the test sequence, the threshold voltage shift (ΔV_{th}) and drain current degradation (ΔI_D) are extracted and shown in Fig. 3. The ΔV_{th} as well as ΔI_D are minor for devices with pure NO annealing process. Adequate amount of NO annealing was suggested to be effective in passivating carbon interstitials which act as hole traps [10, 17]. Still, under -10 V stress condition (NBS) both POA conditions exhibit significant negative ΔV_{th} and the ΔI_D increases for NMOSFET while decreases for PMOSFET. In contrary, there is no significant ΔV_{th} and ΔI_D under positive bias stress (PBS) condition. The negative ΔV_{th} indicates the existence of positive trap charges created during the stress period and the stress-induced trapping hardly emission after 500 s of stress. Under NBS, there are large number of holes accumulated at the SiO_2/SiC interface, part of them tunneled through the barrier of the interface and were trapped in SiO_2 and thus leading to negative ΔV_{th} and ΔI_D for PMOSFET. Based on the above phenomena, the electrical characteristics drift might be caused by hole traps in SiO_2, which were lower in the pure NO-annealed sample and started to saturate after NBS for 500 s. Since holes are harder to tunnel into SiO_2 than electrons but the results show minor drift under PBS, which indicates that a large number of hole traps existing in gate oxide. The estimated hole trap densities (D_{HT}) are 1.36×10^{11} and 4.22×10^{11} cm^{-2} for pure NO and diluted NO annealed samples, respectively, from the result of ΔV_{th}.

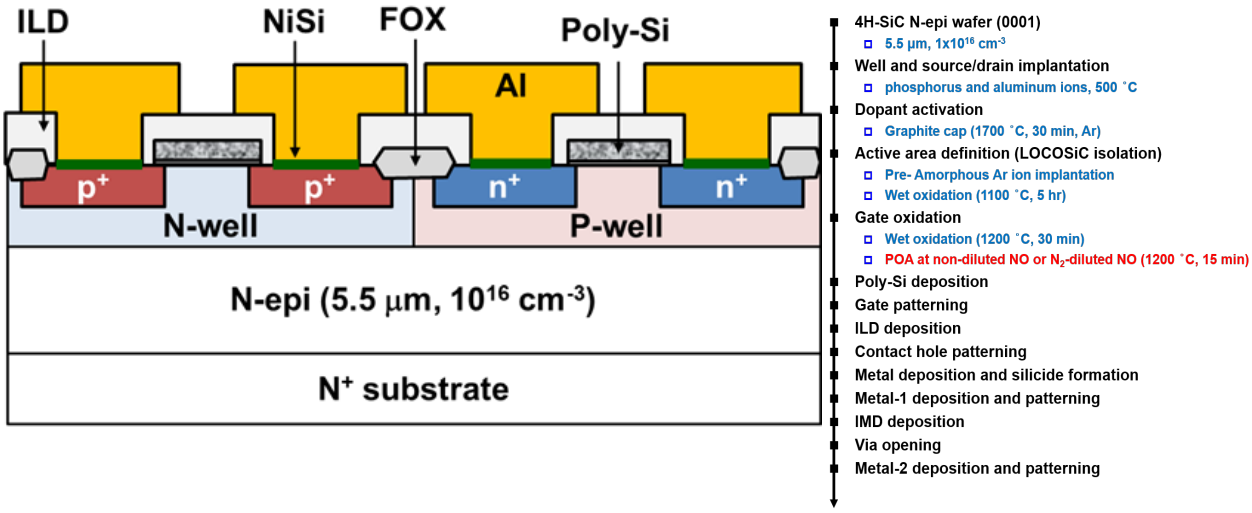

Fig. 1. (a) Schematic cross-sectional structure of the N/PMOSFET. (b) Main process flow and POA split conditions of the N/PMOSFETs in this work.

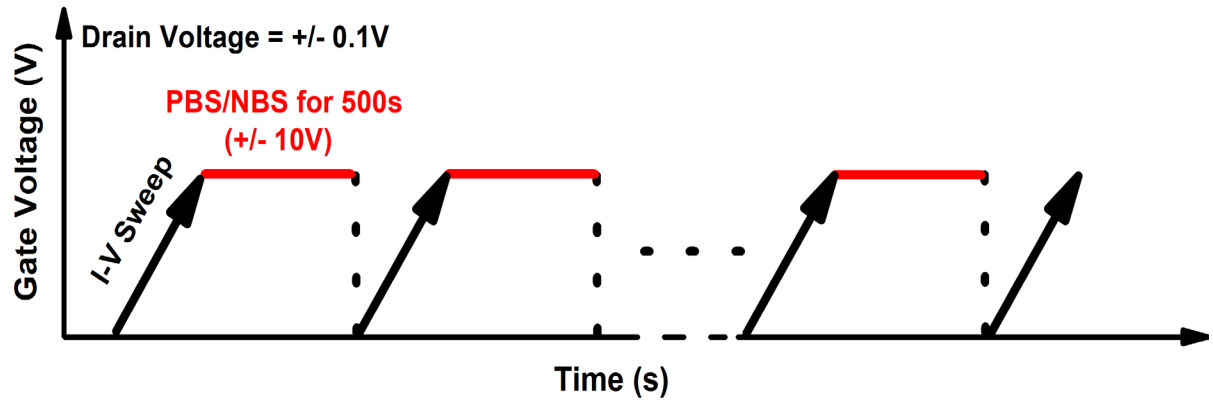

Fig. 2. Conventional measure-stress-measure (MSM) test sequence to study the bias instability. I-V sweep from 0 to +/-10 V for N/PMOSFETs for measurement. Positive or negative bias stress of +/-10 V for 500 s per cycle on the gate for stressing.

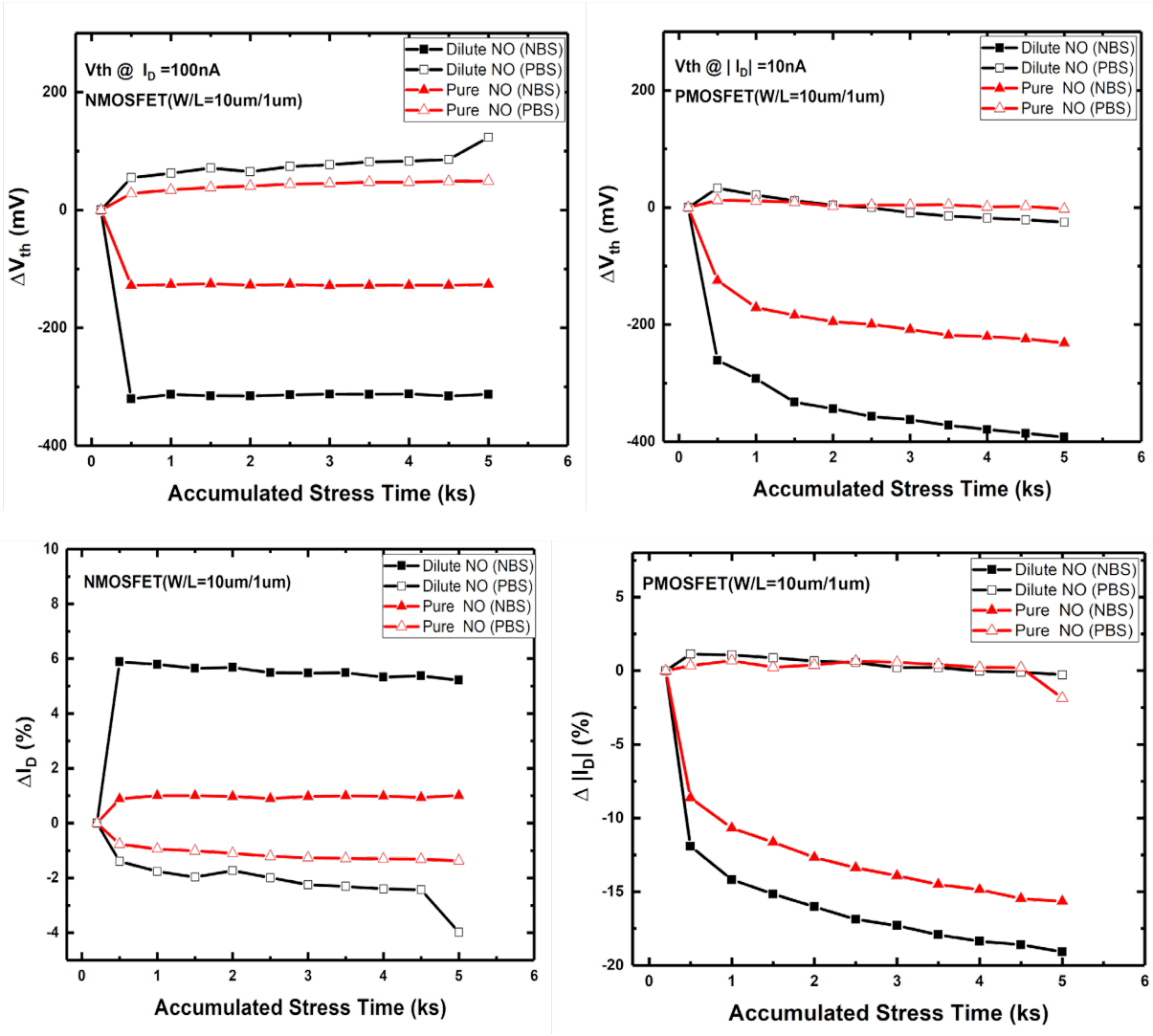

Fig. 3. Threshold voltage shift (ΔV_{th}) and drain current degradation (ΔI_D) of 1-μm-long SiC N/PMOSFETs under positive bias stress (open symbol) or negative bias stress (filled symbol) with N_2-diluted NO annealing sample (black squares), pure-NO annealing sample (red triangles).

Summary

According to the above results, hole trap might be the most possible defect that leads to electrical characteristics instability during operation. Furthermore, pure NO annealing is effective to reduce the instability. Clearly, there is still room for further optimization that passivate more amount of the defect, but thermal budget of the NO annealing process is crucial to balance the defect passivation and creation.

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