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On the Frequency Dependence of the Gate Switching Instability in Silicon Carbide MOSFETs

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Abstract. Silicon carbide power metal-oxide semiconductor field-effect transistors (MOSFETs) are suitable for more compact and energy efficient electric power conversion, pushing forward numerous key technologies in emission-free mobility and green power generation. These applications require fast gate switching up to hundreds of kilohertz. Typically, to assure a clear turn-off state of the electron channel, a negative turn-off gate bias is used in conjunction with a positive turn-on gate bias. Recently, several reports have revealed a new and so far unknown degradation mechanism that emerges during such operation conditions in apparently all commercial silicon carbide MOSFETs. As this mechanism arises upon gate switching, the terms gate switching instability (GSI) and gate switching stress (GSS) for the mechanism and the associated stress, respectively, have been introduced.
Here, we show that this degradation mechanism does not depend on the used frequency up to at least 2 MHz, but that it is actually related to the cumulative number of switching cycles. For this purpose, we performed measurements at various frequencies comprising ultra-fast in-situ measurements of the threshold voltage and pre- and post-stress characterization by impedance analysis. The results are important both for understanding the underlying physics and for developing a correct methodology for industrial device qualification.

Introduction

In the context of an increasing demand for renewable energy resources and emission-free mobility, high power electronics are receiving greater attention from both industry and academia. Indeed, research and development do not only focus on the creation of efficient solar cells or batteries with high energy density, but also consider the conversion of the gained electric power into its needed form. Silicon carbide (SiC) power metal-oxide semiconductor field-effect transistors (MOSFETs) are suitable for AC-DC and DC-DC conversion. In these applications, the SiC MOSFETs are exposed to an AC gate signal with a frequency of up to hundreds of kilohertz. For turn-on, the gate of an n-channel MOSFET is biased positively, whereas for the off-state zero gate bias is typically used. However, particularly circuit designs with SiC MOSFETs having a small threshold voltage V_{th} often choose a negative voltage for turn-off [1].
Recently, semiconductor manufacturers and research groups have revealed a new degradation mode that is exclusively triggered under such bipolar AC switching conditions [2, 3]. This degradation leads to an increase of V_{th} that can exceed the results from static DC tests. In response to this, a novel stress test for SiC MOSFETs within industrial device qualification was initiated [4] and the terms gate switching instability (GSI) and gate switching stress (GSS) for the mechanism and the associated stress, respectively, were introduced [4].

Different properties of this new degradation mechanism have been discussed in the scientific community and explanations of the underlying physics have been proposed. Jiang *et al.* hypothesized that fast trapping/detrapping of charges (hysteresis) enhances charge trapping into defects with higher capture activation energies via a spatially and temporally local increase in the electric field [5]. The authors speculated that positive charges trapped during the application of a negative bias temporarily decrease the capture activation energy for negative charges, once the MOSFET is turned on. Besides this study, Xu *et al.* found a negligible duty cycle dependence [6] and Tang *et al.* studied the impact of switching stress on the forward voltage of the body diode [7]. Furthermore, Zhong *et al.* discussed the voltage level dependence, undershoots and overshoots, and confirmed the independence of the duty cycle [8, 9]. Ghosh *et al.* have also contributed investigations [10, 11].
Here, we investigated the components of the total V_{th} drift and their frequency dependence by both threshold voltage measurements and impedance characterization before and after stress.

Experimental Details

Our experiments were performed on trench power MOSFET devices in TO-247 packages. These relatively small devices particularly designed for high frequency switching featured a gate capacitance of $0.31\,\mathrm{nF}$ and a gate charging time constant of $1.2\,\mathrm{ns}$, whereby they were selected based on similar on-state resistance ($(314 \pm 20)\,\mathrm{m\Omega}$ at $V_{\mathrm{GS}} = 17\,\mathrm{V}$) and initial V_{th} ($(3.11 \pm 0.03)\,\mathrm{V}$ at $I_{\mathrm{DS}} = 2\,\mathrm{mA}$), which assured comparability of the measurements between the different devices.
Initially, the devices were characterized before stress by measurements of the impedance between the gate terminal and the shorted drain and source terminals with a Keysight E4990A impedance analyzer. After open and short circuit calibration of the measurement system, the gate voltage was swept upwards from $-30\,\mathrm{V}$ to $30\,\mathrm{V}$ and back down. The used sweep rate was $1.92\,\mathrm{V\,s^{-1}}$ with a pause at the bias of $30\,\mathrm{V}$ between up and down sweep of $11.7\,\mathrm{ms}$.
The devices were then mounted in small ovens and a custom setup [12] was used for both stress signal generation and V_{th} measurements at $175\,^{\circ}\mathrm{C}$. Direct mounting of the tested devices on the stress board assured short wiring and hence low parasitic inductance. Our custom setup further ensured low output resistance and excellent control over the applied gate signal, which was a $20\,\mathrm{V}/{-10}\,\mathrm{V}$ square waveform (duty cycle of $50\,\%$, see Fig. 1a) with rise and fall times of $50\,\mathrm{ns}$, respectively. The eight

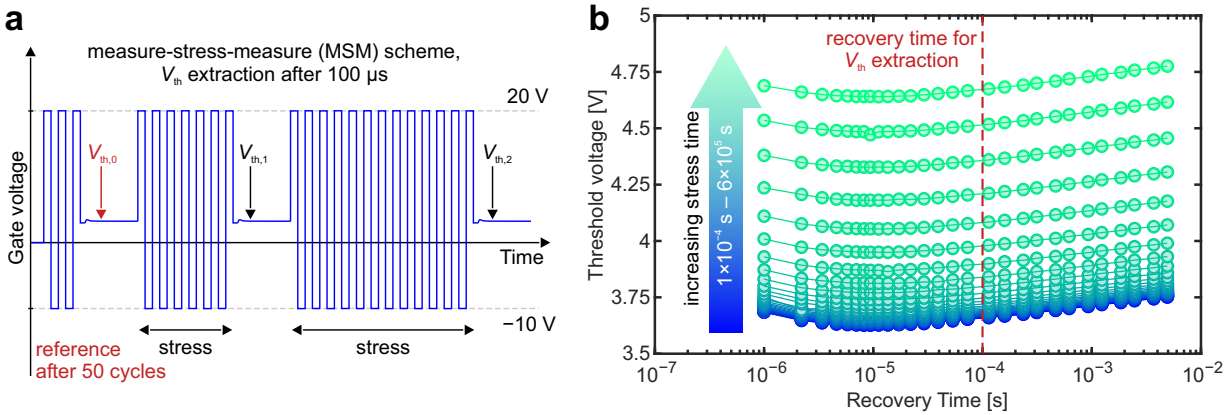

Fig. 1: **a)** The measure-stress-measure (MSM) scheme of the performed experiments. The reference measurement $V_{\mathrm{th},0}$ is performed after 50 stress cycles. This accounts for the fast recoverable component of the V_{th} shift that can follow the switching gate signal. Reproducible timing and control of the stress waveform are crucial for precise measurements. **b)** The V_{th} recovery curves measured during the measurement periods of an experiment with a stress frequency of $500\,\mathrm{kHz}$. The curves are parallel indicating no impact of the degradation on short-term charge trapping within the considered recovery time. V_{th} is extracted at a standard recovery time of $100\,\mu\mathrm{s}$.

devices were exposed to the same total number of 3×10^{11} stress cycles by using different frequencies between 71 kHz and 2 MHz, while keeping all other stress parameters constant. In consequence, the total stress time varied between 1.5×10^5 s and 4.2×10^6 s.
The employed experimental technique, a measure-stress-measure (MSM) scheme, assured a reproducible impact of short-term charge trapping and detrapping (hysteresis) during measurement. Hysteresis can effectively shift the V_{th} dynamically during the application of AC gate stress [12, 13]. To capture only long-term degradation, the reference measurement $V_{\mathrm{th},0}$ was performed after 50 cycles of the gate stress signal, which is always reproducibly interrupted for measurement after the positive gate voltage pulse. All V_{th} measurements, including the reference measurement $V_{\mathrm{th},0}$, consisted of recovery phases of 5 ms during which an operational amplifier based feedback loop tracked the gate voltage by forcing a drain-source current of 1 mA at $V_{\mathrm{DS}} = 1$ V (see Fig. 1b). During these recovery phases, the threshold voltage was measured on a logarithmic time scale. The V_{th} was then extracted after a recovery time of 100 µs.
After the stress tests, the same impedance characterization as before the stress was repeated within an hour after the end of stress to deduce the impact of the performed stress. Both the pre-stress and post-stress impedance characterizations were conducted at room temperature.

Results

First, we considered the impact of a varying stress frequency f on V_{th}. The threshold voltage drift $\Delta V_{\mathrm{th}} = V_{\mathrm{th}} - V_{\mathrm{th},0}$ of each measurement period after a fixed recovery time of 100 µs is shown for the various frequencies in Fig. 2a. Bias temperature instability (BTI) is known to roughly relate to the stress time t_{s} via a power law

$$\Delta V_{\mathrm{th}}(t_{\mathrm{s}}) = A \cdot t_{\mathrm{s}}^{n} \tag{1}$$

with a constant A and a power law exponent n. In a double logarithmic plot a power law appears as a straight line with slope n. However, as shown for GSI in Fig. 2a, ΔV_{th} does notably not follow a single straight line [2]. In the range of 10^2 s–10^4 s of stress time, the slope of all drift curves increases. Furthermore, for a fixed stress time, ΔV_{th} increases with increasing frequency. Assuming a mechanism where the total drift depends only on the cumulative stress time at positive and negative bias, such a result would be unexpected. Consequently, the cumulative stress time itself no longer appears to be the determining parameter for the degradation. If the threshold voltage shift followed a power law

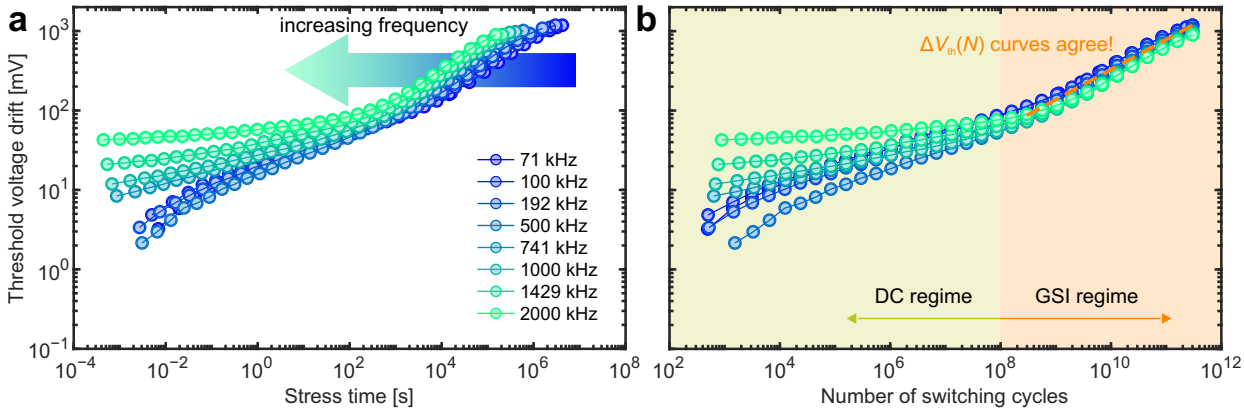

Fig. 2: **a)** ΔV_{th} extracted at a fixed recovery time of 100 µs for various frequencies. The drift curves shift towards lower stress times with increasing frequency. **b)** The same data as in a), however plotted against the number of passed switching cycles. The DC and GSI regimes below and above 10^8 switching cycles, respectively, are indicated by the background color. Within the GSI regime, the drift curves roughly match without the necessity of separating the DC component.

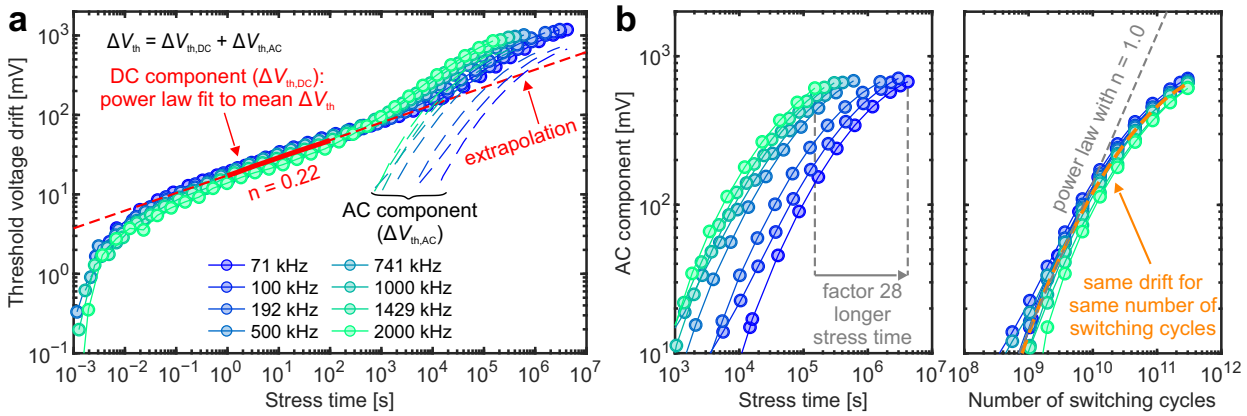

Fig. 3: **a)** The threshold voltage drift ΔV_{th} relative to an initial V_{th} versus the stress time **b)**. The AC component versus the stress time and the number of switching cycles, respectively. It depends on the number of switching cycles.

dependence on the stress time (as in equation 1), plotting it in a double logarithmic plot against the number of switching cycles $N = t_{\text{s}} \cdot f$ would still result in a straight line as

$$\Delta V_{\text{th}}(N) = \underbrace{\frac{A}{f^n}}_{A'} \cdot N^n \tag{2}$$

is again a power law with the same exponent n, but with a different constant A' that depends now on the frequency. A change in frequency would therefore lead to a parallel shift of the drift curve in a double logarithmic plot. Such a plot of the drift ΔV_{th} versus the number of switching cycles is presented in Fig. 2b. For a high number of switching cycles, where an increased slope n is observed in Fig. 2a, the drift curves start to match. It is reasonable that we observe two different effects that superimpose to the measured ΔV_{th} at any point in time. The first effect is the drift of ΔV_{th} originating from conventional charge trapping that would also be present under DC bias conditions (DC regime), whereas the second effect above 10^8 cycles is a dominant contribution to the total ΔV_{th} driven by the cumulative number of switching cycles (GSI regime).

For the precise evaluation of this new drift component and its dependence on the used frequency, it is however important to relate the drift to an identical initial stress time rather than to an identical number of stress pulses. This provides a new reference value $V'_{\text{th},0}$. For $V'_{\text{th},0}$, we use a stress time of 1 ms. The resulting drift plot of $\Delta V'_{\text{th}} = V_{\text{th}} - V'_{\text{th},0}$ is shown in Fig. 3a. It confirms the presence of the DC and AC components. During the DC regime, all drift curves plotted versus the cumulative stress time match because the cumulative stress time is the driving parameter for the DC component. Once the GSI regime is entered at around 10^3 s, the drift starts to depend on the frequency. We can separate the AC component by subtracting the DC component as illustrated in Fig. 3a. By assuming a power law dependence on stress time of the DC component, we extrapolated it into the GSI regime. By subtracting the DC component from the total V_{th} drift, we obtained the AC component that is indicated by dashed lines in Fig. 3a and presented in detail in Fig. 3b. The AC component is clearly the dominating contributor to the total drift, covering almost two orders of magnitude in stress time via the various frequencies. Once plotted against the number of switching cycles, the drift curves match better than the data shown in Fig. 2b because the stress-time driven DC component was removed. Between 10^9 and 10^{10} cycles the AC component can be fitted with a power law with an exponent $n = 1.0$, which is larger than typical values from conventional BTI (see DC component with $n = 0.22$ in Fig. 3a). Consequently, the AC component appears to be roughly proportional to the number of switching cycles.

Next, we looked into the impact of GSS on the impedance of the MOS structure. Such measurements before and after GSS provide more detailed information aside from the bare threshold voltage which

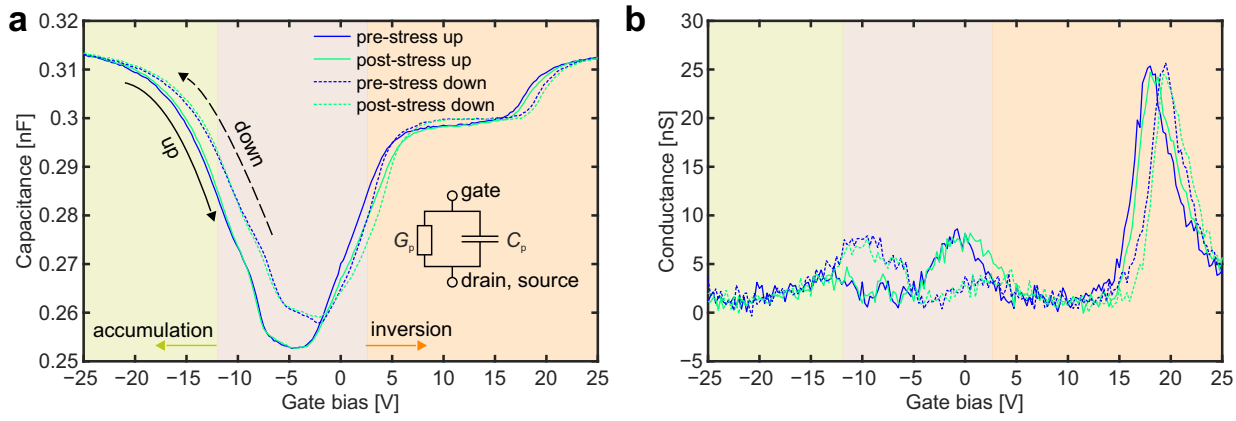

Fig. 4: **a)** The capacitance C_p and **b)** the conductance G_p from the equivalent circuit (see inset in **a**) that was used to interpret the measured impedance, exemplarily shown for a stress frequency of $500\,\mathrm{kHz}$.

by itself does not necessarily reflect the impact of traps on the device characteristics at other Fermi levels [14]. Full sweeps of the gate bias cover accumulation, depletion, and inversion of the MOS structure. The measured complex impedance is interpreted in terms of an equivalent circuit as indicated in the inset of Fig. 4a, consisting of a capacitance C_p and a conductance G_p that are connected in parallel. Exemplarily, for a stress frequency of $500\,\mathrm{kHz}$, Fig. 4 shows the up and down sweeps before (pre) and after (post) 3×10^{11} switching cycles of stress. In accumulation and depletion, we observed similar behavior for both up and down sweeps. The strongest impact of the stress for both the capacitance and the conductance can be observed in the range of $0\,\mathrm{V}$–$5\,\mathrm{V}$.
The goal of the following considerations is not to determine the contributions of defects to the total capacitance or conductance. A typically observed hysteresis in the current-voltage characteristics of up and down sweeps is similarly present in the capacitance characteristics (see Fig. 4). Associated stretch-out of the capacitance-voltage curves adversely affects the interpretation of the small-signal capacitance [14]. Therefore, our premier goal is to illustrate that although the stress times for different frequencies varied strongly over almost two orders of magnitude, the impact on the impedance characteristic is similar or even identical. For this purpose, we considered the change in the capacitance ΔC_p and conductance ΔG_p at a certain gate bias V_GS.

$$\Delta C_\mathrm{p}\left(V_\mathrm{GS}\right) = C_\mathrm{p}^\mathrm{stressed}\left(V_\mathrm{GS}\right) - C_\mathrm{p}^\mathrm{pristine}\left(V_\mathrm{GS}\right) \tag{3}$$

$$\Delta G_\mathrm{p}\left(V_\mathrm{GS}\right) = G_\mathrm{p}^\mathrm{stressed}\left(V_\mathrm{GS}\right) - G_\mathrm{p}^\mathrm{pristine}\left(V_\mathrm{GS}\right) \tag{4}$$

Both quantities are plotted as a function of V_GS in Fig. 5 separately for up and down sweeps. Apart from qualitative agreement between the curves, there is also an excellent quantitative agreement with only slight differences. Particularly around the threshold voltage, the curves match very well. Consequently, even though different stress frequencies were used with strongly varying stress times, the caused permanent device degradation appears identical.
Apart from the more permanent degradation, transient charge trapping and detrapping, commonly known as hysteresis, is an important characteristic of a SiC MOSFET. We characterized the hysteresis by extracting the interface trap capacitance C_it of defects with time constants between $10\,\mu\mathrm{s}$ and $1\,\mathrm{ms}$, corresponding to impedance measurement frequencies of $100\,\mathrm{kHz}$ and $1\,\mathrm{kHz}$, respectively. The extraction of C_it was performed according to $C_\mathrm{it} = qAD_\mathrm{it} = \left(C_\mathrm{1kHz}^{-1} - C_\mathrm{ox}^{-1}\right)^{-1} - \left(C_\mathrm{100kHz}^{-1} - C_\mathrm{ox}^{-1}\right)^{-1}$, where q is the electron charge, A is the gate area, D_it is the defect density, and C_ox is the oxide capacitance [15]. Fig. 6a shows the resulting C_it before and after stress for a stress frequency of $500\,\mathrm{kHz}$. There is hardly any difference except a slight stretch-out that was also observed in Fig. 4a. The change in C_it due to stress of different frequencies is shown in Fig. 6b. Apparently, there is no dependence on

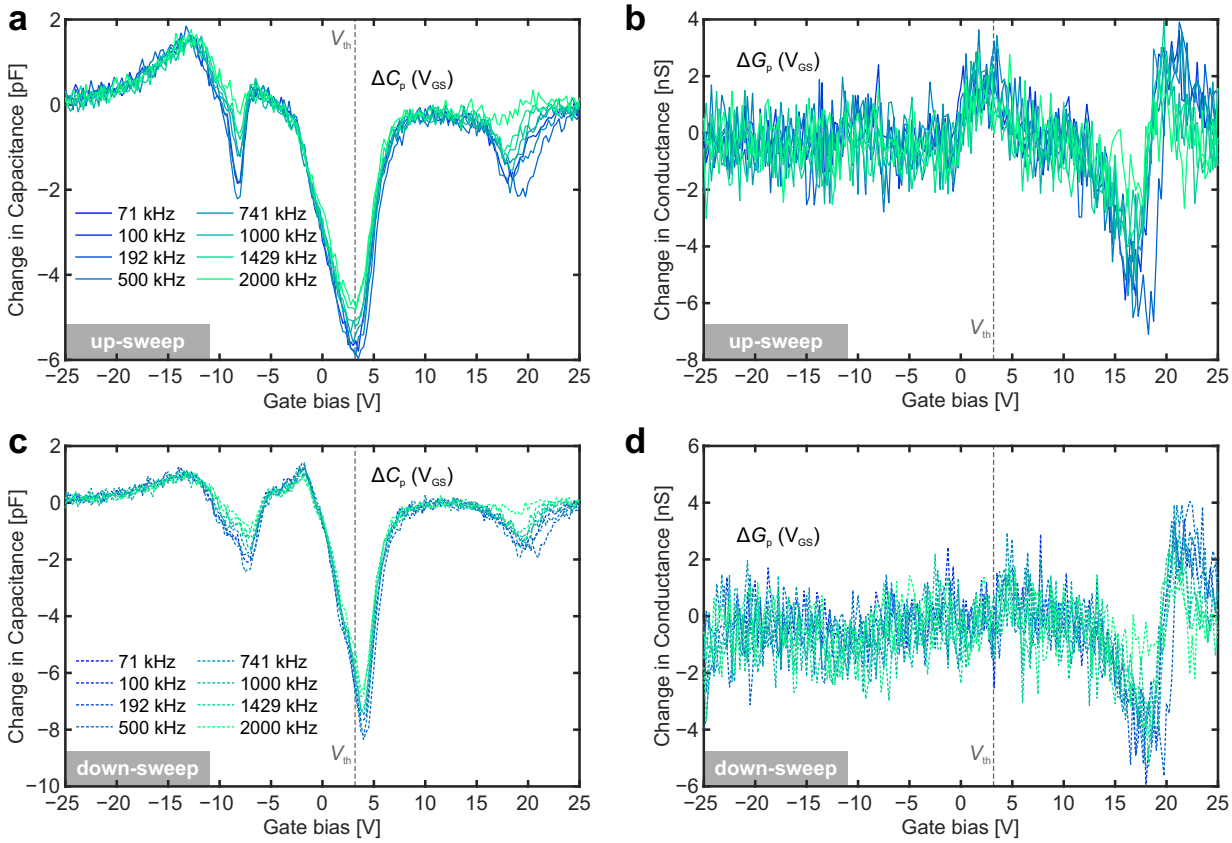

Fig. 5: The stress-induced change of **a)** the capacitance ΔC_p and **b)** of the conductance ΔG_p, both measured during an *up sweep*. The stress-induced change of **c)** the capacitance ΔC_p and **d)** of the conductance ΔG_p, both measured during a *down sweep*. The legend entries refer to the *stress* frequency.

the stress frequency. The results suggest that no interface defects with time constants between $10\,\mu\mathrm{s}$ and $1\,\mathrm{ms}$ are created or annealed by stress exposure. This behavior is also not influenced by the stress frequency.

Discussion

For the tested device, the impact of GSS on the threshold voltage is apparently dominated by the cumulative number of switching cycles to which the device is exposed. Once GSI dominates the threshold voltage drift, a similar V_th drift is obtained for the same number of switching cycles. This suggests that any change to any type of defect at or near the $\mathrm{SiC/SiO_2}$ interface is identical for all tested frequencies. This is fundamentally different to what is known about charge trapping under static bias conditions, where the stress time is the important parameter. Furthermore, we observed an approximate power law dependence of the AC component with an exponent $n = 1$, which means that the associated V_th drift is roughly proportional to the number of switching cycles. From the fit in Fig. 3b, we can subsequently extract the proportionality factor of $1.4 \times 10^{-8}\,\mathrm{mV}$ which is the average ΔV_th contribution from a single switching cycle. Under the assumption that the underlying mechanism is based on trapped charges located at the $\mathrm{SiC/SiO_2}$ interface, this would, on average, correspond to roughly 0.03 trapped electrons per switching cycle, which is a small number compared to 3×10^{10} inversion electrons.
Apparently, the presented independence on frequency appears contradictory to a mechanism based on locally increased electric field as suggested by Jiang *et al.* [5]. More charges would be trapped with increasing pulse width [12, 13], which would subsequently locally increase the electric field, thus enhancing the threshold voltage drift for the same number of switching cycles with decreasing frequency.

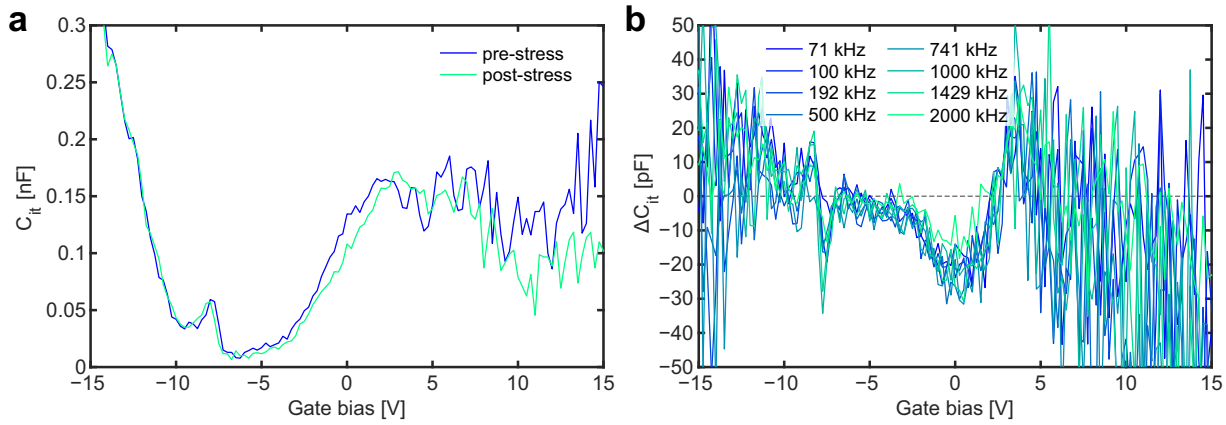

Fig. 6: **a)** The capacitance of the interface defects with time constants between 10 µs and 1 ms before and after 500 kHz stress. **b)** The change in capacitance of the interface defects for the various stress frequencies.

However, the fact that the threshold voltage increases with the number of switching cycles suggests that the switching events themselves are indeed responsible for the degradation. A bipolar switching event comprises several contemporary charge trapping/detrapping and defect-assisted recombination events. Apart from electrical detection of charge carrier recombination at the SiC/SiO_2 interface during bipolar switching [16], optical detection also confirms the presence of defect assisted recombination, whereby hundreds of photons can be detected during a single gate voltage transient [17]. With regard to hundreds of radiative recombination events per switching cycle, only 0.03 trapped electrons per switching cycle appears as a rather low number. A plausible explanation for GSI might therefore be a recombination enhanced defect reaction, that provides a ”phonon kick” to charge a defect with a high capture activation energy that would otherwise not be easily accessible under a DC gate bias [18, 19, 20, 21]. Similar observations on silicon devices have however been assigned to gate-sided hydrogen-release [22].

Summary

In summary, the threshold voltage drift caused by the gate switching instability is composed of two components: the conventional effective DC component driven by the stress time and the AC component driven by the number of switching cycles. As the latter dominates the threshold voltage drift for a high number of switching cycles, the total drift roughly shares this dependence and is hence almost exclusively governed by the number of switching cycles. We observed an approximate power law dependence of the AC component with a unity exponent, meaning the drift exhibits a direct proportionality to the cumulative number of switching cycles. Trapping at the SiC/SiO_2 interface would feature, on average, 0.03 trapped electrons per switching cycle. Furthermore, impedance analysis showed neither a significant impact of the frequency on the device after an identical number of stress cycles nor a creation or annealing of interface defects with time constants between 10 µs and 1 ms. Hence, our results support the validity of frequency acceleration at least up to 2 MHz in gate-switching stress testing of SiC MOSFETs.

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