Materials Science Forum
ISSN: 1662-9752, Vol. 1092, pp 119-125
doi:10.4028/p-hpfivz

Submitted: 2022-09-01
Revised: 2022-11-02
Accepted: 2022-11-25
Online: 2023-06-06

Robustness of SiC MOSFETs under Repetitive High Current Pulses

Bettina Findenig[1,a*], Markus Sievers[1,b], Ingo Voss[2,c], Thomas Aichinger[3,d]

[1]KAI GmbH, Europastr. 8, 9524 Villach, Austria

[2]Infineon Technologies AG, Am Campeon 1-15, 85579 Neubiberg, Germany

[3]Infineon Technologies Austria AG, Siemensstr. 2, 9500 Villach, Austria

[a]bettina.findenig@k-ai.at, [b]markus.sievers@k-ai.at, [c]ingo.voss@infineon.com, [d]thomas.aichinger@infineon.com

Keywords: SiC MOSFET, Robustness Validation, High Current Stress, Degradation Monitoring, Device Characterization, Clamped Inductive Switching

Abstract. In this paper the robustness of state of the art SiC MOSFETs is analyzed under repetitive high current pulses far beyond the nominal values specified in their data sheets. SiC MOSFETs are more and more used in many power electronics-based applications, such as industrial motor control units. During start-up events or load changes of such motors sudden high current pulses may occur. This imposed stress might trigger the drift of electrical parameters that can limit the operating range and lifetime of commercially available SiC MOSFETs. Nevertheless, the tested devices withstood millions of repetitive high current pulses several times higher than the rated nominal current without any signs of degradation.

Introduction

The market adoption of Silicon Carbide (SiC) Metal-Oxide Semiconductor Field Effect Transistors (MOSFETs) has accelerated significantly in recent years. Not only motivated by the increasing demand for products with highly efficient power electronics the technology has reached a level where it is mass market ready, especially with respect to reliability. Although there are new degradation phenomena such as the dynamic gate instability [1, 2] the robustness of SiC MOSFETs continues to increase. For example, [3] has studied the behavior of SiC MOSFETs under repeated Short Circuit (SC) to investigate their robustness when such SC pulses are used to limit the over-voltage stress caused by inrush currents into a DC link capacitor. While there are studies that have investigated the critical SC energy [4] SiC MOSFETs can withstand, SC robustness continues to be a widely discussed topic [5, 6]. Besides SC robustness, there is a lack of information regarding the behavior of SiC devices under high pulsed drain currents that might occur in motor applications during the start-up or during load changes. Also, irregular operating conditions of other applications might introduce short high-current pulses. In case of a Si Insulated Gate Bipolar Transistor (IGBT) with its high amount of electron/hole plasma it might happen that during repetitive switching events with very high currents specific degradation effects at the Si/SiO_2 interfaces can occur resulting in a changed switching behavior (switching gradients and delay times). However, by a proper IGBT design in the area of the trench cells it is possible to achieve a very stable long-term behavior [7]. In case of a unipolar SiC MOSFET the expectation is that nothing conspicuous will be discovered, when turning off the device at very high current levels, since no bipolar plasma exists. To confirm this expectation and to ensure that there are no other yet unknown degradation mechanisms under these operating conditions the results of a series of experiments are presented. During the experiments the Devices Under Test (DUTs) have been subjected to repetitive high current pulses. Therein also lies the novelty of this contribution, since no publication on such repetitive switching with high current densities have been reported so far to our knowledge.

For the here presented research it is assumed that there might be an application that experiences approximately 10 million over current pulses over a 10-year lifetime. To guarantee that a device can withstand such repetitive high current pulses throughout its lifetime, normally a part with a sufficiently

high current rating would be selected. This part would have a current rating multiple times higher than what would be needed under normal operating conditions. To detect potential degradation, intermediate device characterizations have been done. In particular, the threshold voltage (V_{TH}) and on-state resistance (R_{ON}), as well as the dynamic behavior of the DUTs were recorded. In this study we show that such a drastic derating may be not required for SiC MOSFETs.

Experimental Setup

The herein presented work utilizes the system presented in [8] and depicted in Fig. 1 to apply a large number of single high current pulses to discrete 1200 V SiC MOSFETs in a discrete TO247 package. The setup consists of a full bridge were one half bridge acts as protection switches. The second half

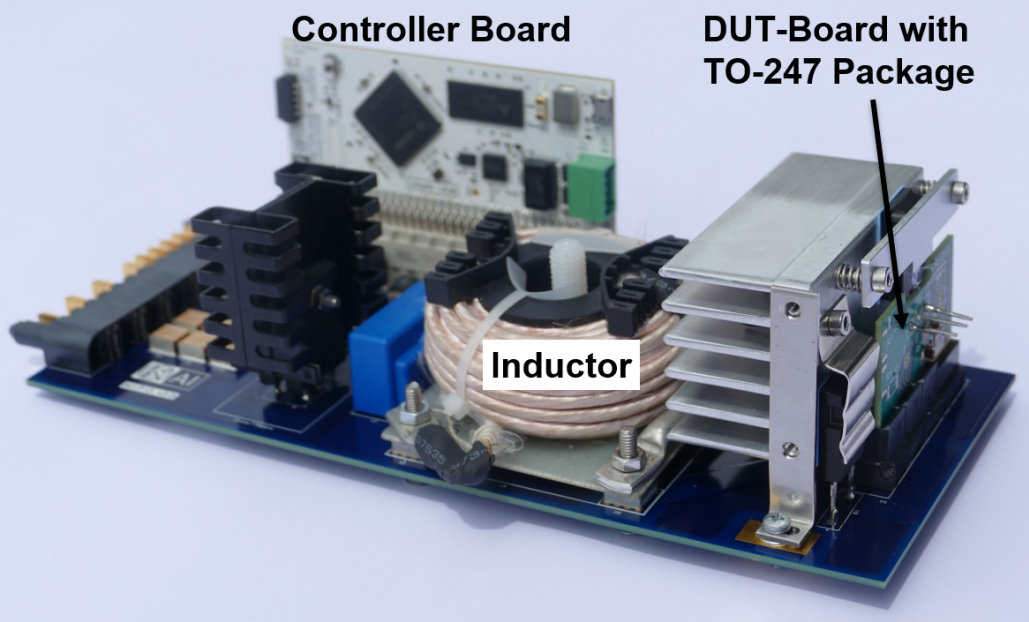


Fig. 1: Test setup used for repetitive pulses.

bridge consists of the DUT and the clamping diode. The test bench offers the flexibility to easily exchange the inductor and the discrete DUT. The gate levels can be changed because a commercially available gate driver has been extended by an adjustable gate voltage circuit. The reference voltages are generated by two Digital-to-Analog Converters (DACs) that are programmed via the Serial Peripheral Interface (SPI) of the controller board. Both positive range of the gate drive supply voltage and the negative range can be adjusted. The maximum test conditions are listed in Table 1. In addition, the

Table 1: Maximum stress test conditions during repetitive pulse testing.

Test Parameters	Symbol	Value
DC Link Voltage	V_{DC}	800 V
Drain Current	I_d	150 A (6x I_{nom})
Gate Voltage High Level	V_{GH}	20 V
Gate Voltage Low Level	V_{GL}	−15 V
Inductor	L	24 µH
Pulse Rate	f_{repeat}	200 Hz

controller board provides the necessary control signal to apply the pulses to the DUT. These high current pulses are, however, not equivalent to SC pulses with respect to their amplitude and pulse

shape. The applied pulses are similar to the work presented in [9] with the difference that the applied DC link voltage was selected to be within the rated drain-to-source voltage of the DUTs. An example of the current pulse shape applied to the DUT during the test is shown in Fig. 2. The tested SiC MOSFET

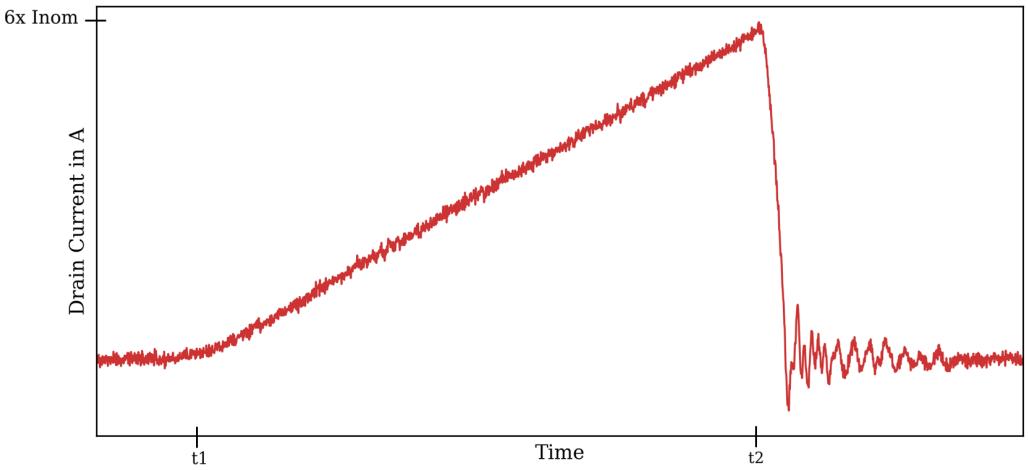


Fig. 2: Shape of the high current pulse used as stressor.

is a 4-pin device, in which the current pulse reaches 150 A within 4.5 µs when the DC link voltage is set to 800 V. The inductance was measured with a precision impedance analyzer and determined to be 24 µH. As mentioned before, the modularity of the setup allows the inductor to be easily exchanged. For the experiments presented in this study we used pulses up to 6 times the nominal current as stressor. The current pulses were applied at a rate of 200 Hz. Thereby, the power loss of the DUT was kept at a minimum such that the device temperature remained nearly at room temperature throughout the test.

Under the assumption of an application that experiences 10 million of such pulses throughout its lifetime our test setup covers these high current pulses within approximately 14 h of test time. In our setup the current amplitude can be adjusted by either varying the time between t_1, where the DUT is turned on, and t_2, where the DUT is turned off again, or by changing the value of the inductor. In contrast to Double Pulse Test (DPT), only a single high current pulse is applied to the DUT. After the peak current has been reached at t_2, the DUT is turned off and the current through the inductor is returned to zero before the next pulse is started. This turn-off transition happens under hard-switching conditions. In order that both the DUT and the protection switches do not suffer from very high over-voltages due to their commutation loop parasitic inductance, a 10 Ω gate resistor was used. Thereby the switching speed is reduced, which limits the di/dt of the DUT and the resulted over-voltage caused by parasitic inductances in the commutation loop.

In order to reduce the commutation loop, usually the DC link capacitors are placed next to the DUT. In this setup the DC link capacitors are placed on the main board instead of on the DUT board itself. While this slightly increases the commutation loop it also minimizes the components on the DUT board. The biggest advantage of this configuration is that the DUT can be characterized intermediately with dedicated high precision equipment without suffering from the influence of the DC link capacitors, similar to the approach described in [1]. An edge connector with the gate drive and high voltage signals enables the easy removal of the DUT board from the test bench to perform the intermitted characterization measurements. After removing the DUT board form the test bench, the DUT board is connected to a Source Meter Unit (SMU), which performs the measurements to obtain the static device parameters. A LabVIEW program controls the SMU and is creating an up and a down sweep of the V_{GS}. Afterwards the program extracts the V_{TH} at 1 mA. The R_{ON} is subsequently obtained at different V_{GS} levels. All device characterizations have been done at room temperature.

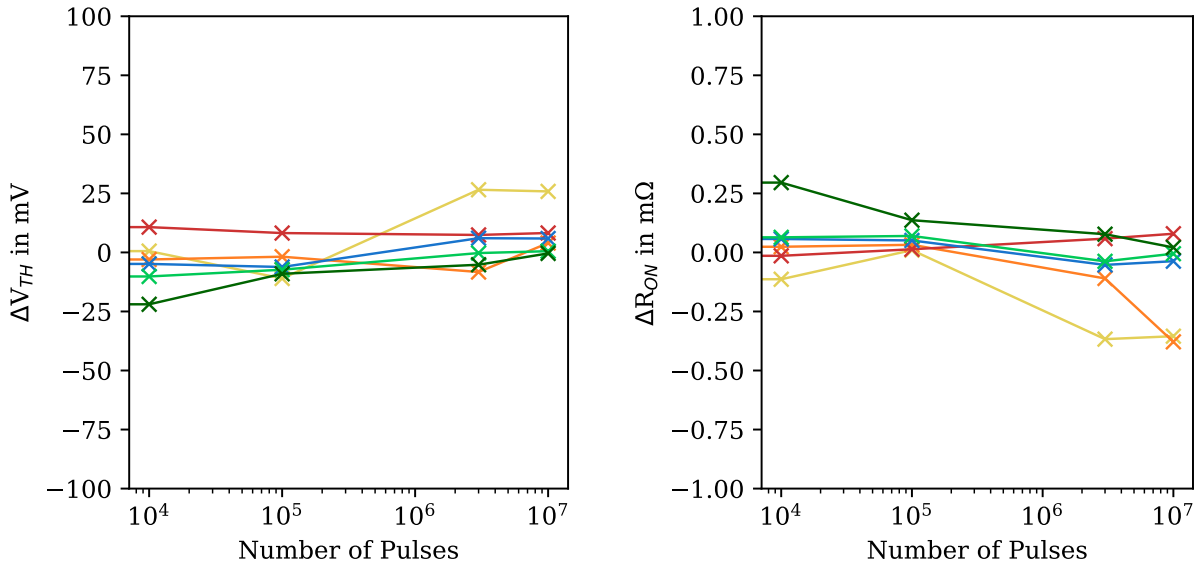
With the SMU measurements only the static device parameters are extracted. To also observe changes in transient behavior of the DUTs an oscilloscope was used to record the switching wave-

forms. Both, V_{DS} and I_d, were recorded during the repetitive current pulses. To acquire the current waveform of the DUT a Rogowski coil was used. In addition to the in-situ oscilloscope recordings during the stress test, further characterization cycles were implemented after every intermediate static device characterization with the SMU. This time, however, a DPT at the nominal data sheet values of the DUT were applied with the test bench. Thereby, the turn-on and turn-off transients of the DUT were recorded for subsequent analysis.

Results and Discussions

To detect potential device degradation the intermediate device characterizations described in the previous section have been done. The measurement intervals were chosen at appropriate intervals such potential device degradation can be monitored currently. Similar to the results presented in [2] V_{TH} and R_{ON} have been monitored with static device characterizations and are presented in the following section. For the discussion of the dynamic behavior the presented results below focus on the turn-off transient.

Static Behavior. As shown in Fig. 3, the measurements of V_{TH} and R_{ON} do not reveal any drift throughout the stress test. Past research has shown that V_{TH} and R_{ON} can have instabilities under pulsed



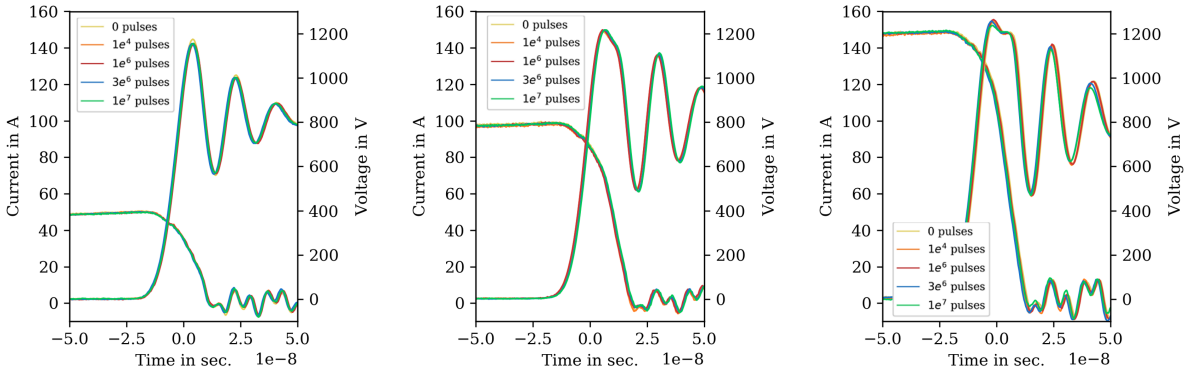
(a) Measured ΔV_{TH} drift

(b) Measured ΔR_{ON} drift.

Fig. 3: Measurement results of the static device characterizations.

gate stress conditions. Within the scope of [2] numerous switching conditions and static tests were applied to SiC devices to show a drift of V_{TH} and R_{ON} under certain conditions. It also showed that a large number of gate switching stress pulses are necessary to cause a significant drift of V_{TH} and R_{ON}. New state of the art qualification procedures for SiC MOSFETs allow this drift phenomena caused by dynamic pulses to be better understood, controlled and improved. Based on the characterization results presented in Fig. 3 there is no noticeable drift in V_{TH} and R_{ON} with the herein presented stress conditions. Although the number of gate switching events applied within the here presented experiments is relatively low compared to [2] the aim was to investigate additional degradation caused by high current pulses. Since no degradation could be observed in any of the conducted experiments it can be concluded that the applied high current pulses do not trigger any new degradation mechanisms and with the applied number of pulses do not affect the static device performance of the DUTs.

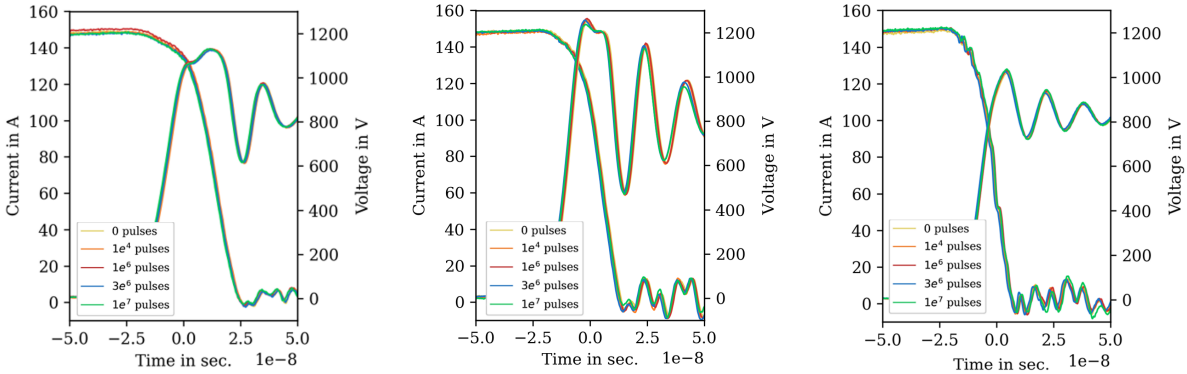
Dynamic Behavior. A similar observation was made for the dynamic behavior. A zoomed view of the turn-off behavior is depicted in Figs. 4 and 5. Also, there no noticeable change in the DUTs'



(a) $V_{GH} = 20\,V$, $V_{GL} = -10\,V$, $I_d = 50\,A$ (b) $V_{GH} = 20\,V$, $V_{GL} = -10\,V$, $I_d = 100\,A$ (c) $V_{GH} = 20\,V$, $V_{GL} = -10\,V$, $I_d = 150\,A$

Fig. 4: Dynamic behavior during the DUT's turning-off recorded throughout the stress test for different I_d levels.

switching behavior was observed throughout the test. Because of the critical loop inductance there is still an overshoot in the V_{DS} present. Figure 4 shows the results of the turn-off behavior for different current levels at t_2. A higher voltage overshoot can be observed when the current is increased. Although these overshoots exceed the maximum values of the tested device during turn-off of the repetitive high current pulses, the device still show the same behavior as before the stress.



(a) $V_{GH} = 20\,V$, $V_{GL} = 0\,V$, $I_d = 150\,A$ (b) $V_{GH} = 20\,V$, $V_{GL} = -10\,V$, $I_d = 150\,A$ (c) $V_{GH} = 20\,V$, $V_{GL} = -15\,V$, $I_d = 150\,A$

Fig. 5: Dynamic behavior during the DUT's turning-off recorded throughout the stress test for different V_{GL} levels.

All curves in Fig. 5 were recorded at 6 times the nominal current value of the MOSFET. Here the gate drive conditions were varied, and no aging effects can be seen either. The recordings show a slightly different switching speed for each gate condition and the overshoot of V_{DS} differs for each condition. Since the same gate resistance was used for each experiment the gate current will be different for each of the test conditions in Fig. 5. Nevertheless, neither the high overshoots in these experiments nor the high current pulses themselves appear to degrade the dynamic behavior of the device.

Conclusion

The experiments presented in this paper demonstrate the robustness of SiC MOSFETs subjected to short repetitive high current pulses. With our test bench we were able to adjust the gate driving- and circuit- parameters to emulate the pulses the DUTs might experience throughout their lifetime. Within the scope of the herein presented experiments the gate driver's turn-off voltage (V_{GL}) and the peak drain current have been varied. Changing the operating conditions, i.e. different level of V_{GL} and I_d, altered the circuit behavior. However, since the gate resistance was kept constant these results are not unexpected. Nevertheless, there appears to be no negative effect when turning the device off with a negative gate bias. Within the scope the herein presented experiments current levels up to 6 times the nominal values were applied. It was shown that the tested SiC MOSFETs do not electrically degrade under such harsh operating conditions. Neither, static readouts revealed any degradation of V_{TH} and R_{ON} nor did the oscilloscope recordings of the dynamic behavior of the DUTs. In conclusion, after 10 million applied stress pulses under each of the presented test conditions there appears to be no adverse effect onto the electrical performance of the investigated DUTs.

High current pulses such as the ones presented in this investigation are usually not covered by data sheet values currently. Therefore, an investigation such as this one is inevitable to study the robustness of SiC MOSFETs under such harsh operating conditions. In case of the herein investigated SiC MOSFETs we have demonstrated that the DUTs can handle the applied stress without revealing any electrical degradation. Such robustness against short-term high current pulses opens the potential to use parts rated closer to the normal operating conditions thereby enabling more compact system designs. Nevertheless, more investigations are necessary to apply such results to a broader range of SiC MOSFET products.

Acknowledgement

This work was funded by the Austrian Research Promotion Agency (FFG, Project No. 884573). Furthermore, the authors would like to thank Judith Specht and Thomas Laska for their valuable input. We also thank Konstantinos Patmanidis for his preliminary research and development of the test setup.

References

[1] M. Sievers, B. Findenig, M. Glavanovics, T. Aichinger, and B. Deutschmann, "Monitoring of parameter stability of SiC MOSFETs in real application tests," *Microelectronics Reliability*, vol. 114, p. 113 731, 2020, 31st European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, ESREF 2020. DOI: 10.1016/j.microrel.2020.113731.

[2] P. Salmen *et al.*, "Gate-switching-stress test: Electrical parameter stability of SiC MOSFETs in switching operation," *Microelectronics Reliability*, vol. 135, p. 114 575, Aug. 2022. DOI: 10.1016/j.microrel.2022.114575.

[3] T. Mannen, T. Isobe, and K. Wada, "Investigation of multiple short-circuits characteristics and reliability in sic power devices used for a start-up method of power converters," *Microelectronics Reliability*, vol. 114, p. 113 775, 2020, 31st European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, ESREF 2020, ISSN: 0026-2714. DOI: 10.1016/j.microrel.2020.113775.

[4] C. Chen, T. Nguyen, D. Labrousse, S. Lefebvre, C. Buttay, and H. Morel, "New definition of critical energy for sic mosfet robustness under short circuit operations: The repetitive critical energy," *Microelectronics Reliability*, vol. 114, p. 113 839, 2020, 31st European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, ESREF 2020. DOI: https://doi.org/10.1016/j.microrel.2020.113839.

[5] A. Castellazzi *et al.*, "Gate-damage accumulation and off-line recovery in SiC power MOSFETs with soft short-circuit failure mode," *Microelectronics Reliability*, vol. In Press, p. 113 943, 2020. DOI: 10.1016/j.microrel.2020.113943.

[6] T. Basler, *Reliability and robustness of sic mosfets*, ECPE SiC & GaN User Forum, Jun. 2021.

[7] T. Laska, F. Hille, F. Pfirsch, R. Jereb, and M. Bassler, "Long term stability and drift phenomena of different trench igbt structures under repetitive switching tests," in *Proceedings of the 19th International Symposium on Power Semiconductor Devices and IC's*, 2007, pp. 1–4. DOI: 10.1109/ISPSD.2007.4294917.

[8] K. Patmanidis, M. Glavanovics, and A. Muetze, "Scalable multitasking dynamic pulse based reliability stress test for high voltage discrete semiconductors," in *Proceedings of EPE'21*, 2021.

[9] J. P. Kozak, R. Zhang, H. Yang, K. D. Ngo, and Y. Zhang, "Robustness evaluation and degradation mechanisms of SiC MOSFETs overstressed by switched stimuli," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 1135–1140. DOI: 10.1109/APEC39645.2020.9124313.