*Materials Science Forum*
*ISSN: 1662-9752, Vol. 1092, pp 127-133*
*doi:10.4028/p-3g1w6r*

*Submitted: 2022-09-02*
*Revised: 2022-10-19*
*Accepted: 2022-11-25*
*Online: 2023-06-06*

# Reliability of SiC MOSFET Power Modules under Consecutive H3TRB and Power Cycling Stress

Felix Hoffmann[1,a], Stefan Schmitt[2,b], Nando Kaminski[1,c]

[1]University of Bremen, Institute for Electrical Drives, Power Electronics and Devices (IALB), Otto-Hahn-Allee 1, 28359 Bremen, Germany

[2]Semikron Elektronik GmbH&Co. KG, Sigmundstraße 200, 90431 Nuremberg, Germany

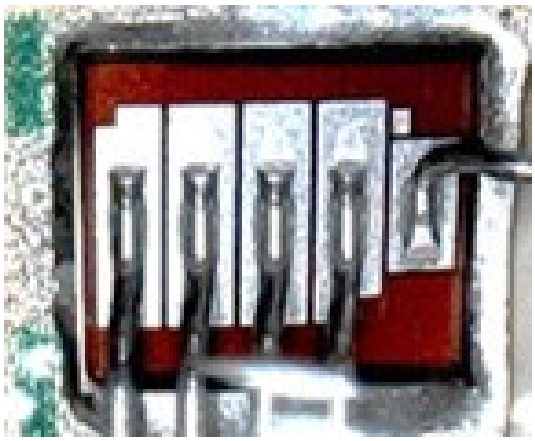
[a]felix.hoffmann@uni-bremen.de, [b]stefan.schmitt@semikron.com, [c]nando.kaminski@uni-bremen.de

**Keywords:** SiC MOSFET, Reliability, High Humidity High Temperature Reverse Bias, H3TRB, Power Cycling, PC, Combined Testing, Multimodal Reliability Testing

**Abstract.** Power semiconductor modules are subject to both thermo-mechanical stress and electro-chemical stress during field operation. Usually, those stressors are investigated separately and possible interaction of both degradation mechanisms is neglected. In this work, the effect of combined thermo-mechanical and electro-chemical stress is investigated by means of consecutive H3TRB and PCT testing. One test group had been subjected to power cycling before the H3TRB test was performed, while another test group had been exposed to H3TRB stress before the power cycling test. As a reference, devices without preconditioning were tested in both, H3TRB and power cycling and are also used to compare the H3TRB and power cycling performance of the SiC devices to similar silicon devices. The results show, that the SiC devices feature a significantly better H3TRB performance than comparable silicon devices, but are inferior in terms of power cycling performance. Furthermore, the results for both test groups of the combined tests indicate that the failure modes for the previously stressed devices were the same as for the pristine devices and no impact of either preceding stress on the devices' lifetime could be observed. Therefore, the results of this work suggest no interaction between both stressors, at least not for the devices used for this investigation.

## Introduction

When power semiconductors are used in harsh environments, they are exposed to electro-chemical stress caused by humidity from the environment [1] and thermo-mechanical stress caused by cyclic changes in power dissipation due to device operation and changing ambient temperatures [2]. At the same time, those applications, e.g. traction or wind power, often require a long service life with low failure rates. In order to ensure that the reliability demands are met, it is crucial to evaluate the impact of both stressors on the devices' reliability to estimate their service life under the respective conditions. Since this is usually investigated separately in High Humidity High Temperature Reverse Bias ($H^3TRB$) tests for electro-chemical stress [3, 4] and Power Cycling Tests (PCT) for thermo-mechanical stress [5, 6], possible interaction of both stressors is not considered. While the electrical performance of SiC power devices make them very attractive for many applications and can drive electrification by increasing efficiency [7, 8], the reliability of SiC devices and particularly the much shorter track record of field reliability is still a potential concern [9]. Due to the high critical field strengths of SiC and its more than 3x higher Young's modulus with respect to silicon, both electro-chemical and thermo-mechanical stress and their interaction can be potentially more critical for SiC compared to their silicon competitors, for which previous reports indicated some degree of interaction [10]. In this work, the reliability of SiC MOSFETs is investigated in terms of electro-chemical and thermo-mechanical stress and specifically, regarding a possible interaction of both stressors by consecutive PCT and $H^3TRB$ testing.



(a) Image of the chip under test, a 1200 V/25 A SiC MOSFET chip with a chip area of approximately 12 $mm^2$


(b) Image of the package under test, a base plate less module package with spring terminals (MiniSKiiP)

Fig. 1: Images of the devices under test

**Devices under Test**

As devices under test (DUTs), SiC MOSFET chips with a nominal blocking capability of 1200 V and a current rating of 25 A were used. An image of the chip under test is shown in Fig. 1a. The chips were packaged in a base plate less module package with spring terminals (MiniSKiiP), depicted in Fig. 1b. The module consists of a DCB substrate with solder die-attach and silicone gel as filler material. For this investigation, a total of 24 SiC MOSFET modules of the same production lot were used.

**Test Procedure**

In order to investigate possible interactions of electro-chemical and thermo-mechanical degradation, both tests were performed consecutively on the same DUTs. The test sequence is illustrated in Fig. 2 and the test conditions for the $H^3$TRB and PCT tests are summarised in table 1. First a PCT (run 1) was performed until end of life (EoL) of all 12 DUTs, to obtain the baseline power cycling capability of the package assembly under test. Afterwards, a second PCT (run 2) was performed until 50 % of the number of cycles to failure ($N_f$) of run 1 was reached. As $N_f$, the Weibull scale factor was considered ($N_{f,63.2}$). In order to investigate a possible impact of preceding PCT stress on the $H^3$TRB performance, and also assess whether the magnitude of the PCT stress has an impact, devices from PCT run 1 and run 2 were used for the subsequent $H^3$TRB test. The test was performed on 4 devices of run 1 (split 1 ”EoL”), 6 devices of run 2 (split 2 ”Precon.”) and 6 fresh devices as a reference (split 3 ”REF”).

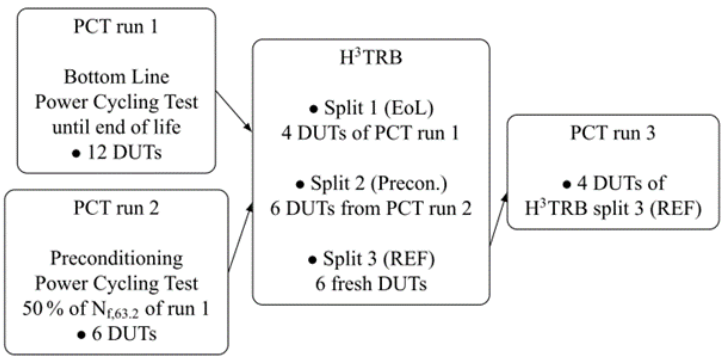



Fig. 2: Flow chart of the sequence of the performed tests

Table 1: Target test conditions of the PCT and H3TRB tests, respectively

| $H^3$TRB Test Conditions | | Power Cycling Test Conditions | |
|---|---|---|---|
| $T_{amb}$ | 85 °C | $\Delta T_{vj}$ | 100 K |
| rH | 85 % | $T_{min}$ | 30 °C |
| $V_{RB}$ | 960 V | $t_{on}$ | 3 s |
| | | $t_{off}$ | 3 s |
| | | $I_{load}$ | 29.3 A |

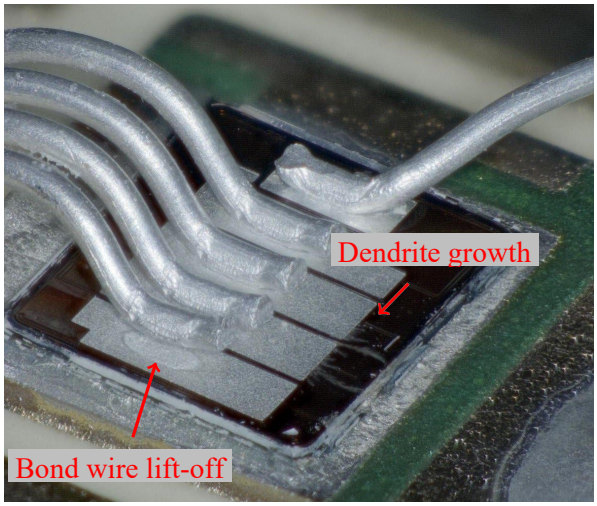



Fig. 3: Microscope image of a chip after consecu- tive PCT and H$^3$TRB stress (H$^3$TRB after PCT)

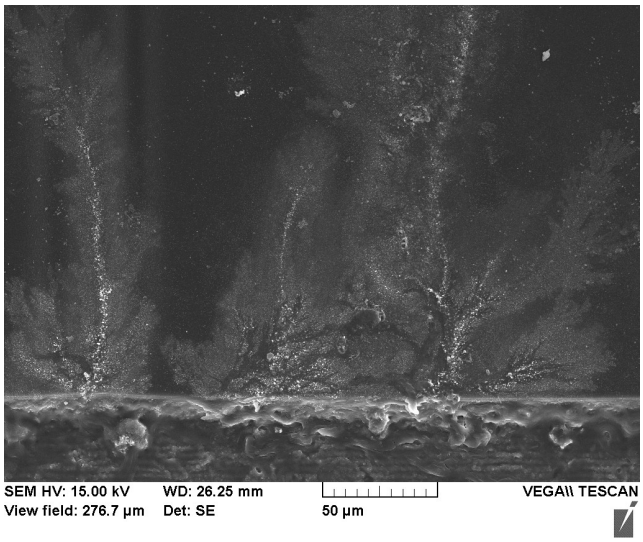



Fig. 4: SEM image of silver dendrites, grown over the edge termination during H$^3$TRB stress

After the H$^3$TRB test, a power cycling test was performed on 4 devices of split 3, which had been subject to H$^3$TRB stress until their parametric end of life, in order to investigate the impact of previous exposure to humidity on the power cycling performance.

**H$^3$TRB after PCT**

The H$^3$TRB test was performed with typical test conditions, i.e. at an ambient temperature of 85 °C and 85 % relative humidity and with a reverse bias voltage of 960 V, corresponding to 80 % of the devices' nominal blocking voltage. As a failure criterion, an increase in leakage current of one order of magnitude was used. DUTs, which had reached the failure criterion, were disconnected and removed from the test. The test was performed until all devices had failed at approximately 12,700 h (i.e. about 1.5 years of net testing time).

**Failure Analysis** After the test, the DUTs were opened for optical failure analysis. Fig. 3 shows a microscope image of one DUT, which was subject to power cycling prior to the H$^3$TRB test. It is visible, that the DUT exhibit a bond wire lift-off of the front most bond wire, which can be attributed to the preceding PCT. Furthermore, dendrites across the right side of the edge termination are visible, which show the degradation caused by the H$^3$TRB test. A scanning electron microscope (SEM) image of part of the dendrites is shown in Fig. 4. An Energy Dispersive X-ray Spectroscopy (EDX) confirmed that the dendrites are composed of silver and grew on top of the passivation layer. Silver dendrites are common to occur during H$^3$TRB stress and are a classical failure mechanism for silicon power semiconductors during H$^3$TRB as well [11]. Other devices showed damage of the polyimide layer, previously reported in [4]. The degradation mechanisms were the same for all DUTs of all three H$^3$TRB test splits and hence, no additional or other degradation mechanisms were triggered by the previous thermo-mechanical stress.

**Statistical Analysis** The Weibull plots of the H$^3$TRB test results are shown in Fig. 5, and the associated Weibull parameters are summarised in table 2. In comparison to the reference data for silicon [4], the Weibull scale factors are significantly higher for all test splits. While this indicates a much higher ruggedness of the SiC devices under electro-chemical stress, as previously reported in [4], this is not necessarily material related, since the considered silicon counterparts are not state-of-the-art designs anymore, because novel silicon devices feature an improved H$^3$TRB performance, too [12]. On the other hand, the Weibull shape factor is much smaller for the SiC devices, which represents the wider failure distribution of the SiC devices. Considering the Weibull scale factors of the three test

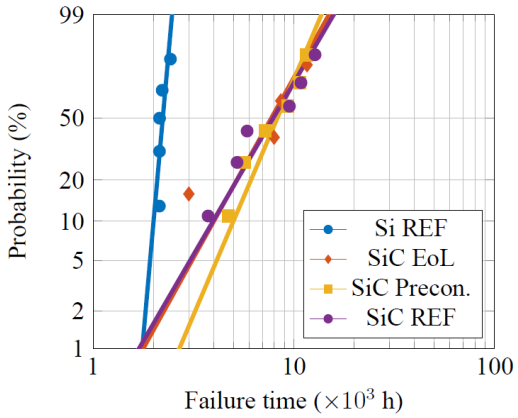



Fig. 5: Weibull plots of the H³TRB test results for all three test splits and data for silicon devices as a reference [4]

Table 2: Weibull parameter of the H³TRB test results for the different splits

| Test split | Scale (h) | Shape |
|---|---|---|
| Si REF | 2270 | 17.82 |
| SiC EoL | 9130 | 3.74 |
| SiC Precon. | 9029 | 2.73 |
| SiC REF | 9310 | 2.66 |

splits of the H³TRB after PCT test, the reference split with the pristine devices features a slightly higher scale factor. However, the difference between the preconditioned devices and the reference split is only marginal, i.e. less than 3 % between the REF split and the one with the lowest scale factor (Precon. split). Considering the error margins, no significant difference between the test splits can be derived from the test results. Hence, the results suggest that the previous thermo-mechanical stress induced by the preceding power cycling test did not affect the lifetime under H³TRB stress for the investigated devices.

**PCT after H³TRB**

The PCT after H³TRB was performed on 4 DUTs of test split 3, i.e. the reference split for the H³TRB test, which had not been subjected to any preceding stress before the H³TRB test. As failure criteria for the power cycling test, a step-increase in $V_{DS}$ was used as an indicator for bond wire failure (BW), and a 15 % increase in $R_{th}$ was used as failure threshold for chip solder degradation (CSD). The power cycling test was conducted with constant on and off times of 3 s, at a target temperature swing of 100 K, minimum temperature of 30 °C and with a load current of 29.3 A. Due to the effect of a settling process of the thermal interface between DUT and heatsink, common for this package type, the temperature swing dropped by approximately 4 K within the first few 100 cycles. For that reason, the actual temperature swing was slightly lower than targeted.

**Failure Mechanism** The characteristics of $V_{DS}$ and $R_{th}$ of all 4 DUTs are shown in Fig. 6. All DUTs exhibited an increase in $V_{DS}$ and $R_{th}$ towards their parametric end of life. Three of the four devices showed only a gradual increase of $V_{DS}$ and $R_{th}$ and surpassed the CSD failure criterion of 15 % increase in $R_{th}$ without any indication of bond wire failure. One DUT exhibited multiple step increases in $V_{DS}$, indicating bond wire failure, shortly before the $R_{th}$ failure criterion was met. Previously published power cycling test results for modules of the same production lot [6] showed that the dominating failure mode for the applied test conditions is CSD, but some bond wire failures can be expected as well. Therefore, the results of this test do not indicate a shift in failure mode due to the preceding H³TRB test. Since the $R_{th}$ only indicates degradation of the thermal path without further information about the location, the thermal impedance characteristics $Z_{th}$ was also monitored frequently during the test. The $Z_{th}$ characteristics of one DUT during the PCT run 3 is shown in Fig. 7.

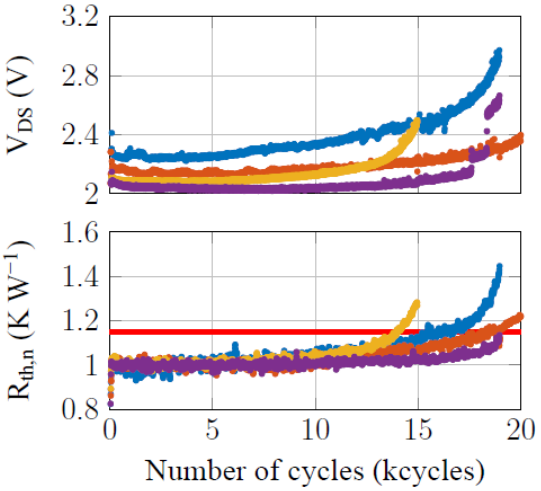



Fig. 6: Characteristics of $V_{DS}$ and $R_{th}$ of the four DUTs of test split 3 during the PCT test, performed after the DUTs parametric end of life during H$^3$TRB

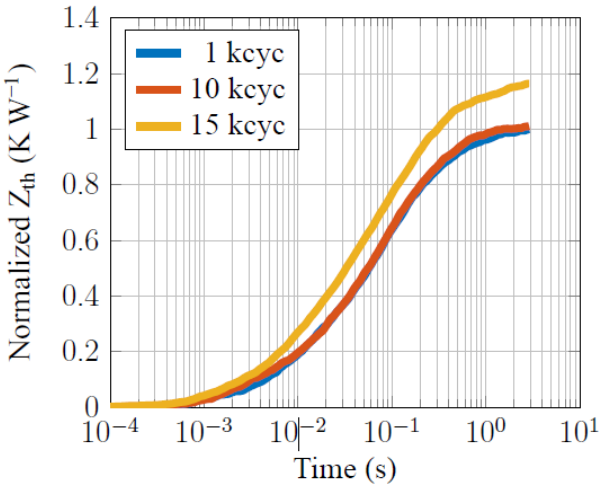



Fig. 7: $Z_{th}$ characteristics of DUT 3 split 3 (yellow line in Fig. 6 ), failed due to chip solder degradation during the PCT performed after the H$^3$TRB test (PCT run 3)

The $Z_{th}$ characteristics exhibit a change in the time domain of 1 ms to 10 ms in the measurement taken at 17 kcycles. Degradation in this time domain is typical for chip solder degradation of this package type [10], which confirms that the underlying failure mechanism of the DUTs was indeed CSD.

**Lifetime Analysis** The test results are shown in the lifetime plot in Fig. 8, with the cycles to failure corresponding to the Weibull scale factor and the error bars indicating the standard deviation of $\Delta T_{vj}$ for the x-axis and $N_f$ for the y-axis, respectively. As a reference, a lifetime model obtained for identical devices of the same production lot, is also shown [6]. The lifetime model is obtained by a parameter fit on the simplified CIPS08 model according to the inset equation in Fig. 8. The corresponding parameters for the devices under test as well as for comparable silicon devices in the same package are given in the inset table in Fig. 8. As published before [6], the number of cycles to failure of the SiC MOSFETs is only approximately 25 % of the number of cycles to failure of their silicon counterparts, which is consistent with other studies [13, 14]. Considering the respective error bars, the data point for the results of the PCT after H$^3$TRB is in good agreement with the lifetime model for the module under test. This indicates that the preceding H$^3$TRB stress of several thousand hours did not affect the power cycling capability of the modules.

## Summary and Conclusion

In this work, a possible interaction between electro-chemical and thermo-mechanical stress was investigated by consecutive H$^3$TRB and PCT testing. For that purpose, an H$^3$TRB test was performed on devices, which had been previously exposed to power cycling. Vice versa, a power cycling test was performed on devices, which were subject to a preceding H$^3$TRB test. As a reference, pristine devices were also tested in H$^3$TRB and PCT. The performance of the preconditioned devices during the respective reliability test was not affected by the preceding stress for both test sequences. Therefore, the results of this investigation suggest that there is no significant interaction between thermo-mechanical and electro-chemical stress for the considered SiC power modules and hence, both stressors can indeed be investigated separately. Furthermore, the excellent H$^3$TRB performance of the investigated SiC power modules proves, that despite the higher electrical fields of SiC edge terminations, their reliability against electro-chemical stress is not compromised and properly designed SiC power modules are indeed suitable to be operated in harsh environments.

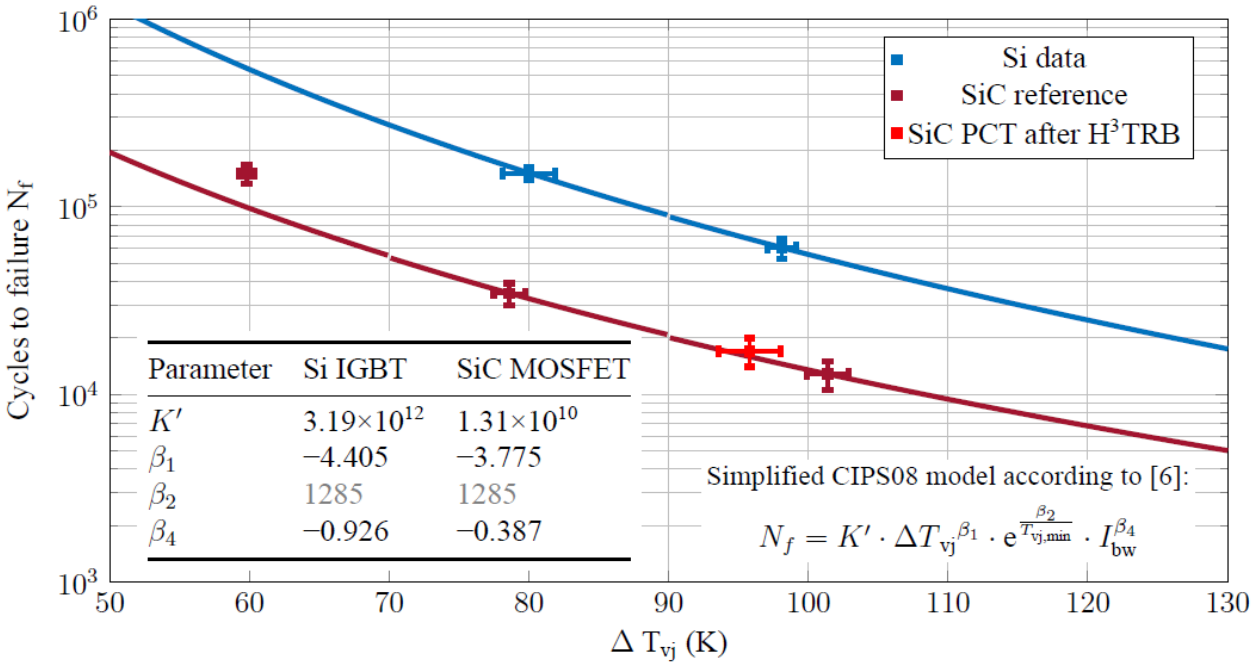



Fig. 8: Lifetime plot of the power cycling test results (Weibull scale factors considered as $N_f$), with reference data for comparable silicon devices for comparison [6]. All 4 DUTs (including the DUT with bond wire failure shortly before the $R_{th}$ failure criterion was reached) were used for the statistical analysis. The error bars indicate the standard deviation of $N_f$ and $\Delta T_{vj}$. The lifetime curves are obtained using a fit on the simplified CIPS08 model according to [6]. The parameter for the impact of $T_{min}$ ($\beta_2$) was not fitted but taken from the original model.

## References

[1] B. Kostka, D. Herwig, M. Hanf, C. Zorn, and A. Mertens, "A concept for detection of humidity- driven degradation of igbt modules," *IEEE Transactions on Power Electronics*, vol. 36, no. 12, pp. 13 355–13359, 2021.

[2] M. Mermet-Guyennet and M. Piton, "Railway traction reliability," in *2010 6th International Conference on Integrated Power Electronics Systems*, 2010.

[3] T. Barbieri, A. Barkley, E. Ayerbe, Z. Major, M. Tauer, J. Young, and D. Gajewski, "Reliability Testing of SiC JBS Diodes for Harsh Environment Operation," in *PCIM Europe 2018; Interna- tional Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2018.

[4] F. Hoffmann, S. Schmitt, and N. Kaminski, "Comparison of the h3trb performance of silicon and silicon carbide power modules," *Materials Science Forum*, vol. 1062, pp. 487–492, 2022.

[5] C. Herold, J. Sun, P. Seidel, L. Tinschert, and J. Lutz, "Power Cycling Methods for SiC MOSFETs," in *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, 2017, pp. 367–370.

[6] F. Hoffmann, N. Kaminski, and S. Schmitt, "Comparison of the power cycling performance of silicon and silicon carbide power devices in a baseplate less module package at different temper- ature swings," in *2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2021, pp. 175–178.

[7] N. Soltau, E. Wiesner, E. Stumpf, S. Idaka, and K. Hatori, "Electric-energy savings using 3.3 kv full-sic power-modules in traction applications," in *2020 Fifteenth International Conference on Ecological Vehicles and Renewable Energies (EVER)*, 2020.

[8] A. Hussein and A. Castellazzi, "Comprehensive design optimization of a wind power converter using sic technology," in *2018 International Conference on Smart Grid (icSmartGrid)*, 2018, pp. 34–38.

[9] N. Kaminski, S. Rugen, and F. Hoffmann, "Gaining confidence - a review of silicon carbide's reliability status," in *2019 IEEE International Reliability Physics Symposium (IRPS)*, 2019.

[10] F. Hoffmann, N. Kaminski, and S. Schmitt, "Investigation on the impact of environmental stress on the thermo-mechanical reliability of igbts by means of consecutive h3trb and pct testing," in *2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2021, pp. 371–374.

[11] C. Zorn and N. Kaminski, "Temperature humidity bias testing on insulated-gate bipolartransistor modules – failure modes and acceleration due to high voltage," *IET Power Electronics*, vol. 8, no. 12, pp. 2329–2335, 2015.

[12] J.-H. Peters, M. Hanf, S. Clausner, C. Zorn, and N. Kaminski, "Improved hv-h³trb robustness of a 1700 v igbt chip set in standard power modules," *Microelectronics Reliability*, vol. 126, p. 114211, 2021, proceedings of ESREF 2021, 32nd European Symposium on Reliability of Elec- tron Devices, Failure Physics and Analysis.

[13] C. Herold, M. Schaefer, F. Sauerland, T. Poller, J. Lutz, and O. Schilling, "Power cycling capa- bility of modules with SiC-diodes," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, 2014.

[14] F. Hoffmann and N. Kaminski, "Power cycling performance and lifetime estimation of 1700v sic mps diode modules with multiple chips connected in parallel," in *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2020, pp. 537–540.