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Chip-Top Packaging Technology for SiC Devices Operational at 250°C with Power-Cycling Durability of Over 300,000 Cycles

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Abstract. This study reports on our cutting-edge packaging technology that achieves high power-cycling (PC) durability of silicon carbide (SiC) devices in high-temperature environments up to 250 °C. The key to improving durability is the precise adjustment of the coefficient of thermal expansion (CTE) of the buffer layer bonded onto the SiC chip. It suppresses the creep rupture of the aluminum chip electrode, resulting in a 2.7-fold improvement in the lifetime at 200 °C from the previously reported 334,000 to 905,000 cycles. The developed structure is subjected to a 250 °C test and a lifetime of 350,000 cycles is successfully demonstrated.

Introduction

Power devices using wide-bandgap semiconductor materials, such as silicon carbide (SiC), are garnering attention as a core technology required for establishing a carbon-neutral society with highly efficient power networks and highly electrified transportation sectors. SiC devices have inherently superior material performance in terms of high breakdown voltage and high efficiency. Such devices have already been commercialized and are being steadily introduced globally to build an advanced society [1]. However, high-temperature performance, a distinctive feature of SiC, has not been utilized owing to the insufficient heat-resistance of packaging materials and technologies.

In 2020, we reported the development of chip-top packaging technology that prevented fatigue failure owing to thermal distortion around the chip [2]. As shown in Fig. 1, a buffer layer comprising of a Copper (Cu)-Invar-Cu (CIC) trilayer, whose coefficient of thermal expansion (CTE) is equivalent to that of SiC, was applied to the chip surface for the first time. Consequently, a power-cycling (PC) lifetime of 334,000 cycles (T_{jmax} 200 °C, ΔT_{jmax} 135 °C, t_{on} 1sec) was successfully achieved at 200 °C. Based on these results, the following two points are further investigated in this paper: 1) Advancement of the buffer layer design using the finite element method (FEM) and its verification at 200 and 225 °C, and 2) Attempt at 250 °C operation, which is a one-step harsher condition. In both cases, a lifetime exceeding 300,000 cycles, which is the criterion for high-reliability applications, was successfully achieved.

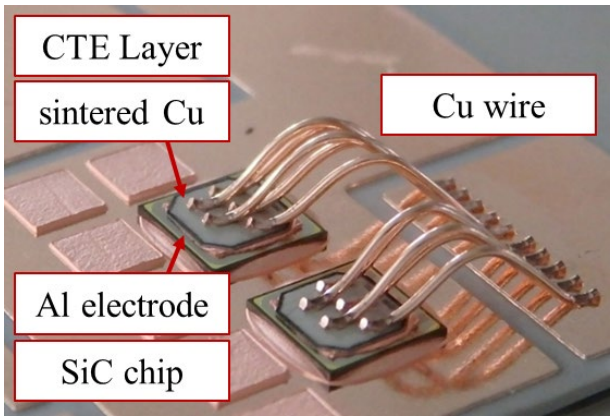


Fig. 1 Overview of the newly developed long-lifetime chip-top packaging technology, including Cu wiring , CTE layer, sintered Cu and SiC chips.

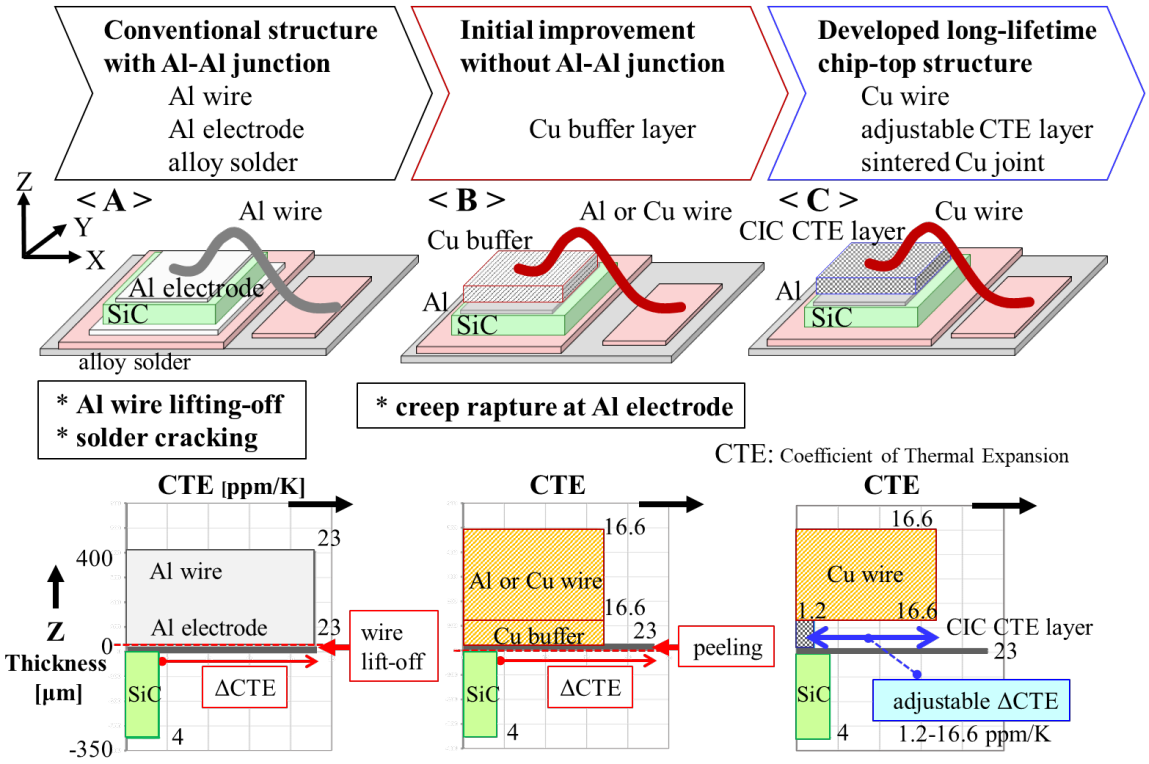


Fig. 2 Summary of the packaging structure for power device chips (upper half) and CTE values of components (lower half) A) Conventional structure: Al wire and Al electrode are used, B) Initial improvement structure: Cu buffer layer on the chip surface, C) Developed structure: chip-top packaging technology with an adjustable CTE layer bonded by sintered-Cu

Chip-top Packaging Technology

Conventional aluminum packaging technology and its wire-lifting-off problems. Figure 2A exhibits a typical packaging structure used in commercially available power devices. Low-melting-point alloy solders, that is, Pb-based and Pb-free alloys, are used for die attachment. On the chip-top side, an aluminum (Al) electrode is widely used, and an Al wire is bonded on top of it. When such a structure is subjected to repeated temperature cycling, "Al wire lifting-off" and "solder cracking" failures occur with a high probability, particularly at temperatures exceeding 175 °C [3,4]. Such failure modes are caused by the CTE difference between the packaging components within the structure. The lower half of Fig. 2 summarizes the CTE distribution around the chip in the thickness direction (z-direction). On the chip-top side, a large interfacial thermal stress is generated at the location of the Al wire junction because the CTE of Al is one order of magnitude larger than that of the chip materials, that is, silicon and SiC. Moreover, exposure to high temperatures accelerates the micro-structural change of Al grains, which gradually degrade bond strength, eventually leading to wire lifting-off failures and breakage.

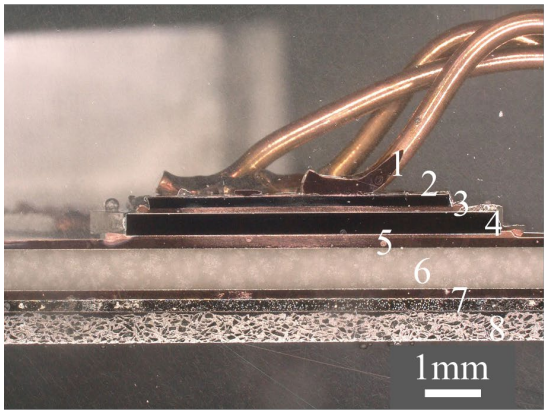
Application of Cu buffer layer and its Al electrode delamination problems. To solve this problem, structures without an Al-Al junction (Fig. 2B) have started to be used, wherein a Cu buffer layer is applied to the chip-top. For such an implementation, either Al or Cu wires can be bonded. However, even with such a structure, the PC lifetime is limited owing to the “delamination of the Al chip electrode” caused by the large CTE difference between Cu and SiC.

Newly developed chip-top packaging technology with CTE adjustable buffer layer. To solve the abovementioned problem caused by the CTE difference, as shown in Fig. 2C and Fig. 3, a buffer layer, called the "CTE layer", was introduced to allow its CTE to be adjusted over a wide range. This CTE layer was bonded by sintered Cu which has a high heat resistance and high thermal conductivity [5]. Adjusting the CTE value reduces the stress at such interfaces and significantly suppresses fatigue failures, as demonstrated by numerical stress-strain analysis by FEM and actual PC tests [2,6].

CTE layer design and the chip-top junction durability. The combined CTE values of the CIC trilayer are designed to be adjustable by over one order of magnitude, from 1.2 to 16.6 ppm/K, by changing the thickness ratio, as shown in Fig. 4 [7]. Within this trilayer, Invar is a nickel-iron alloy with a uniquely low CTE of approximately 1.2 ppm/K. In this study, the CIC layer was specified by the Invar ratio, combined CTE, and ΔCTE. The Invar ratio is the ratio of the Invar thickness to the total thickness. The ΔCTE represents the difference of the combined CTE of the CIC trilayer relative to SiC (4.0 ppm/K). For example, in the case of a Cu-Invar-Cu layer with a 1-3-1 structure, the Invar ratio is 0.6, and the combined CTE and ΔCTE are 5.2 and +1.2 ppm/K, respectively.

To investigate the junction durability at the chip-top, particularly between the CTE layer and SiC with high accuracy, a simple test structure of CTE layer / sintered Cu / SiC single-crystal substrate was fabricated with different CTE designs and subjected to a temperature-cycling (TC) test in a range of -40–250 °C.

Figure 4 shows the scanning acoustic tomography (SAT) images focused on the sintered Cu joint and were acquired before and after the tests. It is evident that, when the ΔCTEs were set sufficiently large from +5.1 to +12.6 ppm/K, cracks and delamination were observed in the early stage of the TC test, at less than 100 cycles, as shown in Figs. 4(2), (3), and (4). Whereas, when the CTEs were precisely adjusted to SiC and the ΔCTEs were set from -1.9 to +1.2 ppm/K such that the difference



1	wire	Cu
2	CTE layer	Cu - Invar - Cu
3	joint	sintered Cu
4	chip	SiC SBD
5	joint	sintered Cu
6	substrate	Cu
		SiN
		Cu
7	joint	SnSb / PbSn solder
8	baseplate	AlSiC

Fig. 3 Cross-sectional structure of the developed chip-top packaging technology. The names and materials of all components are listed.

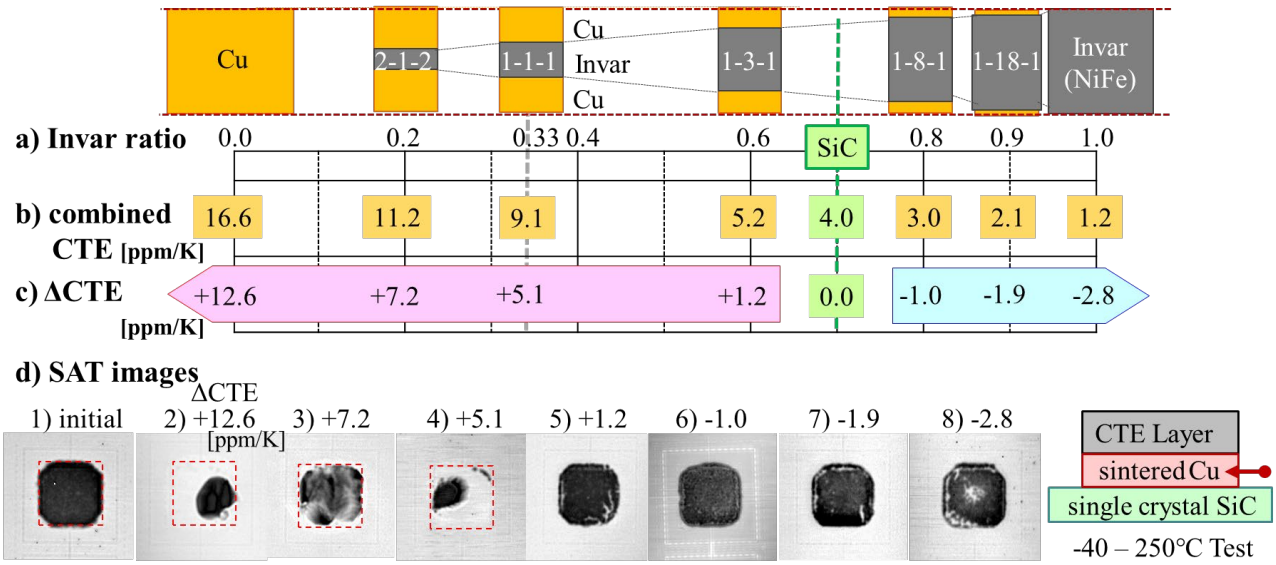


Fig. 4 Temperature-cycling (TC) test of sintered Cu joint between the CTE layer and SiC. The thickness of the CTE layer was fixed at 0.2 mm while the Invar ratio was varied from 0 to 1, corresponding to a ΔCTE ranging from +12.6 to -2.8 ppm/K. As a substrate, a single-crystal SiC wafer with Ni electrodes was used. (conditions: -40 to 250 °C, cycles: 3,500, joint area: 4 x 4 mm^2, method: scanning acoustic tomography (SAT))

with SiC was within 2 ppm/K (Figs. 4(5), (6), and (7)), the junction area was mostly unchanged after severe test conditions of 3,500 cycles. This implied that a highly durable junction was formed and maintained between the CTE layer and SiC chip surface in the sample used for the actual PC test.

Stress reduction effect of the CTE layer calculated by FEM. FEM analysis was performed using the ANSYS Mechanical Enterprise Package to analyze the effectiveness of the CTE layer design and the failure mechanism observed during the PC test. All components from the baseplate to the Cu wires, as shown in Fig. 3, were included, and the stress–strain distributions were analyzed under thermal equilibrium conditions from 25 to 200 °C.

Figures. 5(1) and (2) depict the cross-sectional stress distribution in the structures with the CTE layers of Cu and CIC as examples, corresponding to Structures F and H in Table 2, respectively. Figure 5(3) illustrates the plots of the vertical stress distribution near the Cu wire junction (line a-a') with different CTE designs of CIC. Evidently, at the SiC chip surface (marked by the red dotted square), mounting the CIC CTE layer reduced the stress at the SiC chip surface compared with the Cu layer, and this reduction enhances with an increase of the Invar ratio, corresponding to a decrease in the ΔCTE. The stress reduction was the largest when the 1-18-1 structure with ΔCTE of -1.9 ppm/K was applied. This is explained in detail later.

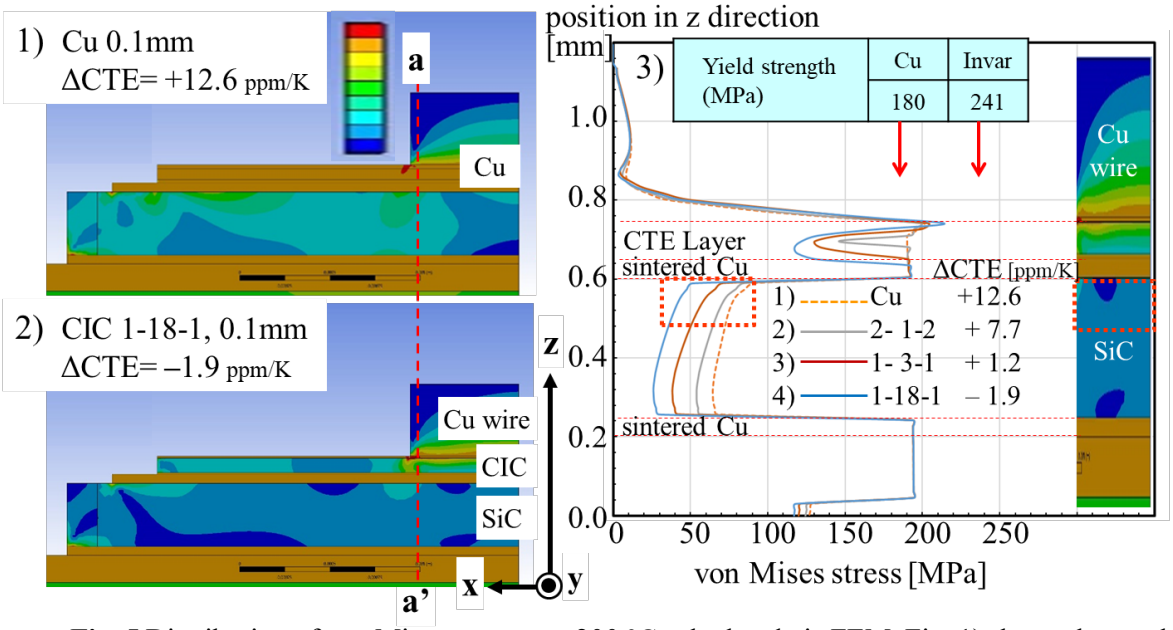


Fig. 5 Distribution of von Mises stresses at 200 °C calculated via FEM. Fig. 1) shows the results from Structure F (Cu layer, ΔCTE of +12.6 ppm/K, 0.1 mm thick) and Fig. 2) from Structure H (CIC, 1-18-1, ΔCTE of -1.9 ppm/K, 0.1 mm thick). Fig. 3) shows the vertical stress distribution along the a-a' line.

Experiments and PC Test Results

Test module structure. The test module samples used in this study were designed for 150 A 1.2 kV half-bridge modules with a footprint of 50 mm × 62 mm. A SiC Schottky barrier diode (SBD) chip (5 mm × 5 mm) was used for the PC tests [2]. Furthermore, sintered Cu was used both at the chip-top and chip-bottom joints [5]. A Cu wire with a diameter of 0.4 mm was bonded on top.

PC test conditions. An active PC test was performed at three different maximum junction temperatures of 200, 225, and 250 °C with a fixed t_{on}/t_{off} of 1/13 sec [2, 6]. Table 1 lists the detailed test conditions and end-of-life (EOL) criteria.

Lifetime controllability by the CTE design. At the time of the first report in 2020 [2], the CTE value of the buffer layer was designed to be equivalent to that of SiC. As listed in Table 2, Structure G (CIC, 0.1 mm thick, ΔCTE of +1.2 ppm/K) designed using this idea exhibits a lifetime of 334,000 cycles [2]. The result is clearly different from the lifetime of 58,000 cycles for Structure F (Cu, 0.1 mm thick, ΔCTE of +12.6 ppm/K), confirming the validity of this idea based on the expertise

Table 1 List of power-cycling (PC) test conditions. Three different conditions are used.

	PCT condition	(i)	(ii)	(iii)
1	T_{jmin} (°C)	65	65	115
2	T_{jmax} (°C)	200	225	250
3	ΔT_j (°C)	135	160	135
4	ton / toff (sec)	1 / 13		
5	EOL criteria (End of Life)	ΔT_j + 20% R_{th} + 20%		

available at that time. Thus, based on these results, a pathway for further improvement was investigated using FEM in this study. Consequently, two directions are identified: 1) lowering the ΔCTE to the negative region, where the CTE value of the buffer layer is below that of SiC, and 2) increasing the layer thickness.

To understand the impact of ΔCTE optimization, test structures with different CTEs were fabricated and tested, as listed in Table 2. Structures A–E were tested at 225 °C conditions, and Structures F–J were tested at 200 °C. Figure 6 presents the trend data of the maximum junction temperature (T_{jmax}) and thermal resistance (R_{th}) obtained from each test condition.

The tests at 225 °C revealed that the lifetime increased proportionally with the increase in the Invar ratio, corresponding to a decrease in ΔCTE [6]. Structure B, which had the highest ΔCTE of +7.7 ppm/K used in the 225 °C test, exhibited a lifetime of 20,300 cycles. By contrast, Structure E, with the lowest ΔCTE of -1.0 ppm/K, achieved a lifetime of 425,000 cycles, which is 20 times longer. It is worth mentioning that ΔCTE of Structure E is in a negative region of ΔCTE. In other words, the CTE is below that of SiC, which is our advanced design principle developed in this study. For reference, Structure A with Al wiring was also tested and had a lifetime of 8,400 cycles, confirming that the developed technology extended the lifetime by two orders of magnitude compared with the conventional one.

A comparable ΔCTE dependence was obtained in the 200 °C tests. Comparing Structure G (ΔCTE of +1.2 ppm/K) with Structure H (ΔCTE of -1.9 ppm/K), the FEM analysis confirmed a 21% reduction in chip surface stress, as shown in Fig. 7, and the PC test results revealed an extension of the lifetime from 334,000 to 472,000 cycles. Evidently, these results indicate that the key to extending the lifetime is to design the CTE value of the buffer layer to be below that of SiC.

Table 2 List of sample structures, power-cycling (PC) test conditions, and obtained lifetimes. ΔCTE represents the difference from SiC (4.0 ppm/K). In this table, G has the same structure as D.

Test Condition	Structure	CTE Layer (Cu-Invar-Cu ratio)		CTE (ppm/K)	ΔCTE (ppm/K)	Thickness (mm)	Lifetime (x10^4 CY)
1) 65 - 225°C	A	< Al wire >		-	-	-	0.8
	B	CIC	2- 1-2	11.7	+7.7	0.1	2.0
	C		1- 1-1	9.1	+5.1	0.1	5.7
	D		1- 3-1	5.2	+1.2	0.1	28.5
	E		1- 8-1	3.0	-1.0	0.1	42.5
2) 65 - 200°C	F	Cu		16.6	+12.6	0.1	5.8
	G (D)	CIC	1- 3-1	5.2	+1.2	0.1	33.4
	H		1-18-1	2.1	-1.9	0.1	47.2
	I		1- 8-1	3.0	-1.0	0.2	84.5
	J		1-18-1	2.1	-1.9	0.2	90.5

Further lifetime extension by the thickness designs. Another pathway, the thickness effect, was examined by doubling the thickness from Structure H (0.1 mm thick, ΔCTE of -1.9 ppm/K) to Structure J (0.2 mm thick). The FEM analysis revealed an additional 32% reduction in stress (Fig. 7), and the PC test showed a lifetime extension from 472,000 to 905,000 cycles (Fig. 6(2)).

Lifetime extension modeling: Effect of developed chip-top packaging technologies. Based on the results obtained from the series of tests at 200 and 225 °C, the cross-sectional observations of the samples after failure were performed to clarify the mechanism of observed lifetime extension. In the short-lifetime structure with a Cu buffer layer (Fig. 8(1), Structure F), delamination was observed over the entire Al electrode layer on the chip surface. On the other hand, no such failure mode was observed in the long-lifetime structure with the thick CIC layer (Fig. 8(2), Structure I), indicating that delamination in this Al layer is the lifetime determining factor.

Such a degradation process can be observable by magnifying the Al layer after EOL, demonstrating that the negative ΔCTE design is evidently effective. At large ΔCTEs, the Al layer apparently became porous and thicker (Fig. 8(4) and (5)) than before the test (Fig. 8(3)). In contrast, when the ΔCTE was set in the negative region of -1.9ppm/K, there was no substantial change in the quality and thickness (Figs. 8(6) and (7)).

Comparing the module components in terms of material strength and heat resistance, the Al layer is the most ductile and weakest material, as confirmed by the following three points. First, Al exhibits the lowest creep initiation temperatures among the major constituent metals. An index of 0.4 times

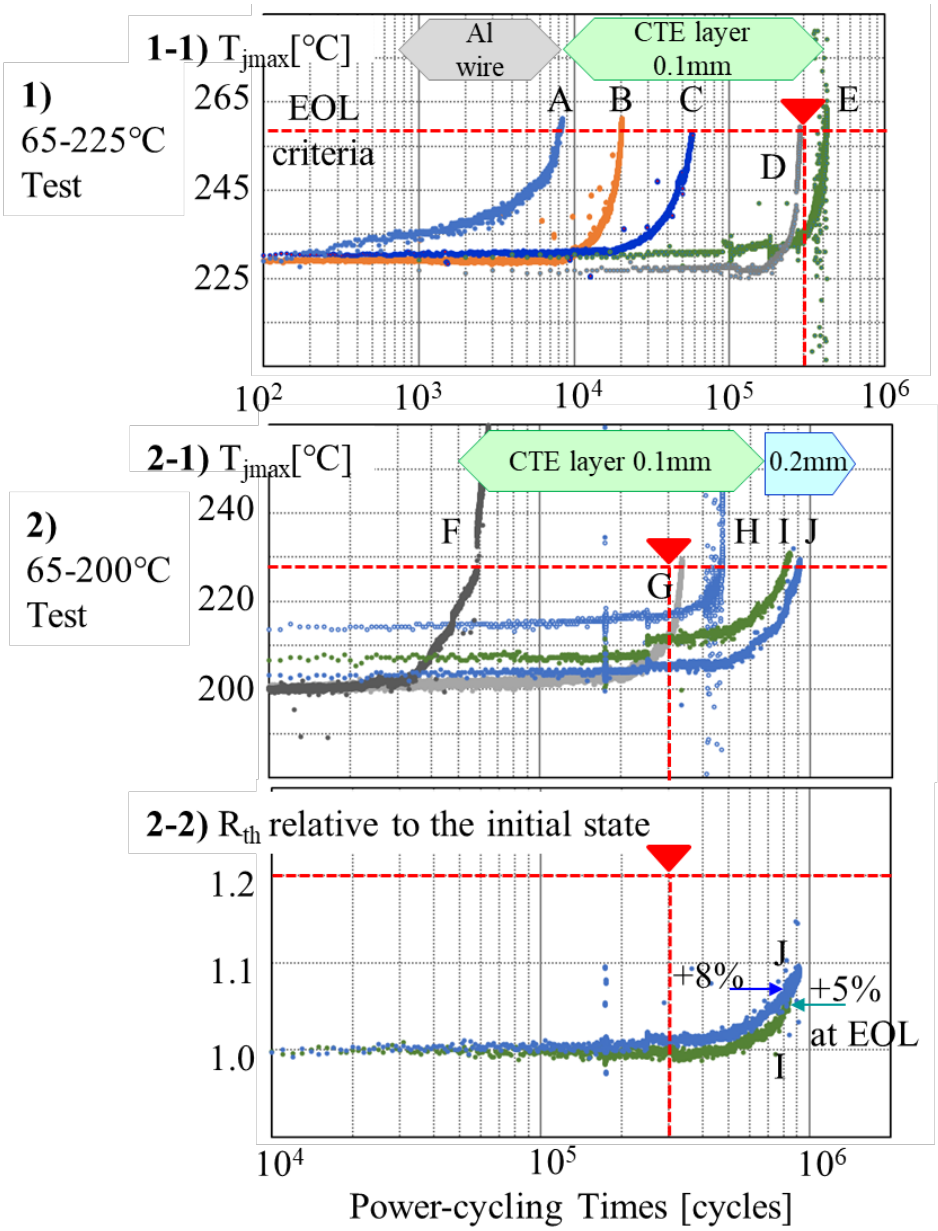


Fig. 6 Trend data of the maximum junction temperature (T_{jmax}) and thermal resistance (R_{th}) relative to the initial state. Figs. 1) and 2) were obtained at conditions of 65-225 and 65-200 °C, respectively. The criteria for high-reliability application of 300,000 cycles is marked as a red triangle. In Fig. 2-2, the increase in R_{th} at the end-of-life is shown.

the melting point (T_m) is generally a good measure [8]. Second, Al exhibits the largest CTE among these metals, causing the largest thermal deformation [0.4 T_m, CTE: Al (100 °C, 23 ppm/K), Cu (270 °C, 16.6 ppm/K), Ni (418° C, 17 ppm/K)]. Third, because this Al layer was grown via the conventional sputtering method, the grain size is much smaller than that of the bulk, typically a few micrometers. Therefore, grain boundaries exist at high densities, and thus their slip-sliding motion

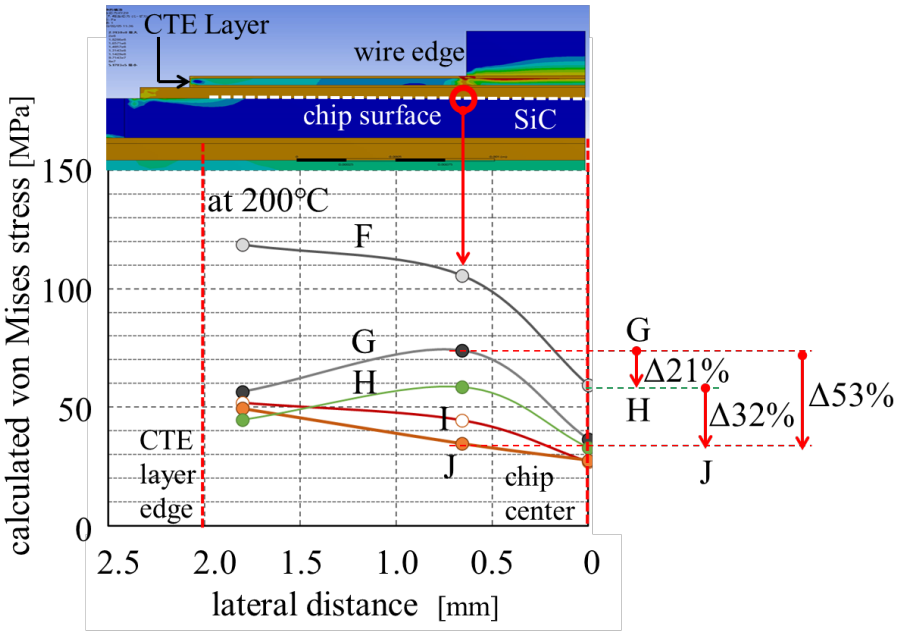


Fig. 7 Stress distribution at 200°C over the chip surface, marked by horizontal white dotted line, in Structures F-J simulated by FEM. The dependence on CTEs and thicknesses of the CTE layer can be observed from the plot.

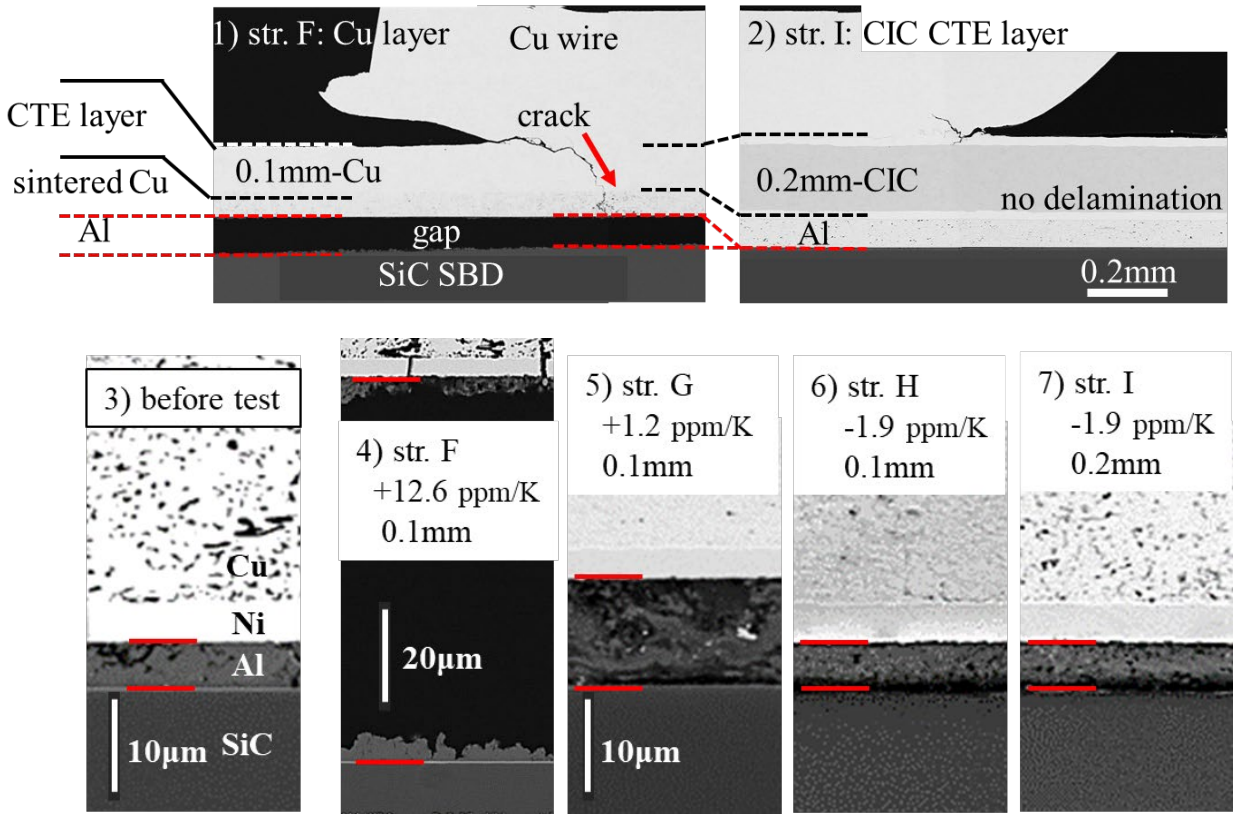


Fig. 8 Longitudinal SEM images of Structures F (1) and I (2). The upper and lower interfaces of the Al electrode layer are indicated by red lines. In Structure F, the Al layer has been completely delaminated after the test. The bottom five magnified images were taken at the Al layers before (3) and after end-of-life (4-7), reveling that the change in thickness and density of the Al layer after the test corresponds well with the ΔCTE design.

occurs at a high probability in such an Al layer. Owing to these factors, the creep-fatigue initiates predominantly in the Al layer by repeated thermal-cycling, and the accumulation of slip-sliding is observed as a thickness increase. This consideration is reported in detail in ref. [6]. Such degradation can be suppressed effectively by our CTE layer design developed in this study.

Additional favorable effects of the CIC CTE layer. i) Formation of tough wire bonding by the CIC CTE layer. Comparing Structures F and I in Fig. 8, it is evident that crack propagation from the Cu wire junction is effectively suppressed in Structure I with the CIC CTE layer. In contrast, in Structure F with the Cu layer, the cracks passed through two layers, including the Cu buffer layer and sintered Cu joint, and reached the chip surface. This difference is primarily because of the inherently tough material property of Invar, which effectively prevents crack propagation. This is reported in detail in ref. [2] [Yield strength at 200 °C: Cu (180 MPa), Invar (241 MPa)] **ii) Addition of thermal capacitance to the chip-top.** As reported in detail in ref. [6], a CTE layer on the chip-top can reduce the transient thermal impedance, which is a measure of the efficiency of heat transfer. The time scale of the transient time is approximately tens of milliseconds, allowing the heat generated in the SBD chip to be transferred with sufficient efficiency to both the chip-bottom and chip-top sides within one second of on-time at every power-cycle. This effectively suppressed the rapid temperature rise and reduced the associated thermal deformation, which is a crucial factor for lifetime extension.

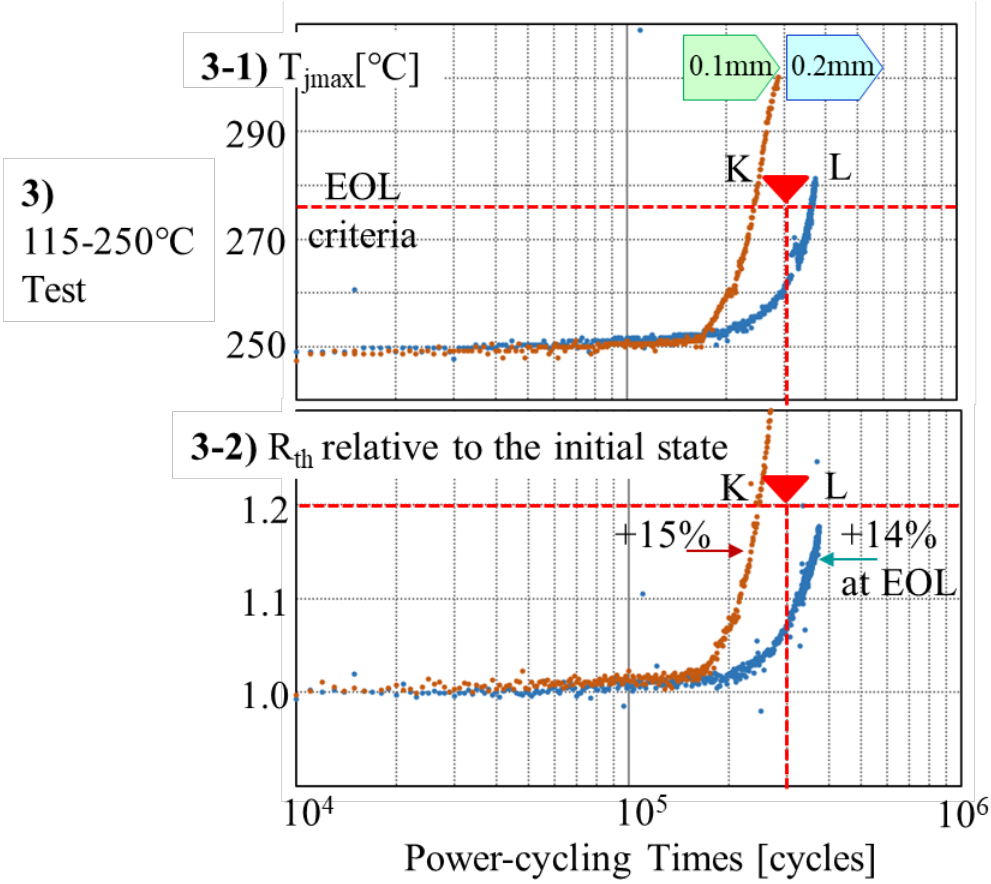


Fig. 9 Trend data of the maximum junction temperature (T_{jmax}) and thermal resistance (R_{th}) relative to the initial state obtained at a condition of 115-250 °C. Two samples were tested and one was depicted for each structure In Fig. 3-2, the increase in R_{th} at the end-of-life is shown.

Table 3 List of sample structures, power-cycling (PC) test conditions, and obtained lifetimes. In this table, K and L have the same structures as E and I, respectively.

Test Condition	Structure	CTE Layer (Cu-Invar-Cu ratio)		CTE (ppm/K)	ΔCTE (ppm/K)	Thickness (mm)	Lifetime (x10^4 CY)
3) 115 - 250°C	K (E)	CIC	1- 8-1	3.0	-1.0	0.1	28.8
	L (I)		1- 8-1	3.0	-1.0	0.2	35.0

Higher Temperature Operation at 250 °C

115-250 °C test and obtained results. The structures designed to be effective at the 200 and 225 °C tests were subjected to the PC test at a higher temperature of 250 °C (ΔCTE of -1.0 ppm/K and thicknesses of 0.1 and 0.2 mm). For the test, the temperature swing ΔT_{jmax} was set to 135 °C, which was the same as that for the 200 °C test (Table 1(iii)). As shown in Fig. 9 and Table 3, lifetimes of 288,000 cycles (Structure K, 0.1 mm thick) and 350,000 cycles (Structure L, 0.2 mm thick) were obtained. The latter structure, which had a lifetime of 845,000 cycles at 200 °C, successfully exceeded the criteria for the high-reliability application of 300,000 cycles under the harsher testing condition.

Discussions: Quests for high-temperature operation. As this study is the first full-scale report of the 250 °C test, the problems identified in this study are summarized to facilitate further high-temperature and high-reliability operations.

Transient thermal resistance analysis was applied to perform a precise examination, which can detect structural degradation nondestructively as changes in the heat capacitance (C_{th}) and thermal resistance (R_{th}). The entire module was divided into four segments as shown in Fig. 10(2), and the changes in each segment before and after the PC test were analyzed.

As depicted in Fig. 10(1), from the 200 °C test of Structure J, the R_{th} values from the four segments from the chip-top structure to the baseplate remained substantially unchanged, with a maximum change of 5%, even after 905,000 cycles. In contrast, in the 250 °C test, an increase of >20% was observed. Such an increase in Segment A at the chip-top structure was also detected as an increase in the electrical series resistance measured by the forward bias characteristics of the SBD, which was not observed in the 200 °C test.

The increase in Segment D (SiN substrate – alloy solder - baseplate) was more pronounced in the 250 °C test than in the 200 °C test. Such a difference was also observed during the PC test in the second half of the test period, particularly when the cycling test approached the EOL. In the 200 °C test, only T_{jmax} predominantly increases while R_{th} remains at a low level (Fig. 6(2-2)). On the other hand, in the 250 °C test, both increased simultaneously and approached the EOL criterion (Fig. 9(3-2)). Although further systematic analysis is needed to specify the failure mode, cracks and voids were observed within the metallic layers of the Al, Cu, and alloy solder.

The observed degradation can be understood by the thermal deformation mechanism of the material combination of Cu and SiC among the major constituents of the module, where the CTE differ by one order of magnitude. When the temperature increased from room temperature to 200 °C, the deformation of Cu was within the elastic region. At approximately 200 °C, the deformation of

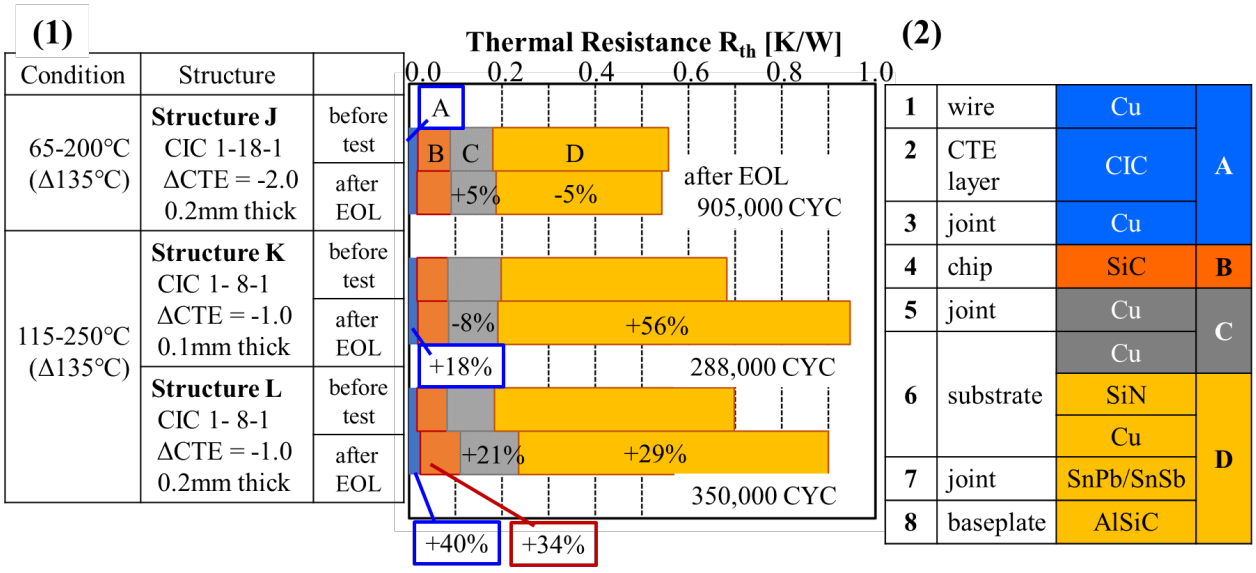


Fig. 10 Transient thermal resistance data of Structures J, K, and L measured before the test and after the EOL. The structure of the module is divided into four segments A-D, as listed in Table (2), the changes in each segment are plotted in Fig. (1). The specific values are listed only when a change of over 5% is observed.

Cu shifted from the elastic to the plastic region. When the temperature was further increased to 250 °C, plastic deformation is accelerated, owing to the decrease in the yield strength of Cu. Once a certain critical point was exceeded, possibly between 200 and 250 °C, the material did not return to its original position during repeated heating-cooling cycles, and such deformation accumulated, eventually leading to failure. The CTE difference problem on the chip-top side, as explained in Fig. 2, has been overcome. However, the CTE difference of the entire module structure remains an obstacle at higher temperatures. To cope with such a problem, it is necessary to use tougher materials with smaller CTE and consider stress buffers at the interfaces. Additionally, the temperature rise tended to be localized, particularly in short on-time PC tests, thus improving heat dissipation is another unavoidable approach.

Summary

SiC power modules operational in high-temperature environments up to 250 °C were successfully developed using the proposed chip-top packaging technologies and exceeded a lifetime criterion of 300,000 cycles, which is required for high-reliability applications. Such a significant improvement was achieved by the application of a buffer layer using the adjustable CTE design, sintered Cu joint, and Cu wiring. In this study, the problems associated with high-temperature applications are also addressed, which provides insights into our further challenges. The developed chip-top packaging technology satisfies all three key performances of high-temperature operation, high breakdown voltage, and high efficiency, and is expected to provide a pathway for developing SiC power devices to the next stage; thus, not only can we effectively realize the redesign and improvements of electronics and cooling systems in existing applications such as automobiles and traction uses, but we can also expect to explore frontier markets by demonstrating high-durability at high-temperature.

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References

[1] T. Masuda *et al.*, 0.63 mΩcm^2 / 1170 V 4H-SiC super junction V-groove trench MOSFET, 2018 IEEE International Electron Devices Meeting, December, San Francisco, CA, USA (2018), 177.

[2] H. Notsu *et al*., SiC module operational at 200 °C with high power-cycling capability realized by fatigue-free chip surface packaging technologies, Proc. PCIM Europe, Germany (2020) 1-8.

[3] K. Suganuma (Ed), Wide bandgap power semiconductor packaging: materials, components, and reliability, Chapter 7, Woodhead Publishing, Sawston, Cambridge, 2019.

[4] R. Amro, Life-Time Estimation of Modern Power Electronics Devices, Noor Publishing, 2017.

[5] H. Nakako *et al.*, "Relation between bonding properties and porosity of sintered Cu bonding", Proc. PCIM Europe, Germany (2019)1-5.

[6] S. Tanaka *et al.*, Extending the Power Cycling Lifetime of SiC Modules Operating at 225°C, Proc. 36th Spring Meeting, Japan Institute of Electronics Packaging, (2022) 25.

[7] G. Jiang *et al.*, Advanced thermal management materials, Chapter 4, Springer, New York, 2013.

[8] A. J. McEvily, Metal failures: mechanisms, analysis, prevention, Chapter 9, Wiley, Hoboken, New Jersey, 2019.