Materials Science Forum
ISSN: 1662-9752, Vol. 1092, pp 145-149
doi:10.4028/p-2953f7

Submitted: 2022-09-02
Revised: 2022-12-02
Accepted: 2022-12-04
Online: 2023-06-06

Avalanche Robustness Investigation of SiC Avalanche Diodes at High Temperatures

Takato Sekiguchi [1,2,a], Masaya Mochizuki [1,2,b], Masayuki Yamamoto[1,2,c]
Koji Nakayama [1,d], Yasunori Tanaka [1,e]

[1]National Institute of Advanced Industrial Science and Technology 1-1-1 Umezono, Tsukuba, Ibaraki, Japan

[2]Department of Electrical and Electronic Engineering, University of Yamanashi 4-3-11 Takeda, Kofu, Japan

[a]sekiguchi-takato@aist.go.jp, [b]mochiduki-masaya@aist.go.jp, [c]yamamoto.masayuki@aist.go.jp
[d]koji.nakayama@aist.go.jp, [e]yasunori-tanaka@aist.go.jp

Keywords: avalanche energy, unclamped inductive switching (UIS), high temperature, diode

Abstract. The avalanche robustness of 430 V SiC avalanche diodes at high temperatures was investigated. The UIS test was performed with a fixed avalanche time t_{ava} to avoid the effect of the thermal diffusion time on the avalanche energy. The avalanche energies at 25 ℃ were found to be 10.5 and 12.7 J/cm^2, while those at 170 ℃ were 8.02 and 9.96 J/cm^2 for t_{ava} = 43 and 72 μs , respectively. Their temperature coefficients were approximately -0.017 and -0.019 J/cm^{2}K, respectively, which were much smaller than those of typical SiC-MOSFETs, which indicated significant avalanche robustness of the SiC diodes even at high temperatures.

Introduction

In recent years, the demand for SiC power semiconductors in electric vehicles has increased. SiC avalanche diodes (AD) connected in parallel with SiC-MOSFETs, which are expected to be used in electric vehicles, can protect SiC-MOSFETs from overvoltage surges [1]. The avalanche robustness of ADs must be validated to optimize the clamping voltage and number of devices in parallel and to provide adequate protection. We developed ADs and reported their avalanche voltages and surge suppression abilities in circuits [2]. In this paper, we report the avalanche robustness of an AD in the high-temperature range using the unclamped inductive switching (UIS) test because automotive parts are required to operate in a wide range of temperatures. Our UIS test was performed with the same avalanche time because the avalanche energy dependency on the thermal diffusion time is non- negligible [3][4]. The temperature dependence of avalanche robustness was investigated and their high capability was obtained even at high temperatures.

Device Structure and Fabrication

Figure 1 shows the cross-sectional device structure of the fabricated AD. Its active area and breakdown voltage were 3.14 mm^2 and approximately 430 V, respectively (Figure 2). We used 4 ° off-axis n+ 4H-SiC(0001) wafers (350 μm thick) as substrates to grow the n-drift layer (6.6×10^{16} cm^{-3}, 3.2 μm). The p + anode region (junction depth 1.2 μm) was formed by Al+ ion implantation at 600 °C. The substrate was then annealed at 1650 °C for 5 min to activate the dopant. A mesa structure was formed by etching up to 3.8 μm for fabricating an AD with excellent surge absorption performance [5]. The chips were then mounted on direct-bonded copper (DBC) substrates with solders and heated in a reflow oven for melting and bonding.

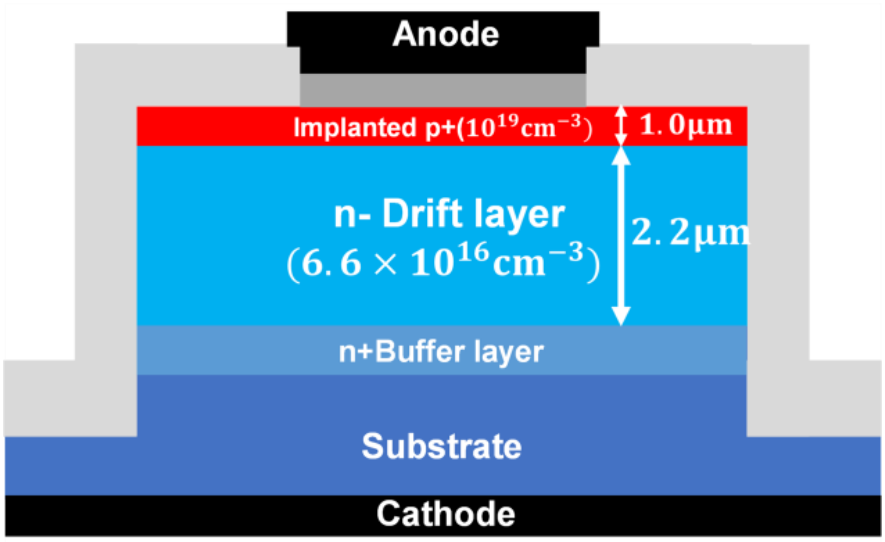

Fig. 1 Cross-sectional schematic of a 4H-SiC avalanche diode.

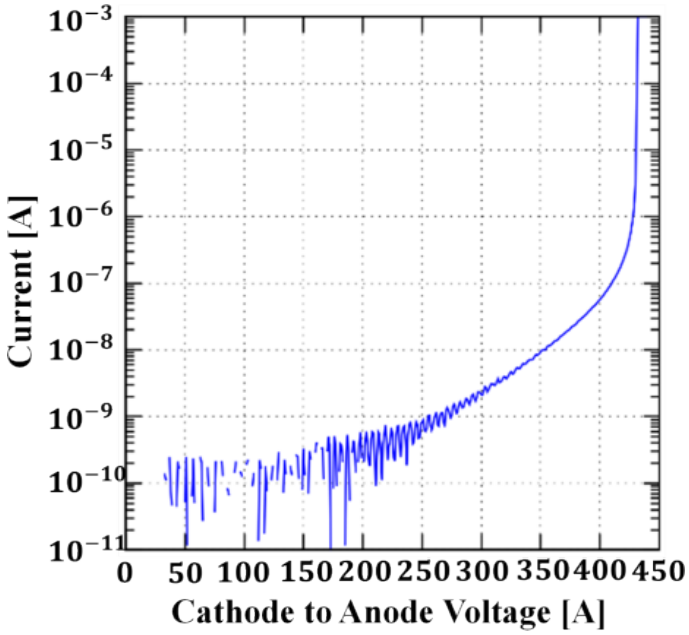

Fig. 2 Reverse IV characteristics of a fabricated 4H-SiC avalanche diode.

Experimental Method

Figure 3 and 4 show the UIS test circuit diagram for evaluating the avalanche robustness and actual experimental apparatus, respectively. The load inductors (L) were 500 μH and 1 mH, respectively. The SiC-MOSFET is usually in the off state, and the capacitor is charged with bus voltage (V_{bus}). When the SiC MOSFET (STMicroelectronics, SCT30N120) was turned on, the current started flowing and increased linearly. Meanwhile, energy was stored in the inductor. When the SiC-MOSFET was turned off, the cathode-to-anode voltage (V_{KA}) of the AD rose rapidly, the diode was shifted into avalanche mode, stored energy was consumed by the AD, and avalanche current (I_{ava}) decreased to zero. During avalanche mode, the V_{KA} was nearly equal to its breakdown voltage. When the current became zero, at which we define the avalanche time (t_{ava}), the avalanche mode was over and V_{KA} eventually settled to V_{bus}.

The avalanche energy is calculated from the current and voltage waveforms obtained during the successful test just before failure using the following equation:

$$E_{ava} = \int^{t_{ava}} V_{KA} I_{ava}\, dt. \quad (1)$$

We evaluated the initial temperature dependence of E_{ava}. Note that our UIS test was conducted by adjusting the bus voltage and current peaks so that device failure occurred almost simultaneously. This method avoids the effect of thermal diffusion time on avalanche robustness, which should be considered in the case of a conventional UIS test where the avalanche peak currents are fixed [6][7]. The cathode-to-anode voltage was measured with a high-voltage differential probe (Tektronix, THDP0200), and the avalanche current was measured using an AC current probe (Tektronix, P6021A). For the UIS tests at different device temperatures (25 − 170 ℃), the ADs mounted on the DBC substrate were placed on a hot plate, and the device temperature (T_C) was monitored from above the DBC substrate using a thermographic camera (Fluke, Ti25).

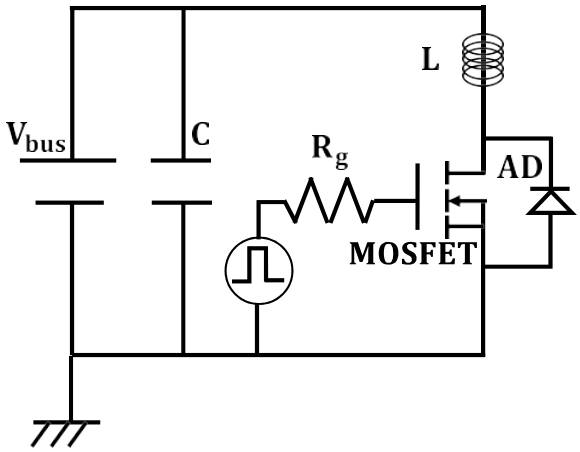

Fig. 3 UIS test circuit.

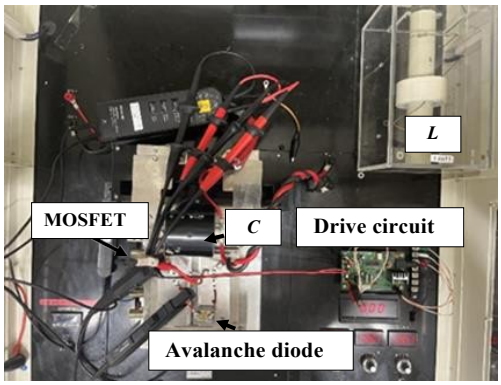

Fig. 4 Image of the UIS test circuit used in this experiment.

Table I Parameters in UIS test circuit.

Symbol	Meaning	Value
V_{bus}	Bus voltage	160–230 V
L	Inductor	500 μH, 1 mH
C	Capacitor	60 μF
R_g	Gate resistor	30 Ω (on), 470 Ω (off)
MOSFET	SiC-MOSFET	1200 V, 45 A

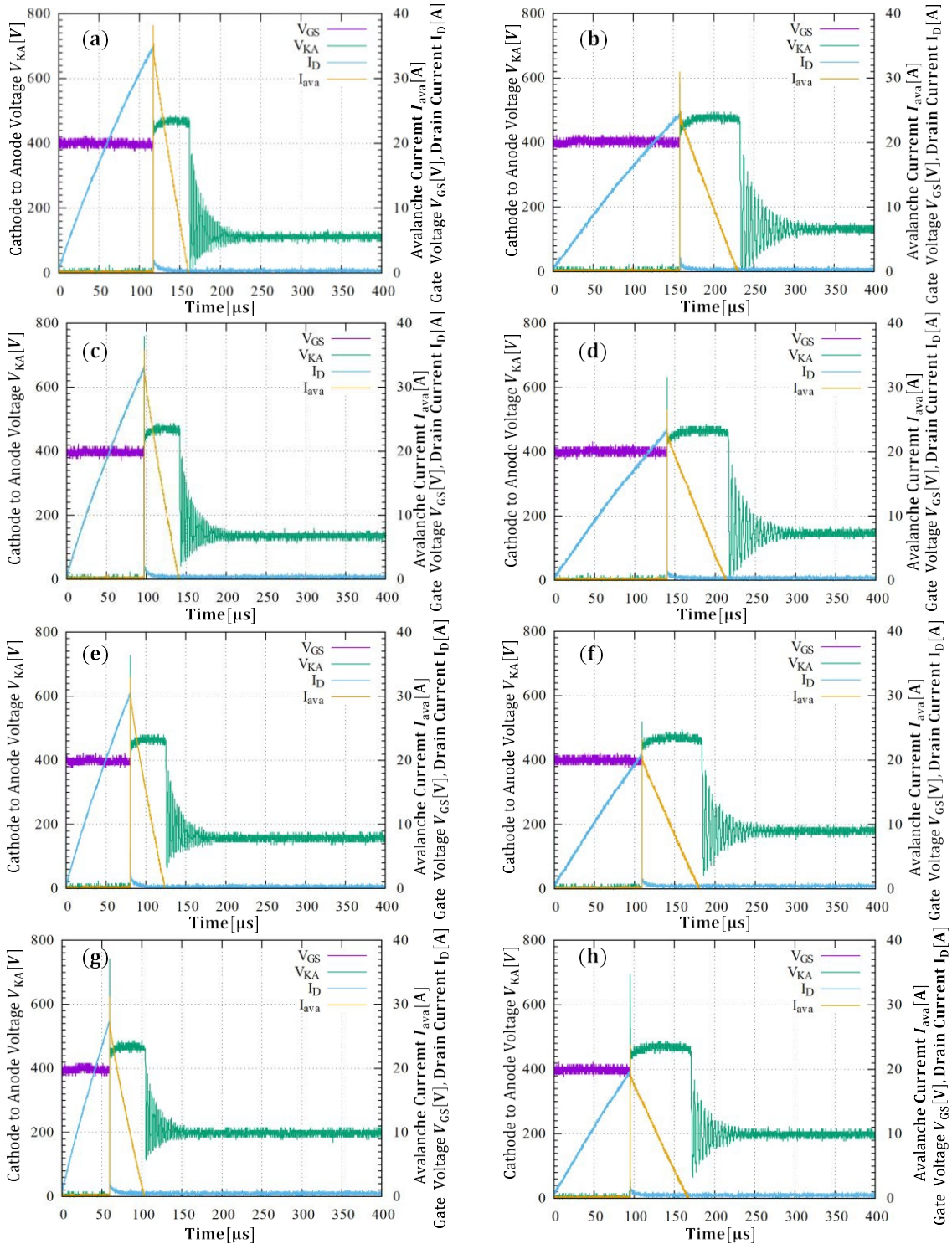

Fig. 5 The UIS waveforms at each ambient temperature and avalanche time. L=500 μH for (a)–(d) and L=1 mH for (e)–(h). Purple, green, light blue, and yellow lines are the gate voltage (V_{GS}), cathode-to-anode voltage (V_{KA}), drain current (I_D), and avalanche current (I_{ava}), respectively.

Results

Figure 5 shows the UIS waveforms for different temperatures and avalanche times. We set the avalanche time to 43 and 72 μs for L=500 μH and 1 mH, respectively. The peak avalanche current decreases as the temperature increases. Figure 6 shows the normalized avalanche energy E_{ava} as a function of the square root of the avalanche time $\sqrt{t_{ava}}$. The E_{ava} were 10.5 J/cm^2 for t_{ava} = 43 μs ($\sqrt{t_{ava}}$ = 6.56 $\sqrt{\mu s}$) and 12.7 J/cm^2 for t_{ava} = 72 μs ($\sqrt{t_{ava}}$ = 8.49 $\sqrt{\mu s}$) at 25 °C. This clearly shows that the avalanche energy increased as the avalanche time increased. This is because a longer

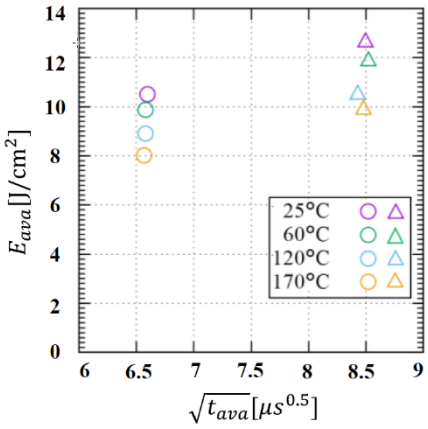

Fig. 6 Normalized avalanche energy as a function of the avalanche time period at various ambient temperatures.

avalanche time results in wider joule heat dissipation. The avalanche energy has been reported to be a linear function of the square route of avalanche time [4][5]. Hence, evaluating avalanche robustness at different temperatures with the same avalanche time is important.

At 170 ℃ , the E_{ava} were 8.02 and 9.96 J/cm^2 for t_{ava} = 43 and 72 μs , respectively. The avalanche energy decreased with increasing temperature. For t_{ava} = 43 and 72 μs, the temperature coefficients of E_{ava} were -0.017 and -0.019 J/cm^{2}K, respectively. These values are much smaller than those reported for SiC-MOSFETs, at which the temperature coefficients of E_{ava} were estimated to be approximately-0.031 J/cm^{2}K [8][9]. SiC ADs maintain high avalanche robustness even at high temperatures.

Summary

In this study, we investigated the avalanche robustness of SiC avalanche diodes at high temperatures using a UIS circuit. Experiments were performed with a fixed avalanche time instead of a fixed avalanche current because the avalanche energy dependency on the thermal diffusion time is nonnegligible. The avalanche energies at 25 ℃ were 10.5 and 12.7 J/cm^2, while those at 170 ℃ were 8.02 and 9.96 J/cm^2 for t_{ava} = 43 and 72 μs , respectively. Their temperature coefficients were approximately -0.018 J/cm^{2}K, which are much smaller than those of typical SiC MOSFETs.

References

[1] K. Koseki, M. Yamamoto and Y. Tanaka, Mat. Sci. Forum 1004, 1129-1133 (2020).
[2] M. Yamamoto K. Koseki, K. Nakayama, Y. Tanaka, S. Nishiyama, Proc. of the 32nd ISPSD, 186- 189 (2020).
[3] A. Konstantinov, H. Pham, D.Waible, B. Lee, K.S. Park, B. Kang, F. Allerstam, T. Neyer, Solid state Electronics 148, 51-57(2018).
[4] A. Konstantinov, F. Allerstam, H. Pham, G. Park, K.S. Park, D.Waible, T. Neyer, Proc. of the 32nd ISPSD, 158-161(2020).
[5] M. Yamamoto, K. Koseki and Y. Tanaka, Proc. of the 31st ISPSD, 171-174 (2019).
[6] J. An, M. Namai, D. Okamoto, H. Yano, H. Tadano, N. Iwamuro, Ele. and Comm. in Japan, Vol. 101, No. 1,24 -31 (2018).
[7] J. An, S. Hu, IEEE JESTPE, Vol. 8, No.1, 206 – 214 (2020).
[8] X. Deng, H. Zhu, X. Li, X. Tong, S. Gao, Y. Wen, S. Bai, W. Chen, K. Zhou, B. Zhang, IEEE transactions on power electronics, VOL. 35, NO. 8, 8524 - 8531(2020).
[9] N. Ren, H. Hu, X. Lyu, J. Wu, H. Xu, R. Li, Z. Zuo, Solid state Electronics 152, 33-40(2019).