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AC-Stress Degradation in SiC MOSFETs

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Abstract. This work presents very recent results regarding threshold-voltage (V_T) degradation due to the application of an AC gate-bias stress (also known as a gate-switching stress). We show that this phenomenon includes both a seemingly-permanent V_T shift and an increase in the observed V_T hysteresis. This degradation effect is found primarily in trench-geometry devices when exposed to what can be described as a negative bias overstress that exceeds the negative bias rating of the device, but that not all trench devices are equally susceptible, suggesting that device design and processing details are critical in limiting the severity of this effect.

Introduction

This work brings together particular aspects of very recent results in SiC MOSFETs regarding both threshold-voltage (V_T) degradation due to the application of an AC gate-bias stress (also known as a gate-switching stress) [1], and its strong dependence in trench-geometry devices on what can be described as negative bias overstress (NBO) effects [2]. AC gate-bias stress induced degradation is a potentially important aspect of V_T instability in SiC MOSFETs that has only recently been revealed [3-8]. Our recent work shows that this phenomenon includes both a seemingly-permanent V_T shift and an increase in the observed V_T hysteresis [1, 9]. It also shows that this degradation effect is proportional to the number of gate-switching cycles, that faster transitions during the switching cycle from accumulation to strong inversion and back again result in larger degradations per cycle, and that this degradation can be annealed out at 300 °C under negative gate bias [1]. Finally, this degradation effect is found primarily in trench-geometry devices when exposed to a NBO that exceeds the negative bias rating of the device [1, 2]. We have also found that not all trench devices are equally susceptible, suggesting that device design and processing details are critical in the severity of this effect. Earlier work that studied bipolar AC stressing failed to find anything of significance, due to the planar devices studied and the relatively small number of switching cycles applied [10].

Fig. 1 illustrates the basic degradation effect that was observed—in certain trench-geometry devices, showing a plot of the variation of both the low side and high side of a V_T hysteresis measurement sequence—wherein first one gate-bias polarity was applied and V_T was measured (by extracting V_{GS} at a fixed current level following a fast *I-V* measurement taking on the order of 10 μs to complete) and then the other polarity was applied and V_T was remeasured, revealing the V_T hysteresis present—as a function of total AC stress cycles applied (all at room temperature). The stress time to measure the V_T hysteresis was 100 μs under each gate polarity, which contrasts with the 200-ns effective stress times applied during the AC stress itself (see the stress-and-measurement schematic shown in Fig. 2). The change in the V_T instability observed is quite dramatic, with the V_T hysteresis increasing from 0.25 V initially to about 2.25 V after 10^{12} total AC stress cycles, with the low side of the V_T hysteresis increasing about 3 V, from 4.7 to 7.7 V and high side increasing by about 5 V, from about 5 to 10 V. It is also interesting to note that the increase in the observed V_T hysteresis occurs only after a significant shift in V_T has occurred first. This is made clearer in the following two figures.

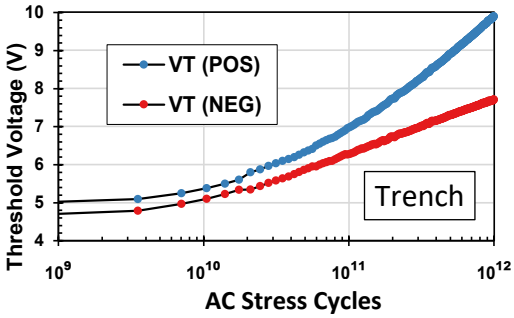

Fig. 1. High side [$V_{T(POS)}$] and low side [$V_{T(NEG)}$] of a V_T hysteresis measurement as a function of AC-stress cycles (at room temperature) in a trench SiC MOSFET (measured using fast *I-V*).

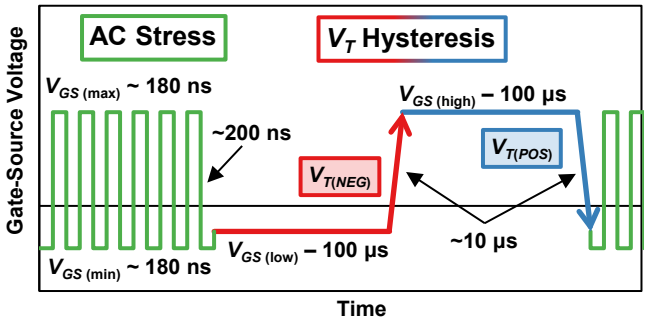

Fig. 2. Schematic showing both the AC-stress cycle and a V_T hysteresis measurement (only one full iteration is depicted before resuming the stress)—all performed at room temperature.

Fig. 3 compares the seemingly-permanent shift in V_T for a trench SiC MOSFET device with the absence of any effect observed in a planar SiC MOSFET (from the same manufacturer). The trench device's V_T begins noticeably shifting between 10^9 and 10^{10} total AC-stress cycles, has shifted about 5 V after 10^{12} total AC-stress cycles, and has shifted more than 8 V after about 10^{13} total stress cycles—with no sign of saturation! Fig. 4 shows that initially, the planar device (which does not degrade) has twice as large a V_T hysteresis as the trench device, but that beyond about 10^{11} total AC-stress cycles, the trench device exhibits a significant increase in its V_T hysteresis (about the time its V_T has shifted about 2 V already). For reasons to be discussed in detail below, this does not represent the activation of additional charge traps. Instead, we have found that this latter effect is due to a significant decrease in the low side of the V_T hysteresis measurement when V_{GS} - V_T shifts positively by several volts. It should also be noted that slow *I-V* measurements on the order of 1 s show just as much V_T shift as fast *I-V* measurements [1], which is to be expected if the V_T shift is due to some sort of permanent charge trapping effect (permanent, at least, until it is annealed out at high temperature, under negative bias [1]). On the other hand, slow *I-V* measurements show much smaller V_T hysteresis effects (and changes in V_T hysteresis) [1], which is also to be expected, since V_T hysteresis is due to dynamic, ephemeral charge-trapping whose magnitude is measurement-speed dependent [11].

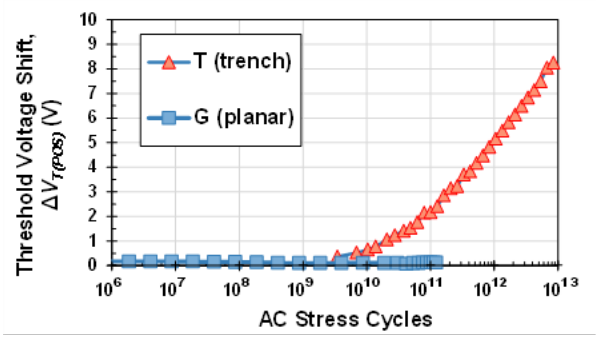

Fig. 3. Comparison of V_T shift in trench and planar SiC MOSFETs (from the same manufacturer) versus the total number of AC-stress cycles.

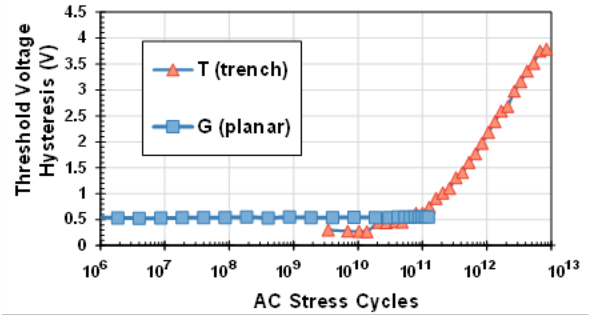

Fig. 4. Comparison of V_T hysteresis in trench and planar SiC MOSFETs (from the same manufacturer) versus the total number of AC-stress cycles.

Figure 5 shows the dependence of the V_T shift versus the total number of AC-stress cycles, as a function of the low-side gate bias [$V_{GS\,(min)}$—see Fig. 2] applied during the AC stress. The more negative the gate bias, the stronger the degradation effect. ($V_{GS\,(min)}$ was −10 V for the results shown in Figs. 1, 3, and 4.) The reference point for calculating the V_T shift is the high side of the V_T hysteresis measurement [$V_{T(POS)}$]. Fig. 6 shows the low-side gate-bias dependence on the corresponding increase in the V_T hysteresis. It is again clear that the increase in V_T hysteresis does not begin until the V_T shift has exceeded at least 1 V , and is not significant until about a 2 V shift.

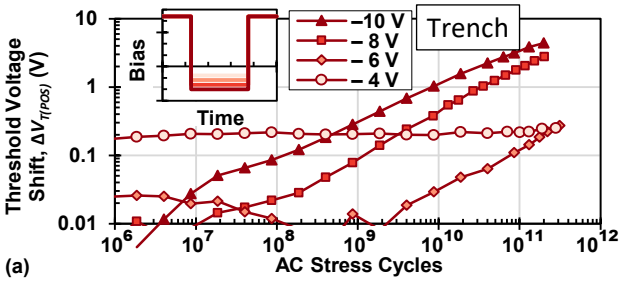

Fig. 5. Effect of the low-side gate bias, $V_{GS\,(min)}$, of an AC Stress on the observed shift in V_T (measured on the high side of the V_T hysteresis envelope), as a function of total stress cycles. $V_{GS\,(max)}$ = +22 V.

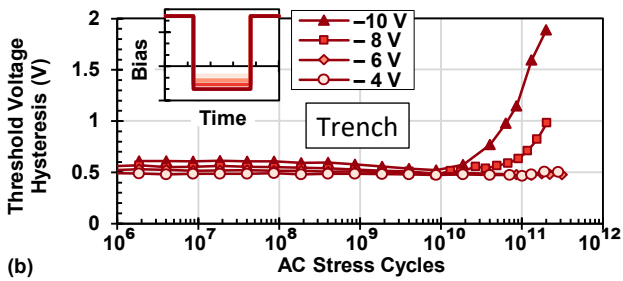

Fig. 6. Effect of the low-side gate bias, $V_{GS\,(min)}$, of an AC Stress on the observed V_T hysteresis (measured using +22 V / –4 V), as a function of total stress cycles. $V_{GS\,(max)}$ = +22 V.

To better understand the relationship between V_T shift and the change in V_T hysteresis due to AC-stress induced degradation, particularly in trench-geometry devices, it is instructive to look at the sensitivity of the V_T hysteresis to the gate bias applied on the low side [$V_{GS\,(low)}$—see Fig. 2] during the V_T hysteresis stress-and-measurement sequence in the absence of AC stress (as-processed devices). Fig. 7 shows how the V_T hysteresis magnitude increases (plotted versus the V_T hysteresis stress interval time) with increasing negative gate-bias (while keeping the high side [$V_{GS\,(high)}$] at +22 V). A significant increase in the magnitude of the V_T hysteresis occurs beginning with $V_{GS\,(low)}$ = –6 V (highlighted in bold), and continues to increase by about 1 V for every 2-V increase in $V_{GS\,(low)}$ up until $V_{GS\,(low)}$ = –14 V (also highlighted in bold), after which the effect quickly begins to finally saturate. (It is no surprise that the maximum negative gate bias specified by the manufacturer for this device is –4 V.) By way of contrast, a planar geometry device from the same manufacturer shows very little increase in V_T hysteresis for the same range of negative gate-bias values (see Fig. 8). For the planar device, the effect is small, and it begins to saturate around $V_{GS\,(low)}$ = –6 V. (It should be noted that the large sensitivity to NBO in trench devices as shown in Fig. 7 is the same for both major manufacturers evaluated, even though the significant degradation due to AC-stress—under NBO conditions [see Fig. 5]— was true for only one of the two manufacturers. [1])

Figs. 9 and 10 provide additional insight into what is driving the large increase in V_T hysteresis in trench geometry devices (as shown in Fig. 7). Fig. 9 shows how the low side of the V_T hysteresis envelope [$V_{T(NEG)}$] moves significantly down in the negative direction with increasing negative gate bias during the V_T hysteresis stress [$V_{GS\,(low)}$]—again plotted versus the V_T hysteresis stress interval time (see Fig. 2). On the other hand, Fig. 10 shows that the high side of that same V_T hysteresis envelope [$V_{T(POS)}$] only moves slightly down in the negative direction with increasing negative gate bias during the V_T hysteresis stress. (Varying the positive gate bias during V_T hysteresis stress [$V_{GS\,(high)}$] is studied elsewhere [1].) Therefore, the large increase in the magnitude of the V_T hysteresis shown in Fig. 7 is due almost entirely to a negative drift in V_T on the low side of the V_T hysteresis envelope with increasing NBO.

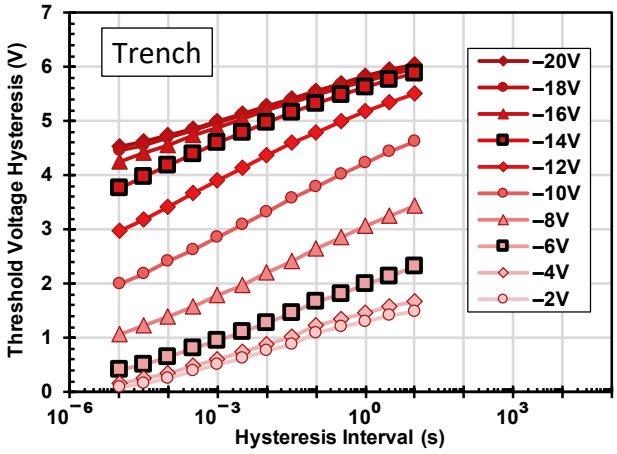

Fig. 7. Effect of negative gate bias, $V_{GS\,(low)}$, on the magnitude of V_T hysteresis observed (plotted as a function of the V_T hysteresis stress interval time) in a SiC MOSFET with a trench design. $V_{GS\,(high)}$ was kept constant at +22 V. (No AC stress was applied.)

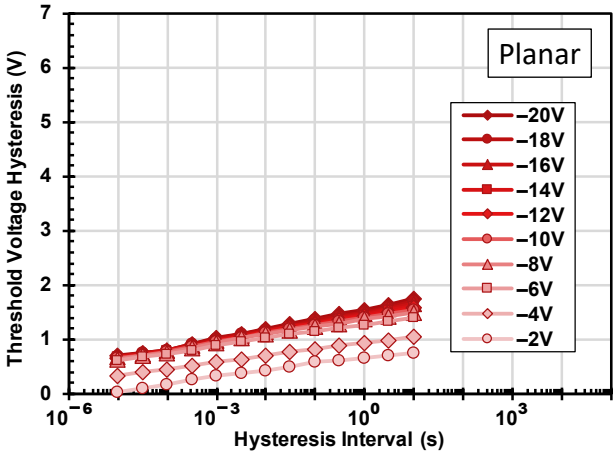

Fig. 8. Much smaller V_T Hysteresis effect due to a negative bias overstress is observed in a planar SiC DMOSFET. (No AC stress was applied.)

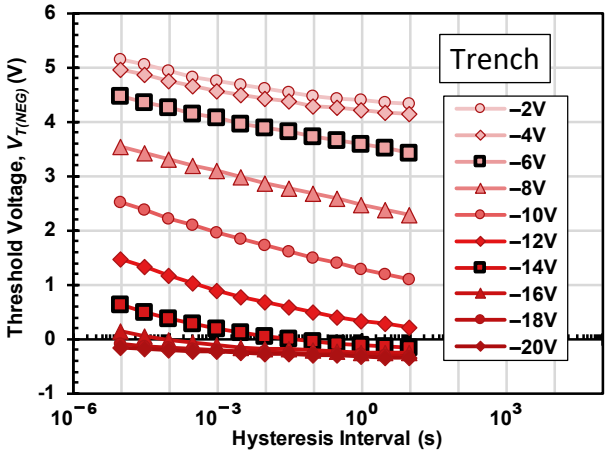

Fig. 9. The negative bias overstress of a trench SiC MOSFET results in a significant negative drift on the low side of the V_T hysteresis envelope [$V_{T(NEG)}$]. This effect saturates at a slightly negative threshold voltage. $V_{GS\,(high)}$ was kept constant at +22 V. (No AC stress was applied.)

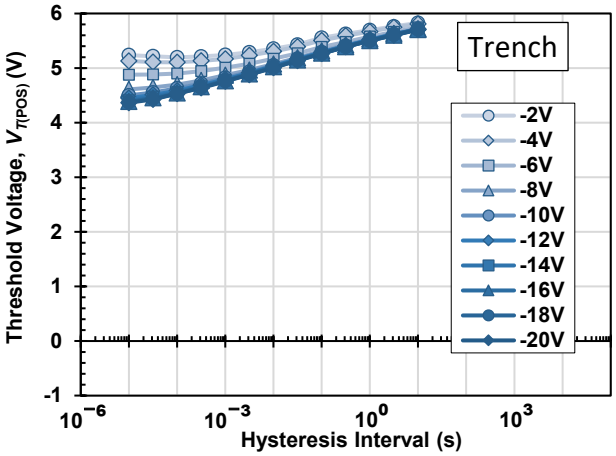

Fig. 10. The same negative bias overstress of a trench SiC MOSFET results in only a small negative drift on the high side of the V_T hysteresis envelope [$V_{T(POS)}$]. $V_{GS\,(high)}$ was kept constant at +22 V. (No AC stress was applied.)

This means that as V_T shifts positively due to AC-stress degradation effects, then $V_{GS} - V_T$ would decrease accordingly so that the effective gate-bias values applied during the V_T hysteresis measurement change. For example, before any positive V_T Shift, applying $V_{GS\,(low)} = -4$ V does not result in a NBO condition. But a 2-V positive shift in V_T would result in $V_{GS} - V_T$ changing such that $V_{GS\,(low)}$ effectively becomes −6 V instead, thus increasing the V_T hysteresis. This results in the value of $V_{T\,(NEG)}$ becoming 1 V less positive than it otherwise would have been. This explains why the V_T hysteresis widens in Fig. 1 as it shifts in the positive direction, and why the V_T shift occurs first, with the increase in V_T hysteresis only beginning to occur once V_T has shifted by at least 1 V first [1]. Therefore, no suggestion of additional trap activation is needed to explain the increase in V_T hysteresis caused by the AC stress in trench devices.

Summary and Conclusion

When exposed to a bipolar AC stress with a negative-bias overstress (a gate bias exceeding the manufacturer's recommended maximum negative gate operating voltage, −4 V in the particular case of interest), trench devices from a particular manufacturer experience a large positive V_T shift of close to 10 V—after about 10^{13} total cycles—without any indication of saturating, whereas planar devices from that same manufacturer (and all devices from other manufacturers) show a much smaller effect [1]. The large, corresponding increase observed in V_T hysteresis is due, not to the activation of new traps but to the increase in V_{GS}–V_T on the negative-bias side of a standard V_T hysteresis measurement (which was not observed in the planar device). Generally, SiC trench MOSFETs show a sensitivity in V_T hysteresis to NBO [2], but this phenomenon alone is not sufficient to cause AC-stress-induced shift. The degradation mechanism, likely due to electron trapping in deep states [1], results in a seemingly-permanent positive shift in V_T. However, this damage can be annealed away with the application of a negative bias at high temperature (300 °C) [1].

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