Materials Science Forum
ISSN: 1662-9752, Vol. 1092, pp 157-164
doi:10.4028/p-gv3hl2

Submitted: 2022-09-04
Revised: 2022-11-02
Accepted: 2022-11-25
Online: 2023-06-06

Power Cycling on Lateral GaN and β-Ga2O3 Transistors

Sarah Rugen[1,a*], Alexander Brunko[1,b], Felix Hoffmann[1,c] and Nando Kaminski[1,d]

[1]University of Bremen, Institute for Electrical Drives, Power Electronics and Devices (IALB), Otto-Hahn-Allee 1, 28359 Bremen, Germany

[a]sarah.rugen@uni-bremen.de, [b]a.brunko@uni-bremen.de, [c]felix.hoffmann@uni-bremen.de, [d]nando.kaminski@uni-bremen.de

Keywords: Power Cycling, PCT, temperature sensitive parameter, TSEP, Ga2O3 MOSFET, GaN GIT, Reliability

Abstract. The load cycling capability of novel power semiconductors is an important aspect when estimating their lifetime in field service. The Power Cycling Test (PCT) is the standard test to evaluate the lifetime of a semiconductor device under thermo-mechanical stress. PCTs are typically performed at temperature swings (ΔT) much higher than common operating conditions, to obtain results within a reasonable time. In this work, the PCT capability of gallium nitride (GaN) and gallium oxide (Ga2O3) lateral transistors is investigated. The GaN devices were tested in two groups with different ΔT. The temperature of the devices was monitored using two different temperature sensitive electrical parameters (TSEPs) and the accuracy of both methods was evaluated by comparing the results with the temperature, monitored by using an infrared (IR) camera. For Ga2O3 devices, no data on potential TSEP exists so far, thus, the typical TSEP for silicon (Si), silicon carbide (SiC) and GaN were investigated for their applicability to Ga2O3 devices. While a PCT was conducted on the devices, the temperature was also monitored using an IR camera. The results of the comparison of TSEP and IR camera data showed, that the accuracy of the TSEP for GaN matched either the temperature of the hottest spot on the chip (V_{DS} method), or the average chip temperature (V_{GS} method). For the Ga2O3 devices no suitable TSEP could be obtained and only the IR camera was used for the temperature measurement. It revealed a very uneven temperature and thus, current distribution on the chip. Furthermore, both GaN and Ga2O3 devices exhibit an outstanding power cycling capability with no failure after completing several millions of cycles. Considering the difference in Young's Modulus of Si, GaN and Ga2O3, the PCT performance of GaN on silicon devices and Ga2O3 devices should be inferior to silicon devices. Thus, both device types, the GaN transistors and the Ga2O3 transistors, showed a PCT capability much higher than expected.

Introduction

During their lifetime, semiconductor devices are exposed to frequent temperature cycles. These cycles lead to thermo-mechanical stress at the interfaces of the different materials or inside the materials. This stress can result in die-attach degradation or bond wire fatigue, which leads to an increase in thermal or electrical resistance. Such failures are investigated by power cycling tests (PCT). For novel semiconductor devices based on gallium, such as gallium nitride (GaN) and gallium oxide (β-Ga_2O_3), the PCT performance should be inferior to silicon (Si) devices, based on the Young's Modulus (Si: $E_{Y,Si}$ = 130-190 GPa [1], GaN: $E_{Y,GaN}$ = 210-405 GPa [2], β-Ga_2O_3: $E_{Y,Ga2O3}$ = 245-261 GPa [3]). However, while there are no publications for PCTs on Ga_2O_3 devices yet, recent publication for GaN devices showed, that they are outperforming silicon devices by orders of magnitude [4]. The root cause of this discrepancy was investigated in this work.

The temperature swing ΔT is the main acceleration factor during the PCT and hence, an accurate and reliable measurement of ΔT is essential to be able to use lifetime models to predict the behaviour of the devices under normal conditions and predict the service life of devices. Therefore, applying a suitable temperature sensitive electrical parameter (TSEP) is crucial to provide a precise junction temperature estimation. Several parameters were investigated as possible TSEPs for SiC devices,

including the voltage drop of the body diode V_{SD}, the on-state resistance $R_{DS,on}$ and the threshold voltage V_{th} [5]. For GaN devices, the drain-source voltage V_{DS} and the gate-source voltage V_{GS} were investigated so far [4]. In this work, the TSEPs V_{DS} and V_{GS} are evaluated for GaN devices, while for the Ga_2O_3 device V_{DS} and V_{th} are investigated as possible TSEPs. Furthermore, the PCT capability of the tested devices is evaluated.

Devices Under Test and Test Setup

As devices under test (DUTs), commercially available discrete GaN Gate Injection Transistors (GIT) and research level chips of β-Ga_2O_3 normally-on MOSFETs on test substrates from Ferdinand-Braun-Institut, Berlin [6], were used. Both device types are lateral devices with gold bond wires, bonded on the edges of the chips.

The Ga_2O_3 chip features 7 normally-on MOSFETs on a substrate. The devices were fabricated on n-doped β-Ga_2O_3 homoepitaxially grown on semi insulating β-Ga_2O_3(100) substrates. More details about these devices can be found in [6] [7] [8].

PCT on GaN

For all PCT tests conducted on the GaN devices, the DUTs were kept in on state over the course of the tests with continuous gate current (I_{GSmeas}). Furthermore, the drain measurement current (I_{DSmeas}) was applied continuously. The switching of the drain load current (I_{load}) and thus the controlling of the heating (t_{on}) and cooling (t_{off}) phase was done by using auxiliary switches

Two PCTs with 4 GaN-GIT each were performed with slightly different parameters. The temperature swing of ΔT was determined in each run using the TSEPs V_{DS} and V_{GS}. The first run was performed with T_{min} = 20°C and ΔT = 60 K, t_{on} = 0.5 s, t_{off} = 1 s, I_{GSmeas} = 18 mA, I_{DSmeas} = 500 mA and I_{load} = 20.9 A. After more than 4.6 Mcyc without any visible degradation of the components, the test was terminated.

For the preparation of the second run, a set of fresh DUTs was parameterised at I_{DSmeas} = 500 mA and a maximum allowed gate current of I_{GSmeas} = 20 mA to achieve the maximum possible ΔT swing. Unfortunately, the DUTs become thermally unstable at very small current increases of the load current, although the water-cooled heat sink is operating at a controlled cooling temperature of 20°C. Figure 1 shows V_{DSon} curves at the end of the on-phase at load current between 25.7 A and 26.8 A. To avoid thermal runway and thus an early destruction of the device, the load current was limited to 25.7 A during the second test run.

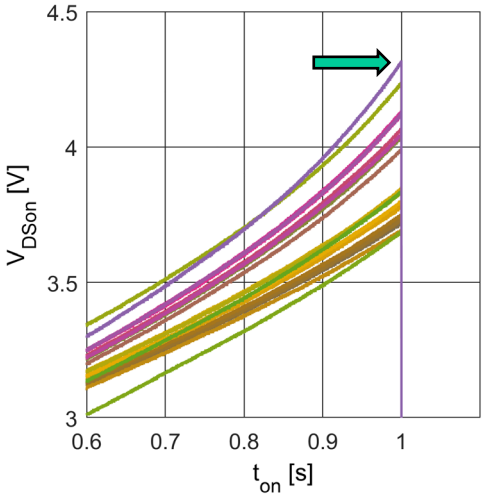

Figure 1: V_{DSon} curves at the end of the on-phase at different load currents. DUTs get thermally unstable (green arrow) at very small increases of the load current (25.7 A – 26.8 A).

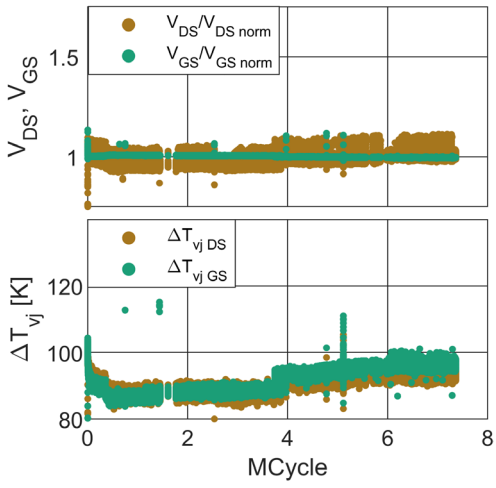

Figure 2: Normalised characteristics of $V_{DS/GS}$, R_{th}, and ΔT_{vj} of DUT#1 tested at ΔT_{vj} = 95 K.

The second run with T_{min} = 20°C, ΔT = 95 K, t_{on} = 0.5 s, t_{off} = 1 s, $I_{GS,meas}$ =20 mA, I_{DSmeas} = 500 mA and I_{load} = 25.7 A was terminated after more than 7.3 Mcyc without any visible degradation of the DUTs. Normalised characteristics of $V_{DS/GS}$, and ΔT_{vj} of DUT#1 are shown in Figure 2. The curves are normalised to their initial mean values obtained between 20 kcyc and 50 kcyc. Over the course of the test, a marginal increase of the ΔT_{vj} was observed. Additionally, a ΔT_{vj} offset was visible upon resumption of the test after interruptions at 0.6 Mcyc and 3.6 Mcyc.

Temperature Sensitive Parameter for GaN

In addition to the V_{DS} as TSEP, the V_{GS} (diode) [9] [10] can be used as TSEP for the GaN-GIT. A direct comparison of the V_{DS} and V_{GS} methods using the calibration curves showed that the spread of the V_{GS} curves among the DUTs was larger compared to the V_{DS} curves (Figure 3). This is clearly shown by the offset-compensated zoom part in Figure 3 in the range of 145°C and 155°C degrees of T_{vj}. The V_{GS} TSEP offers a better resolution of − 2.6 mV/K vs 0.2 mV/K with the V_{DS} TSEP.

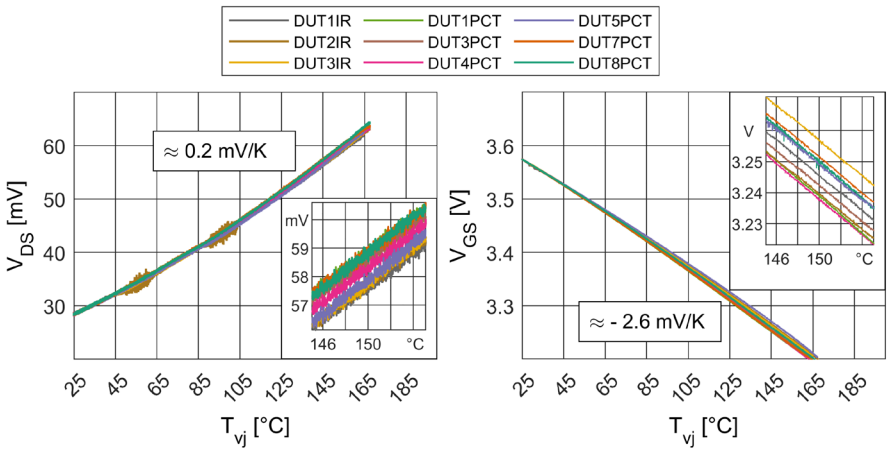

Figure 3: Calibration curves for TSEP of the PC-tested DUTs and the DUTs decapsulated for temperature determination by the IR camera.

After two test runs without failures, three fresh DUTs (DUT1IR, DUT2IR and DUT3IR, Figure 3) were calibrated and prepared for TSEP validation via an IR camera. The DUTs were decapsulated down to the chip surface and then the chip surface was coated with a thermographic paint (Lab IR Paint, HERP-HAT-MWIR-BK-11) to achieve a constant emissivity. In order to investigate the repeatability, multiple measurements with the same test conditions were performed. At first, measurement series I was conducted at the same conditions as in the second PCT test run with I_{GSmeas} = 20 mA, I_{DSmeas} = 500mA and I_{load} = 25.7 A resulting in $T_{vj,max}$ = 139°C. Furthermore, measurements at higher $T_{vj,max}$ (≈ 154°C, series II and ≈ 167°C, series III, all temperature values of the V_{GS} measurement) were performed.

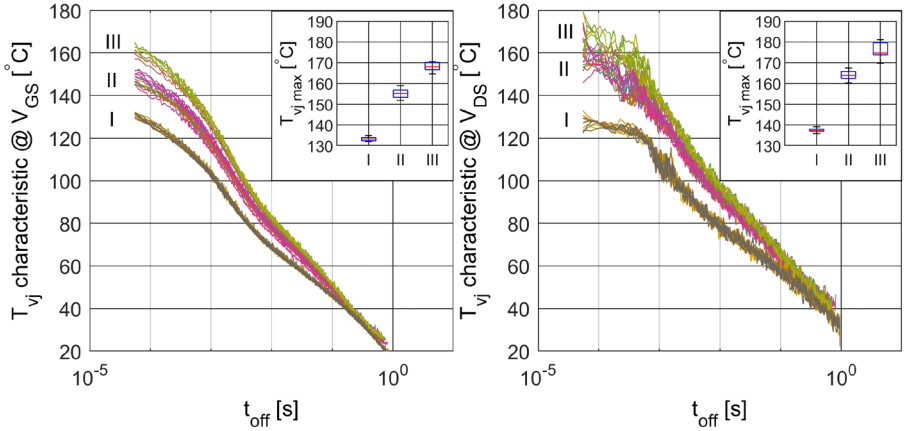

Figure 4: Comparison of the two methods for T_{vj} determination using V_{GS} or V_{DS} as TSEP at three different temperatures

The measurements via TSEP, shown in Figure 4, confirm that the V_{GS} method features a smaller noise level than the V_{DS} method, due to the better resolution. The associated box plots are shown as insets in Figure 4. The temperature values in the box plot are extrapolated to the maximum temperature at turn-off, since the temperature estimation with TSEPs starts with a delay of 30 µs after turn off. The box plots suggest, that the V_{GS} method also provide a more stable temperature estimation. On the other hand, the variation among the DUTs is much higher for the V_{GS} method due to the variance in V_{th} (see Figure 3) and hence, the V_{GS} calibration has to be performed for each DUT individually.

Another important property is the accuracy of the TSEP. Figure 5 shows a validation of T_{vj} using the IR camera. The top-left image shows a typical decapsulated device without the thermographic paint. The two bottom graphs show the thermographic image at the maximum temperature during a single power cycle. Furthermore, the temperature distribution of the chip, the respective temperature profiles of the areas of interest and the associated transient curves (right graph) are shown.

Table 1: Temperatures TSEP vs IR

		Temperature [°C]		
		Test I	Test II	Test III
TSEP	V_{GS}	131.7	154.6	166.5
	V_{DS}	132.2	165.5	173.0
IR	spot	138.2	161.2	172.0
	rectangle	136.2	154.3	163.7
	diagonal	133.7	151.7	161.3
	bondline D	118.4	143.3	144.7
	bondline S	111.3	130.0	133.7

The camera data revealed, that the temperature swing ΔT measured by the V_{DS} method corresponds well with the highest temperature of the chip, which is a spot on the active area. The V_{GS} method matches the average temperature of the active area (see Table I). However, since the chip is bonded on the edge and not on the chip's active area, the ΔT at the possible point of failures, i.e. bond feet, was significantly lower (by around 30 K) than the temperature estimated by the TSEP. This can at least partially explain the significantly better PCT performance.

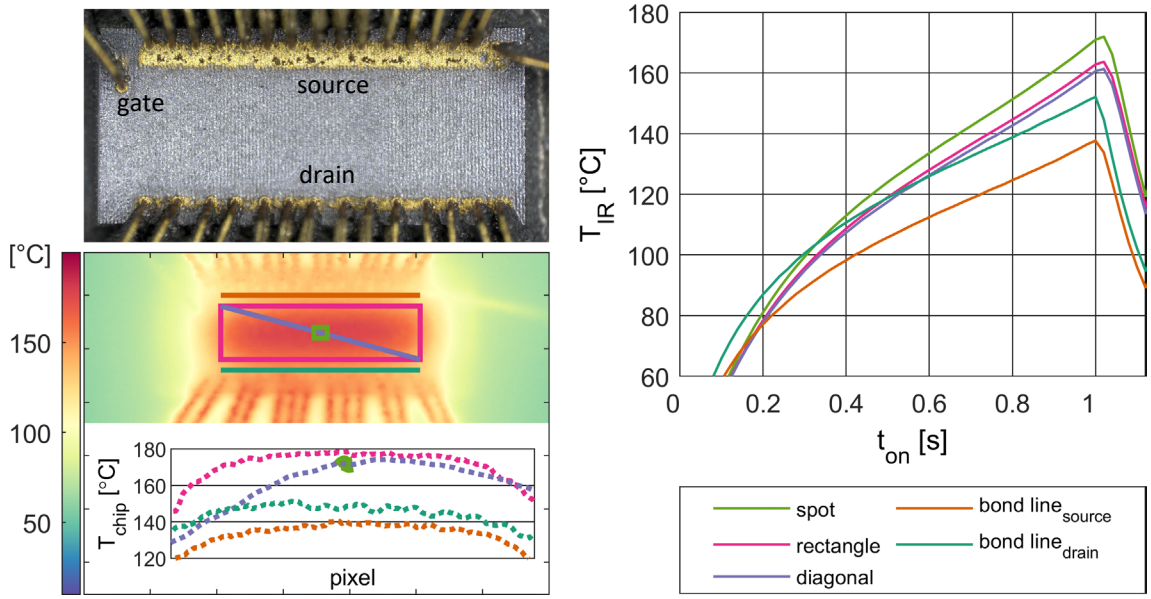

Figure 5: Thermographic validation of T_{vj} with the IR camera of the decapsulated DUT in a single active power cycle

Temperature Sensitive Parameter for Ga_2O_3

In preparation of the PCT on the Ga_2O_3 chip, measurements were carried out to find a suitable temperature sensitive parameter to determine the (junction) temperature of the chip. Since V_{DS}, V_{GS} and V_{th} are frequently used TSEPs for other device topologies and materials, those methods were considered and investigated regarding their applicability for Ga_2O_3.

For this purpose, the quasi-static output characteristics were measured for different temperatures between 23°C and 120°C (105°C for threshold voltage measurements) and gate voltages V_{GS} between -20 V and -10 V. (see Figure 6 for the temperature dependence of the I_D-V_{DS} curve for a gate voltage of V_{GS} = -14 V and Figure 7 for the temperature dependence of the threshold voltage measurement).

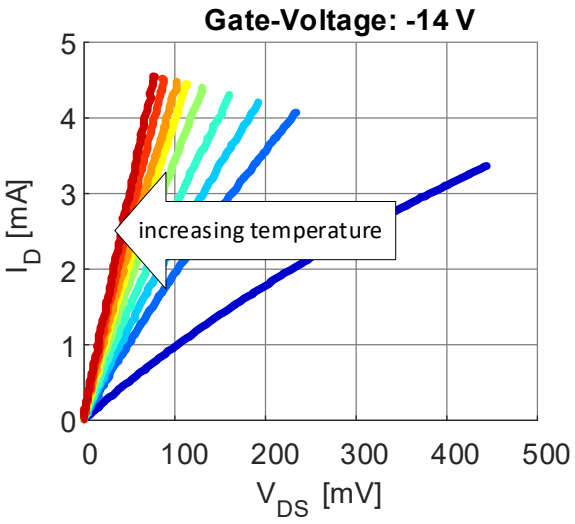

Figure 6: Forward and reverse characteristics of the Ga_2O_3 transistor for a gate voltage of V_{GS} = - 14 V and temperatures between 23°C and 120°C

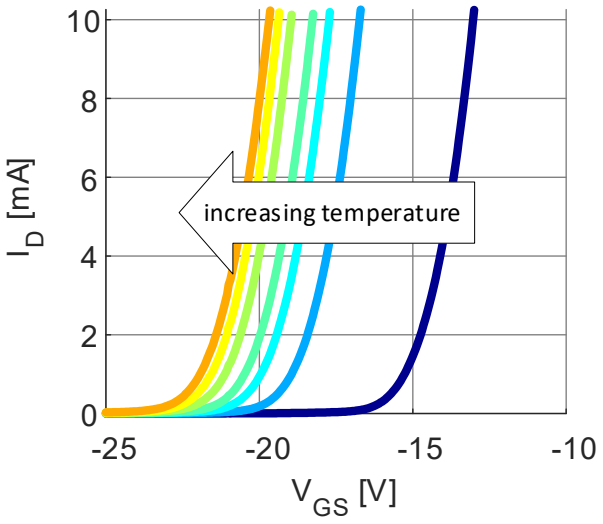

Figure 7: Transfer characteristics at different temperatures (between 23 and 105°C) for a drain-source voltage of V_{DS} = 0.5 V

As depicted in the curve in Figure 8, the temperature dependence of the drain current I_D for a fixed drain source voltage exhibited a linear behaviour. The temperature dependence of V_{th}, on the other hand, showed a non-linear behaviour (Figure 9).

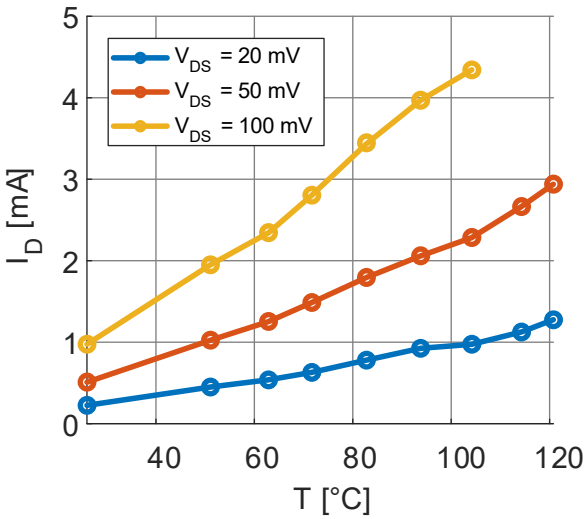

Figure 8: Drain current I_D for a gate voltage of V_{GS} = - 14 V at different drain-source voltages V_{DS}

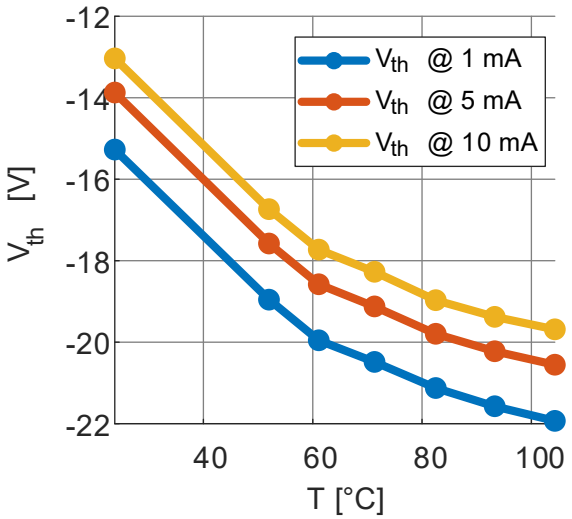

Figure 9: Threshold voltage V_{th} for different drain currents.

To investigate the stability of the measurement methods, which is required for the usage of the parameter as TSEP, all measurements were carried out twice.

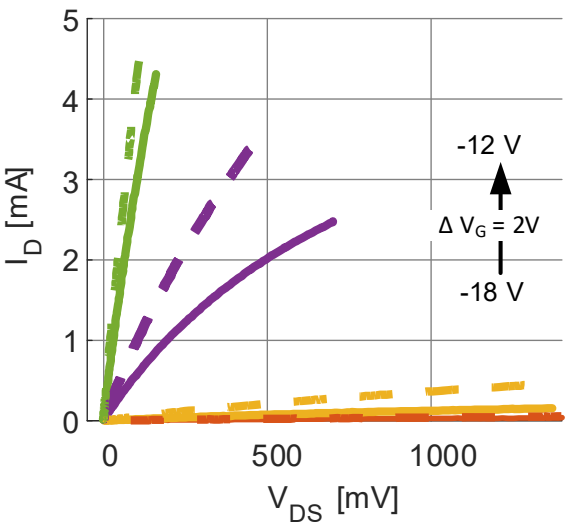

Figure 10: Comparison of measurement 1 (solid line) and measurement 2 (dotted line) for the output characteristics at room temperature for different gate voltages

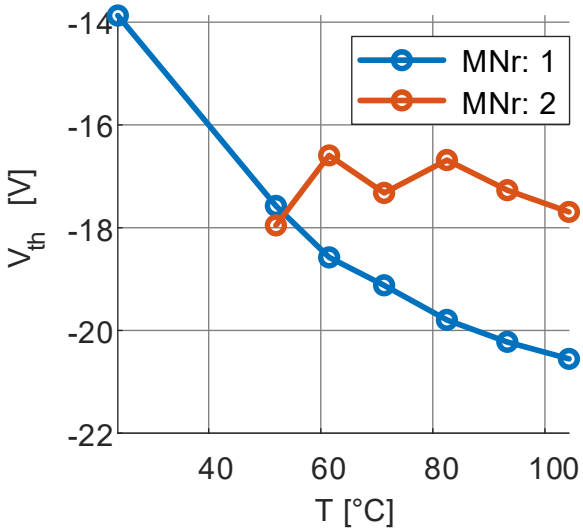

Figure 11: Comparison of the temperature dependence of V_{th} for measurement 1 (blue line) and measurement 2 (orange line)

The comparison of the first and the second measurements of the output characteristics as well as the threshold voltage revealed a highly "dynamic" behaviour (Figure 10 and Figure 11). There was a large drift in the threshold voltage, which also showed a strong nonlinear behaviour. The shift in threshold voltage was observed in lateral Ga_2O_3 in several publications [7] [8] [11] and was found to be due to charge trapping taking place in oxide border traps [11]. Due to this unstable behaviour, none of the investigated TSEPs were suitable to provide a stable and accurate temperature estimation and hence, the temperature during the power cycling test was measured exclusively by thermography.

PCT on Ga_2O_3

One PCT on a β-Ga_2O_3 transistor was performed with T_{min} = 14°C, ΔT = 64 K, and I_{load} = 0.46 A. The on-time was t_{on} = 3 s and the off-time was t_{off} = 6 s. The Ga_2O_3 chip was mounted on a water-cooled heat sink to provide a stable cooling temperature and to avoid thermal runaway. This was necessary, as the Ga_2O_3 sample showed a similar thermally unstable behaviour at very small current increases as observed in the tested GaN devices, which limited the achievable temperature swing.

The sample was coated with the thermographic paint, also used for the GaN test, to provide a homogenous emissivity and allow accurate temperature readings by thermography. The test was carried out at a gate voltage of V_{GS} = 0V and the load current was controlled using auxiliary switches. The test is still ongoing and has already completed more than 2.2 Mcyc without failure.

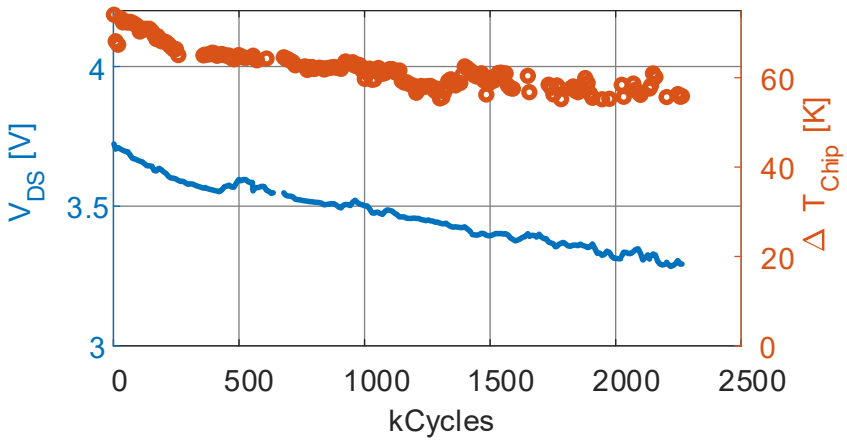

Figure 12: Number of cycles in the PCT vs. measured V_{DS} and average ΔT of the chip (measured with an IR camera)

Figure 12 shows the V_{DS} (mean value) and chip temperature readings of the power cycling test. It is visible that both, V_{DS} and ΔT exhibit a decrease over the course of the PCT, likely caused by a shift of the electrical characteristics of the chip, which were observed to be instable (see Figure 10).

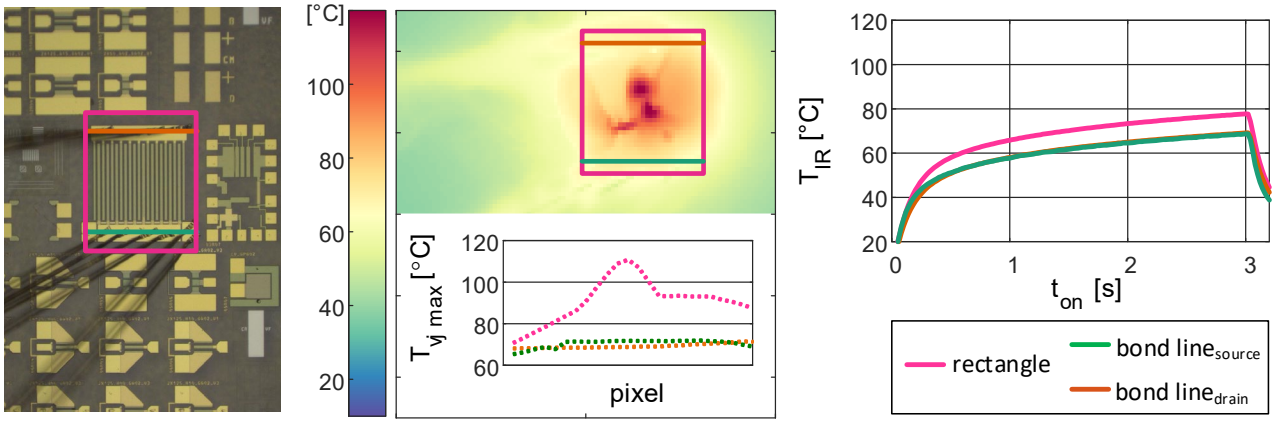

Figure 13: *Left*: picture of the Ga_2O_3 chip. *Centre*: thermographic measurement at the maximum temperature of the active power cycle and the respective profiles of the areas of interests (pink lines: average temperature of active area in the pink box, green and orange lines: temperature of the bond feet. *Right*: transient curves of the different areas of interests on the active chip area and on the bond feet during the heat phase of PCT. The maximum temperature is measured in the centre of the active area of the chip.

Figure 13 depicts the temperature measurement of the Ga_2O_3 PCT. The measurement illustrates, that the temperature of the bond wires (green and orange lines) was about 10 K lower than the average temperature of the chip (pink box and lines in graph) and significantly lower (by about 40 K) than the hottest spot on the chip's active area. This observation is similar to the measurements carried out on the GaN devices.

Summary and Conclusion

In this work, the PCT capability and possible TSEPs for GaN and Ga_2O_3 devices were investigated. Both GaN-GIT and Ga_2O_3 MOSFETs were lateral devices with gold bonds outside of the chip's active area. The results show, that for GaN, suitable TSEPs with a stable temperature estimation could be determined, while for the Ga_2O_3 devices, all investigated TSEPs are inapplicable, due to their instabilities.

Furthermore, the temperature measurements for the GaN devices show that the junction temperature estimation by V_{DS} as TSEP corresponds well to the hottest spot on the chip, whereas the temperature on the possible point of failure, the bond feet, is severely overestimated (by around 30 K). This is a result of the lateral topology of the device and hence, the temperature swing at the bond feet of the Ga_2O_3 devices is also significantly lower than the average chip temperature. Due to their unstable behaviour, the GaN and Ga_2O_3 devices showed thermal runaway already at very small current increases, which limited the achievable maximum temperature swing for both devices.

In the PCT, the GaN devices passed 4.6 and 7.3 Mcyc, respectively, and the Ga_2O_3 devices passed 2.2 Mcyc without any sign of degradation. These values are at least an order of magnitude higher than expected (ca. 100 kcyc based on silicon parameters) and cannot be explained by thermo-mechanical properties alone. In fact, the temperature estimation based on both, V_{DS} and V_{GS}, delivers a junction temperature with a strong emphasis on high temperature regions (for the GaN devices). As a result of the thermal runaway, all tests were performed at comparatively low junction temperature swings and hence, even lower temperature swings at the possible point of failures. In combination with the difference in bonding technology this can explain at least partially the much better power cycling performance of lateral GaN and Ga_2O_3 devices compared to silicon.

However, since the measured ΔT_{vj} is not a good predictor for ΔT_{PoF}, neither the established lifetime models can be applied, nor the better power cycling performance translates necessarily into a longer service life. Additionally, the die attach has not limited the devices' lifetime in these tests, thus power

cycling seems not to be lifetime limiting for this kind of devices. However, this might change with more aggressive designs, in particular when bonding on the active area to minimise the chip size and requires continuous verification.

Acknowledgement

The authors would like to thank the members of the ForMikro GoNext project, Kornelius Tetzner, Oliver Hilt and Joachim Würfl (all Ferdinand-Braun-Institut, FBH, Berlin) as well as Andreas Popp (Leibniz-Institut für Kristallzüchtung, IKZ, Berlin), for providing the Ga_2O_3 sample. The work was funded by the BMBF under grant number 16ES1084K.

References

[1] M. A. Hopcroft, W. D. Nix and T. W. Kenny, “What is the Young's Modulus of Silicon?”, *Journal of Microelectromechanical Systems,* vol. 19, pp. 229-238, April 2010

[2] M. Rais-Zadeh, V. J. Gokhale, A. Ansari, M. Faucher, D. Théron, Y. Cordier and L. Buchaillot, “Gallium Nitride as an Electromechanical Material”, *Journal of Microelectromechanical Systems,* vol. 23, pp. 1252-1271, December 2014.

[3] X.-Q. Zheng, H. Zhao, Z. Jia, X. Tao and P. X.-L. Feng, “Young's modulus and corresponding orientation in β-Ga2O3 thin films resolved by nanomechanical resonators”, *Applied Physics Letters,* vol. 119, p. 013505, July 2021

[4] M. Goller, J. Franke, J. Lutz and T. Basler, “Power Cycling Results of Discrete Gallium Nitride Gate Injection Transistors,” in *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, 2021.

[5] C. Herold, J. Sun, P. Seidel, L. Tinschert and J. Lutz, “Power cycling methods for SiC MOSFETs,” in *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, 2017, pp. 367-370.

[6] J. Böcker, K. Tetzner, S. Heucke, O. Hilt, E. Bahat-Treidel, S. Dieckerhoff and J. Wuerfl, “Dispersion effects in on-state resistance of lateral Ga2O3 MOSFETs at 300 V switching,” *Electronics Letters,* vol. 56, p. 838, May 2020.

[7] K. Tetzner, E. Bahat Treidel, O. Hilt, A. Popp, S. Bin Anooz, G. Wagner, A. Thies, K. Ickert, H. Gargouri and J. Würfl, “Lateral 1.8 kV β-Ga2O3 MOSFET With 155 MW/cm2 Power Figure of Merit,” *IEEE Electron Device Letters,* vol. 40, pp. 1503-1506, September 2019.

[8] K. Tetzner, O. Hilt, A. Popp, S. B. Anooz and J. Würfl, “Challenges to overcome breakdown limitations in lateral β-Ga2O3 MOSFET devices,” *Microelectronics Reliability,* vol. 114, p. 113951, November 2020.

[9] C. Herold, J. Franke, R. Bhojani, A. Schleicher and J. Lutz, “Methods for virtual junction temperature measurement respecting internal semiconductor processes,” in *2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2015, pp. 325-328.

[10] J. Franke, G. Zeng, T. Winkler and J. Lutz, “Power cycling reliability results of GaN HEMT devices,” in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2018, pp. 467-470.

[11] M. Fregolent, E. Brusaterra, C. D. Santi, K. Tetzner, J. Würfl, G. Meneghesso, E. Zanoni and M. Meneghini, “Conduction properties and threshold voltage instability in β-Ga2O3 MOSFETs,” in *Oxide-based Materials and Devices XIII*, 2022.