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Temperature Dependence of the Channel and Drift resistance of SiC Power MOSFETs Extracted from I-V and C-V Measurements

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Abstract. SiC power MOSFETs show very promising electrical performance for efficient and reliable high temperature operation. This work presents a novel approach for the determination of the temperature dependence of SiC power MOSFET's channel and drift resistance components in the on-state, which are extracted based on current-voltage (I-V) and capacitance-voltage (C-V) measurements without the need of data extrapolation. The results show that the channel resistance has weak, whereas the drift resistance has strong temperature dependence.

Introduction

Characterization of SiC power MOSFETs at different temperatures is highly important for both device and system engineers to fully benefit from SiC material properties, and to better understand and model the device characteristics at elevated operation temperatures [1, 2]. The resistance between the drain-source terminals (R_{ds}) of a MOSFET is a strongly temperature dependent parameter. R_{ds} (of planar gate or trench power MOSFETs) can be divided into the channel resistance (R_{ch}) of the inversion layer at the oxide/SiC interface, and the sum of the JFET, epi-layer, and n^+ substrate resistances, which is denoted as R_{drift}, $R_{ds}=R_{ch}+R_{drift}$, see equivalent circuit 3c). The (small) contact resistances of the source and drain terminals are included in R_{ch} and R_{drift}, respectively, and are negligible in power MOSFETs. The value of R_{ch} is controlled by V_{gs} and significantly reduces when the device is turned on by increasing V_{gs} above the threshold voltage (V_{th}). By contrast, R_{drift} has only a small dependence on V_{gs} in the JFET region for $V_{gs} > 0$V. Both R_{ch} and R_{drift} depend on the applied drain-source bias (V_{ds}).

Several methods have been proposed to extract the source (R_s) and the drain (R_d) residual resistance components, $R_s+R_d=R_{res}$ (R_s and R_d do not depend on V_{gs}), of lateral MOSFETs e.g., in [3-6]. In [3, 4] R_{res} is extrapolated at the intercept of R_{ds} versus $(V_{gs}-V_{th})^{-1}$. In addition, it was assumed that $R_{drift}(V_{ds}, V_{gs}) \approx R_{drift}(V_{ds}) \approx R_{res}(\text{const})$ for $V_{gs} \sim 20V \gg V_{th}$. This extrapolation method was applied to SiC power MOSFETs in [7, 8]. A similar method was developed for GaN FinFETs and validated by Technology Computer-Aided Design (TCAD) simulations in [9]. In [10] the components of the drain-source resistance were evaluated by means of TCAD simulations for SiC power MOSFETs of different nominal V_{ds}.

In this paper we show a fast and simple technique for reliably extracting the components of the on-state resistance at different temperatures. The new method proposed in this work for estimating/extracting R_{ch}, R_{drift} is based on the measurement of the inter-terminal capacitances between gate-source (C_{gs}/C_{sg}) and gate-drain (C_{gd}/C_{dg}) in the on-state, the estimation of the overlap capacitance (C_{ov}) between the gate-source terminals, and the measurement of the drain-source resistance R_{ds} [11]. In the following the extrapolation and the new C-V based method are explained and compared by the extraction of R_{ch} and R_{drift} for three different types of SiC power MOSFETs.

Extrapolation Method The current-voltage characteristic of a power MOSFET can be expressed in the linear mode of operation for low V_{ds} using the gradual channel approximation as

$$I_d = k[V_{gs} - V_{th} - 0.5(V_{ds} - I_d R_{drift})](V_{ds} - I_d R_{drift}), \quad (1)$$

where $k = W_{eff}\mu_{eff}C_{ox}/L_{eff}$ (W_{eff} the effective channel width, μ_{eff} the effective channel mobility (assumed independent of V_{gs}), C_{ox} the gate oxide capacitance per unit area, and L_{eff} the effective channel length) [12]. Assuming $V_{gs} - V_{th} >> 0.5(V_{ds} - I_d R_{drift})$ and using the relation $R_{ds} = V_{ds}/I_d$, (1) can be transformed into

$$R_{ds} = \frac{1}{k(V_{gs} - V_{th})} + R_{drift}. \quad (2)$$

From (2) R_{drift} can be determined at the vertical intercept of extrapolated R_{ds} versus $(V_{gs} - V_{th})^{-1}$ (at maximum bias V_{gs} = 20V), see Fig. 2b). R_{ds} is derived from the I_d-V_{gs} characteristic shown in Fig. 1a) and 1b). The values of V_{th} are obtained from the I_d-V_{gs} characteristic by linear extrapolation of I_d at the V_{gs} values of maximum transconductance $g_{m,max}$, as depicted in Fig. 2a).

New C-V based Extraction Method The new extraction methodology for R_{ch} and R_{drift} is based on their dependence with the MOSFETs inter-terminal capacitances C_{gs}/C_{sg} and C_{gd}/C_{dg} in the on-state [11, 13]. The capacitances $C_{ij} = -\partial q_i/\partial v_i$ are defined based on the change of the small-signal charge q and voltage v at the device terminals i,j ∈ {g, d, s} [11]. These capacitance characteristics must be measured at lower frequency i.e., some ten kHz (~ 30kHz) as shown in Figs. 3a) and 3b), to limit the influence of the terminal series impedances Z_g, Z_d, and Z_s [11]. By solving the power MOSFET simplified lumped electrical equivalent circuit in the on-state, see Fig. 3c) [13], [14], using the conditions $|Z_d|$, $|Z_s| << R_{ch}$, R_{drift} and the relation $C_{gg} = C_{g'} + C_{ov}$, where C_{gg} is the total terminal gate capacitance, C_{ov} the overlap capacitance between the gate and source metallization in parallel to the capacitance between the gate and the n^+ source, and $C_{g'} = C_{g1} + C_{g2}$ is the oxide capacitance over the channel and JFET region, C_{dg} and C_{sg} can be extracted as

$$C_{dg} = \frac{C_{g'}R_{ch}}{R_{ch} + R_{drift}}, \quad (3)$$

$$C_{sg} = \frac{C_{g'}R_{drift}}{R_{ch} + R_{drift}} + C_{ov}. \quad (4)$$

The value of C_{ov} is approximated at the maximum depletion of the channel region when the value of C_{sg} becomes minimal, which leads to

$$C_{ov} \approx \min(C_{sg}). \quad (5)$$

By defining $C_{sg'} = C_{sg} - \min(C_{sg}) \approx C_{sg} - C_{ov}$ the ratio of $C_{dg}/C_{sg'}$ yields

$$\frac{C_{dg}}{C_{sg'}} \approx \frac{R_{ch}}{R_{drift}}. \quad (6)$$

Finally, based on (5) and (6) the relation between R_{ds}, R_{ch}, and R_{drift} can be derived as

$$\frac{C_{gg} - \min(C_{sg})}{R_{ds}} \approx \frac{C_{sg'}}{R_{drift}} \approx \frac{C_{dg}}{R_{ch}}. \quad (7)$$

Results

The new C-V and the extrapolation method were applied to extract R_{ch} and R_{drift} of three SiC power MOSFETs M1-M3 listed in Tab. 1. M1 and M2 have the same nominal $V_{ds,max}$ but different $R_{ds,on}$, while M3 has a higher nominal $V_{ds,max}$ than M1, M2. Both extraction methodologies are demonstrated for M1.

Tab. 1: Characteristics of the SiC power MOSFETs M1-M3 [15]

Manufacturer	Number	DUT	$V_{ds,max}$ [V]	$R_{ds,on}$ [mΩ]	active area (A) [mm^2]
Wolfspeed	C2M0080120D	M1	1200	80	6.45
Wolfspeed	C2M0025120D	M2	1200	25	19.04
Wolfspeed	C2M0045170D	M3	1700	45	21.92

The I_d-V_{gs} characteristics of M1-M3, as depicted for M1 in Fig 1 a), were measured with the Parametric Curve Tracer Keithley PCT-4B. The extrapolated values of $V_{th}(T)$, based on the I_d-V_{gs} characteristics as shown in Fig. 2, are listed in Tab. 2 and show a reduction of V_{th} with increasing temperature.

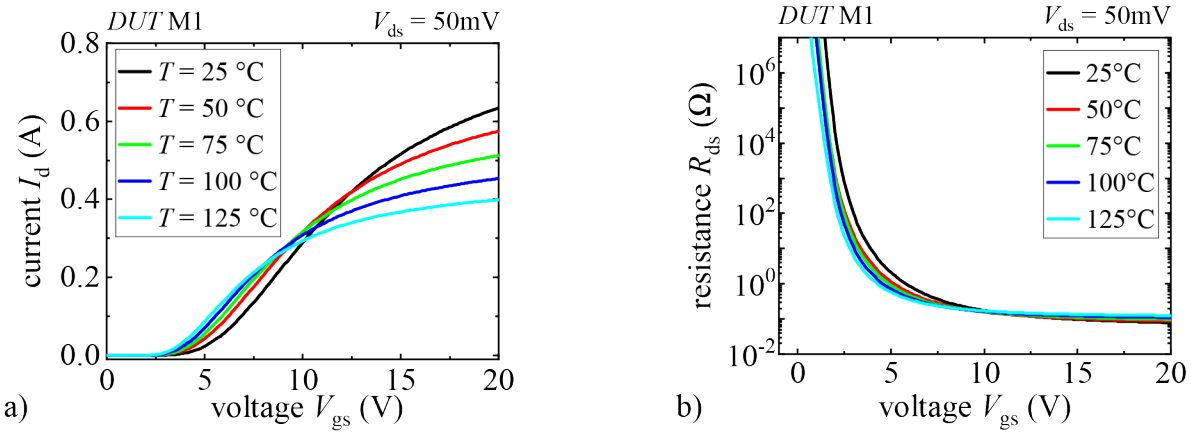

Fig. 1: Plot of a) the transfer characteristic I_d-V_{gs} of M1 at V_{ds} = 50mV measured for T = 25 °C, 50 °C, 75 °C, 100 °C, and 125 °C, and b) extracted drain-source resistance R_{ds} from a).

The C-V characteristics of C_{sg} and C_{dg} depicted for M1 in Figs. 3a) and 3b) were measured with the impedance analyzer Keysight E4990A and the test fixture Keithley 16047E. The MOSFET's terminals were connected to the high, low, and guard terminals [11], respectively. The values of C_{ov} were obtained from the C_{sg} characteristic according to (5). $C_{ov}(T)$ of M1-M3 vary less than 1% in the measured temperature range. The ratios of $C_{dg}/C_{sg'}(T)$ at V_{gs}=20 V, which were derived based on (7), are plotted in Fig. 4 and listed in Tab. 3.

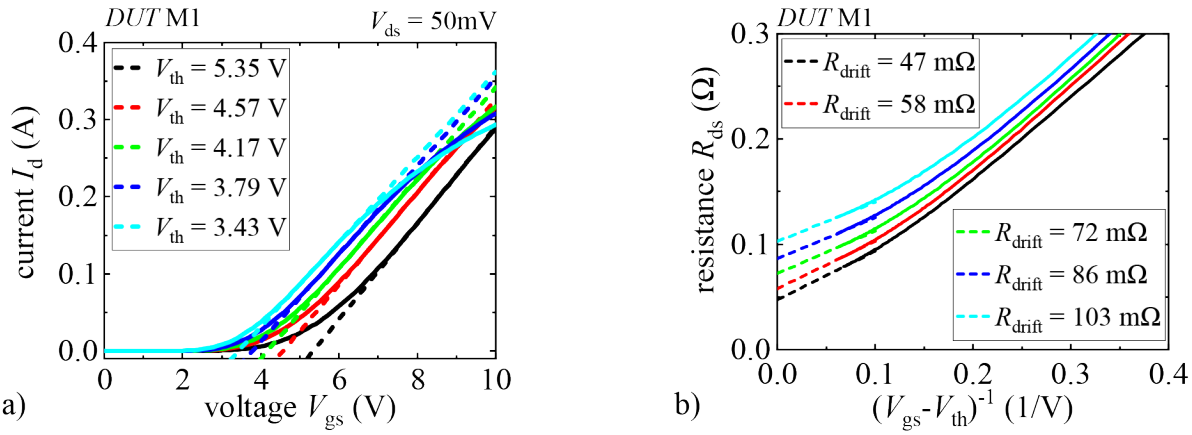

Fig. 2: a) V_{th} of M1 extracted at different temperatures from the I_d-V_{gs} characteristics shown in Fig. 1a). V_{th} is obtained at the intercept of the horizontal axis with the tangent of I_d-V_{gs} at the point of maximum transconductance $g_{m,max}$. b) Linear extrapolation of R_{ds} vs. $(V_{gs}$-$V_{th})^{-1}|_{V_{gs}\,=\,20V}$ of M1 at different temperatures to extract the drift resistance R_{drift} component (values listed) at the intercept of the vertical axis for T = 25 °C, 50 °C, 75 °C, 100 °C, and 125 °C.

Tab. 2: V_{th} values of the DUTs M1, M2, and M3 obtained by linear extrapolation from the measured I_d-V_{gs} characteristics, see Fig. 2a)

Temperature	M1	M2	M3
		V_{th}	
25°C	5.35 V	4.72 V	4.68 V
50°C	4.75 V	4.2 V	4.09 V
75°C	4.17 V	3.83 V	3.7 V
100°C	3.79 V	3.49 V	3.36 V
125°C	3.24 V	3.17 V	3.07 V

Tab 3.: Extracted $R_{ch}/R_{drift} = C_{dg}/C_{sg}$' values of the DUTs M1, M2, and M3 at V_{gs} = 20V, see Fig. 4

Temperature	M1	M2	M3
		R_{ch}/R_{drift}	
25°C	0.73	0.82	0.59
50°C	0.65	0.69	0.52
75°C	0.54	0.61	0.44
100°C	0.43	0.51	0.38
125°C	0.35	0.43	0.33

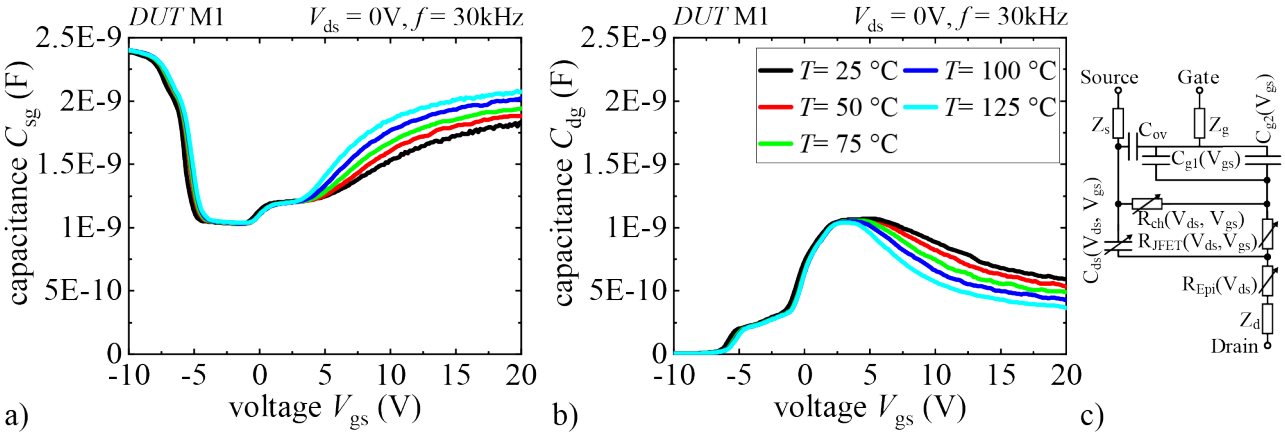

Fig. 3 Plot of a) the source-gate capacitance C_{sg} and b) the drain-gate capacitance C_{dg} as function of the gate-source voltage V_{gs} for V_{ds} = 0V measured at f = 30 kHz, T = 25 °C, 50 °C, 75 °C, 100 °C, 125 °C, and c) the MOSFET equivalent circuit in the on-state including the series impedances Z_g, Z_d, and Z_s.

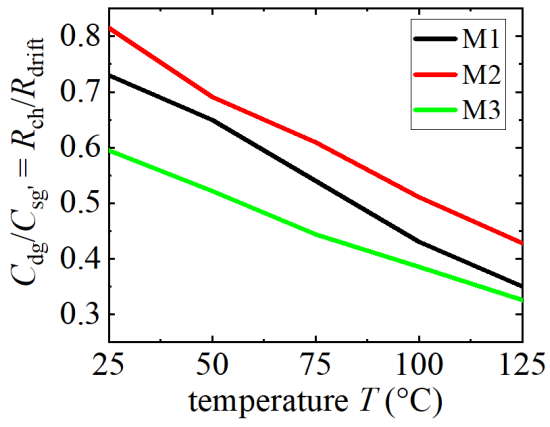

Fig. 4: Ratios C_{dg}/C_{sg}' = R_{ch}/R_{drift} for the DUTs extracted at V_{gs} = 20 V and T = 25 °C, 50 °C, 75 °C, 100 °C, and 125 °C.

Tab. 4: Values of the drift resistance R_{drift} extracted by the new C-V method based on C_{dg}/C_{sg}'and R_{ds}, the extrapolation method R_{ds} vs. $(V_{gs}$-$V_{th})^{-1}$, and their relative difference (R_{ds} vs. $(V_{gs}$-$V_{th})^{-1}$) / (C-V)

Temperature	R_{drift} of M1		
	C_{dg}/C_{sg}'	R_{ds} vs. $(V_{gs}V_{th})^{-1}$	Δ%
25°C	46 mΩ	47mΩ	3.8 %
50°C	53 mΩ	58 mΩ	9.8%
75°C	64 mΩ	72 mΩ	14%
100°C	77 mΩ	86 mΩ	12.1%
125°C	93 mΩ	103 mΩ	11.1%

The values of R_{ch} and R_{drift} extracted by the new C-V based method are depicted in Fig. 5a) and are scaled in Fig. 5b) by the MOSFET's active areas (A) listed in Tab. 1 [15]. As indicated by C_{dg}/C_{sg}'(T) ≈ R_{ch}/R_{drift}(T) in Tab. 3, the values of R_{drift}(T) increase with increasing temperature, whereas the values of R_{ch}(T) indicate almost no temperature variation. The increase of R_{drift}(T) is explained due to

increasing carrier scattering with increasing temperature. Yet, further investigations and comparison with other SiC power MOSFETs are necessary to understand the temperature independence of $R_{ch}(T)$. The accuracy of the new method is verified in Fig. 5b) by: 1) R_{ch*}A of M1-M3 have similar values, which can be expected due to a similar planar gate structure, and 2) a very close matching of R_{drift*}A from M1 and M2 with the same nominal V_{ds} as listed in Tab. 1. In comparison, R_{drift*}A of M3 is expected to be larger due to its higher nominal blocking voltage $V_{ds,max}$.
The comparison of the new C-V and the extrapolation methods is illustrated by the values of $R_{drift}(T)$ of M1 plotted in Figs. 2b), 5a) and listed in Tab. 4, which show a relative difference of up to 12.1%. Yet, a larger discrepancy of R_{drift} is observed for M2 and M3 with relative difference up to 27.1%. These differences might be introduced by the linear extrapolation, the approximation of $R_{drift} \approx R_{res}$, and/or the simplified equivalent circuit in Fig. 3c) of the MOSFETs distributed behavior.

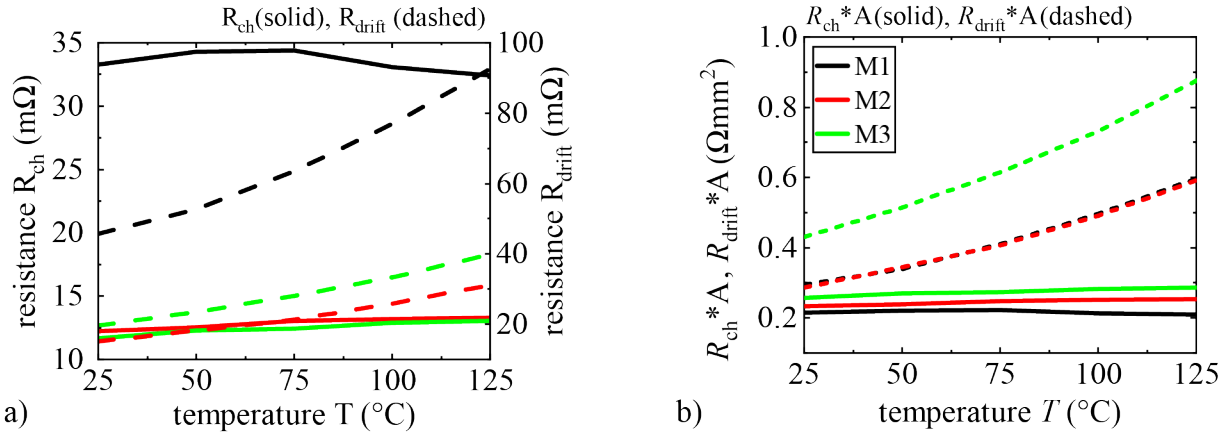

Fig. 5. Plot of a) the channel R_{ch} and drift R_{drift} resistances extracted based on the ratio of $R_{ch}/R_{drift} = C_{dg}/C_{sg}$, listed in Tab. 3 and the values of R_{ds} at V_{gs} = 20V in Fig. 1b). 5b) plot of R_{ch} and R_{drift} scaled by the active area (A) of the DUTs listed in Tab. 1.

Conclusion

This work demonstrates a new and simple approximation technique to determine $R_{ch}(T)$ and $R_{drift}(T)$ from the MOSFET's I_d-V_{gs}, C_{sg} and C_{dg} characteristics. The separation of $R_{ds}(T)$ into $R_{ch}(T)$ and $R_{drift}(T)$ allows a more accurate modeling of the heat generation within SiC power MOSFETs during high-temperature operation [16]. In addition, the new method serves as quality control of the MOSFET's gate structure and can be applied to extract other MOSFET parameters e.g., μ_{eff}, when comparing devices with different channel length L, and suchlike.

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