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Humidity Robustness of 3.3kV SiC-MOSFETs for Traction Applications – Compared to Standard Silicon IGBTs in Identical Packages

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Abstract. Silicon carbide (SiC) MOSFETs are gaining more and more market share in typical silicon (Si) IGBT applications such as traction or renewable energies. Especially in reliability sensitive traction applications, medium voltage IGBT-modules (3.3 kV-6.5 kV) are widely used and introducing SiC-MOSFETs to such industries is the next self-evident step already on the way. While their superior electrical performance has been generally accepted already (e.g. [1]), SiC-modules have not yet established a track record of high reliability in this voltage class. For this study, 3.3kV SiC-MOSFET-switches were compared to standard Si-IGBTs regarding their humidity robustness under high voltage bias. Both chip types had been assembled in the same traction rated packages to exclude this influence. The Si-IGBTs resembled the well-known industry standard performance, while the SiC-MOSFETs show no degradation within the reported test time of 2000 h. Given the fact [2], that the latest Si-IGBT generation offers a much better humidity performance as well, the standardised HV-H³TRB is no longer sufficient to provoke failures within a reasonable testing time. On the one hand, this suggests that humidity driven failures will not be an issue under field conditions anymore. On the other hand, even harsher tests are required to investigate differences in humidity performance.

State of the Art Accelerated Testing under High Humid Conditions

Accelerated reliability testing is mandatory for any kind of application-relevant life time estimation of power semiconductor devices. These testing procedures are well documented and standardised for the currently used technologies such as Si-IGBTs. A number of standards and guidelines define test procedures as well as accelerated conditions to determine the humidity robustness of such devices:

- IEC60749-5 [3], general standard
- ECPE guideline PSRRA01 [4], traction applications
- ECPE guideline AQG 324 [5], automotive applications

All of the said documents refer to the well-established HV-H³TRB (**H**igh **V**oltage, **H**igh **H**umidity, **H**igh **T**emperature, **R**everse **B**ias) test. While the climate is constant at 85 °C and 85 % relative humidity, the electrical stress differs between the standards. For example, [4] defines the electrical stress based on the DC-link voltage of traction applications, while in [5] 80 % of the device's nominal voltage (V_{nom}) is recommended. In each case of the mentioned standards, the bias voltage is limited by the power loss and the resulting temperature increase at the chip interface. As described in [6], the bias voltage is an important acceleration factor, resulting in a faster degradation of silicon devices. However, well designed, latest Si-IGBT-modules proved to be highly robust against humidity and show little to no degradation in accelerated humidity testing anymore [2]. While the failure mechanisms and the corresponding degradation is well documented for standard Si-IGBTs, the situation for SiC-MOSFETs is completely different. SiC enables higher voltages even for the discrete market, leading to a variety of EMC-packaged SiC-MOSFETs with blocking capabilities up to 1.7 kV. Therefore, humidity robustness assessments are often carried out on discrete devices [7, 8, 9] showing an overall high robustness. However, the performance under high humidity is strongly influenced by the packaging materials and especially for high power modules, silicone gel insulated housings need to be considered. In contrast to Si-IGBT-modules, SiC-MOSFET-modules tend to be

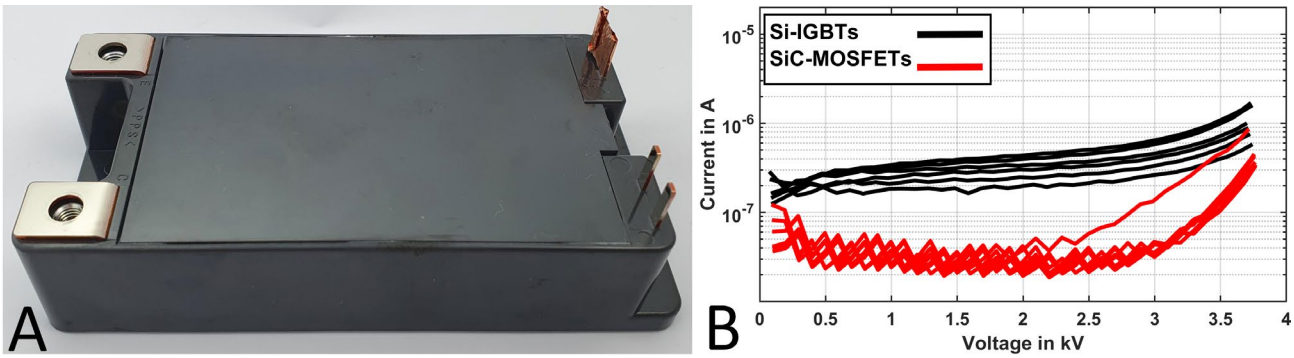

Figure 1: (A) Research grade high voltage single switch package, technologically similar to production modules for traction applications (foot print: 125 mm by 60 mm),
(B) Initial blocking curves of all devices under test measured at room temperature. SiC-MOSFETs exhibit a generally lower leakage level mostly below the measurement resolution.

much more reliable when being exposed to constant high humid climatic conditions. Studies [10, 11] show an extended lifetime under 80 % V_{nom} for 1.2 kV SiC-MOSFETs in a constant climate of 85 °C and 85 % rel.h. of more than 3,000 h. Referring to [10], a lifetime of up to 10,000 h is possible for SiC-devices, while conventional Si-IGBTs in the same package type failed before 2,500 h of accumulated test time.
However, no benchmark of the humidity induced degradation of 3.3 kV SiC-MOSFETs has been published and the direct comparison to state-of-the-art Si-IGBTs with their known field performance shown in this work is the best method to determine the usability of 3.3 kV SiC-MOSFETs for traction applications.

Devices under Test (DUT)

Power modules in the voltage class of 3.3 kV are particularly interesting for traction applications and need to fulfil high reliability specifications due to the long service life of 20-40 years. At the moment, the low availability and the high cost prohibit fully populated SiC-modules as DUTs for reliability test and therefore, an engineering, single-switch/-chip-package was used to compare the two different device types. Fig. 1 (A) shows the module, developed and manufactured by Mitsubishi Electric Corp., which is specially designed for reliability testing of different chip concepts. Furthermore, this package type is manufactured with traction rated materials and produced on the same line like the standard modules. With the same packaging design and the same materials used, a comparison between Si-IGBT- and SiC-MOSFET-chips is more meaningful. The IGBT-chip is always operating with an external free-wheeling Si-diode, leading to a second chip per module, while the SiC-MOSFET can be operated individually due to its body diode. These configurations imply, that the actual comparison will include the minimum usable number of chips per switch of each technology.

Table 1: Test groups for the different chip types and bias voltages

Split	Si-IGBT-Modules	SiC-MOSFET-Modules
65% V_{nom}	**3**	**4**
90% V_{nom}	**3**	**4**
Reference	**2**	**2**

Test Setup, Procedure and Conditions

The testing procedure [2, 6, 9, 10] is based on the combination of intermediate blocking curve measurements (I_{DSS} (I_{CES}) @ V_{GS} (V_{GE}) = 0 V) at room temperature between test cycles and a leakage monitoring during the test cycles of different durations. To ensure the same conditions throughout all cycles, the voltage was ramped up after pre-conditioning the devices for a minimum of 24 h at 85° C and 85 % rel.h. Comparable intermediate measurements are key for the degradation monitoring and therefore, the DUTs were dried post-test at 85° C, 10 % rel.h. (4 h) and 50° C, 10 % rel.h. (20 h).

Since silicon IGBTs exhibit a higher leakage level compared to SiC-MOSFETs, different current resolutions have to be utilised for the respective device types. Therefore, a highly sensitive, 32 channel, leakage logging system is used to monitor the current under high voltage during the stress test. The same system ensures a fast turn-off in case of a failure, protecting the devices from excessive damage. If an over-current event is triggered, the voltage source is disconnected by an external half-bridge and ramped up again after opening a high voltage relay at the corresponding channel.
After each test cycle, all devices are measured individually with a high voltage curve tracer up to ~110 % V_{nom}, although, the degradation can be identified long before the blocking capability reaches the nominal voltage of the device. The sensitive parameter for this type of measurement is the bend-off-voltage (premature avalanche), which is the first indication of the avalanche inception. Stopping the measurement at this voltage level avoids damaging the devices and improves the degradation monitoring. Fig. 1 (B) shows the blocking curves of the complete test group with differences in the leakage level as well as the shape of the curves. The scattering between the DUTs of each test group is in an acceptable range and just one SiC-MOSFET shows an elevated leakage current above 2 kV. The complete test group contains 18 devices, 10 SiC-MOSFET- and 8 Si-IGBT-modules. Two devices each are used as references to distinguish between voltage and climate related degradation (chamber reference, placed in the chamber without bias voltage), as well as calibrating the intermediate blocking curve measurements (shelf reference, stored at room climate also without bias). The test system can provide two different voltage levels at the same time. A first test voltage is chosen with respect to the application relevance [4] at a level of 65 % V_{nom}, which offers a realistic electrical stress for the modules. To achieve degradation in an acceptable time frame, a higher acceleration factor is mandatory and therefore, a higher voltage level with 90 % V_{nom} is used as well (tab. 1). For Si-IGBTs, the acceleration factor between 65 % and 90 % of the nominal voltage is expected to be 2.1 [6] and this might enable an early degradation of the SiC-MOSFET-modules, too. However, due to the engineering status of the SiC-MOSFET-modules, a higher bias voltage might be an over-stress, resulting in early failures.

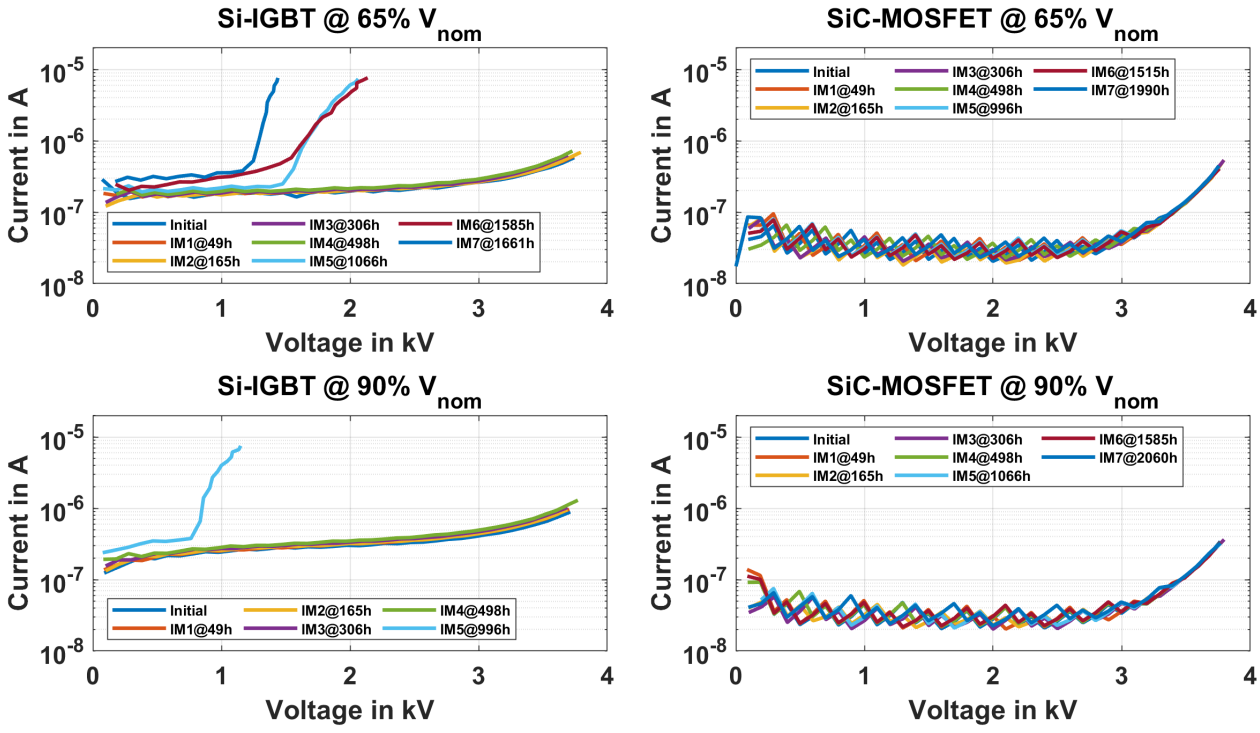

Figure 2: Blocking curve evolution for Si-IGBTs and SiC-MOSFETs at the corresponding intermediate measurements over time with little to no change in case of the SiC-MOSFETs.

Results

An overall test time of 2,000 h has been reached, with intermediate measurements at around 50 h; 150 h; 300 h; 500 h; 1,000 h; 1,500 h and 2,000 h, respectively. An insulation breakdown event occurred at ca. 1,000 h leading to a voltage drop during ~60 h at the 90% test group (fig. 3). Within the complete test time, all IGBT-modules were turned off one by one due to a high leakage current during testing and due to a low blocking capability in the intermediate measurements (limit at 10 µA). The first failure occurred after 551 h and the last IGBT-module was removed after an accumulated test time of 1,661 h due to over current events at the voltage ramp up. All silicon devices showed the typical behaviour, already reported in [2, 6] with an oscillation in the leakage current monitoring combined with a reduction of the bend-off-voltage in the intermediate measurements. Every Si-IGBT-module was shut down during the test cycle when reaching the current limit of 450 µA. The split, connected to 65 % V_{nom} showed a significantly longer lifetime compared to the 90 % split. An example of the blocking curve evolution is shown in fig. 2 with the corresponding leakage monitoring in fig. 3.

In contrast, the SiC-MOSFET-modules show no sign of degradation at the blocking curve measurements and no differences can be seen with respect to the different voltage levels (fig. 3). A significant difference was found in the leakage monitoring. At 90 % V_{nom}, the leakage current increases over time after an accumulated test time of ca. 300 h and decreases after 700 h, resulting in an elevated leakage level with respect to the initial value. This effect is reproducible in every test cycle and starts again in a more pronounced way after 1,700 h. Oscillations like this were monitored on more devices, biased with 90 % V_{nom} in this test. At room temperature and after the drying procedure, no evidence of degradation can be found in the intermediate measurements.

In summary, the conventional Si-IGBTs show an expected behaviour within the first 2,000 h of testing, while the SiC-MOSFETs confirm the expectations by an outstanding performance in this type of accelerating testing.

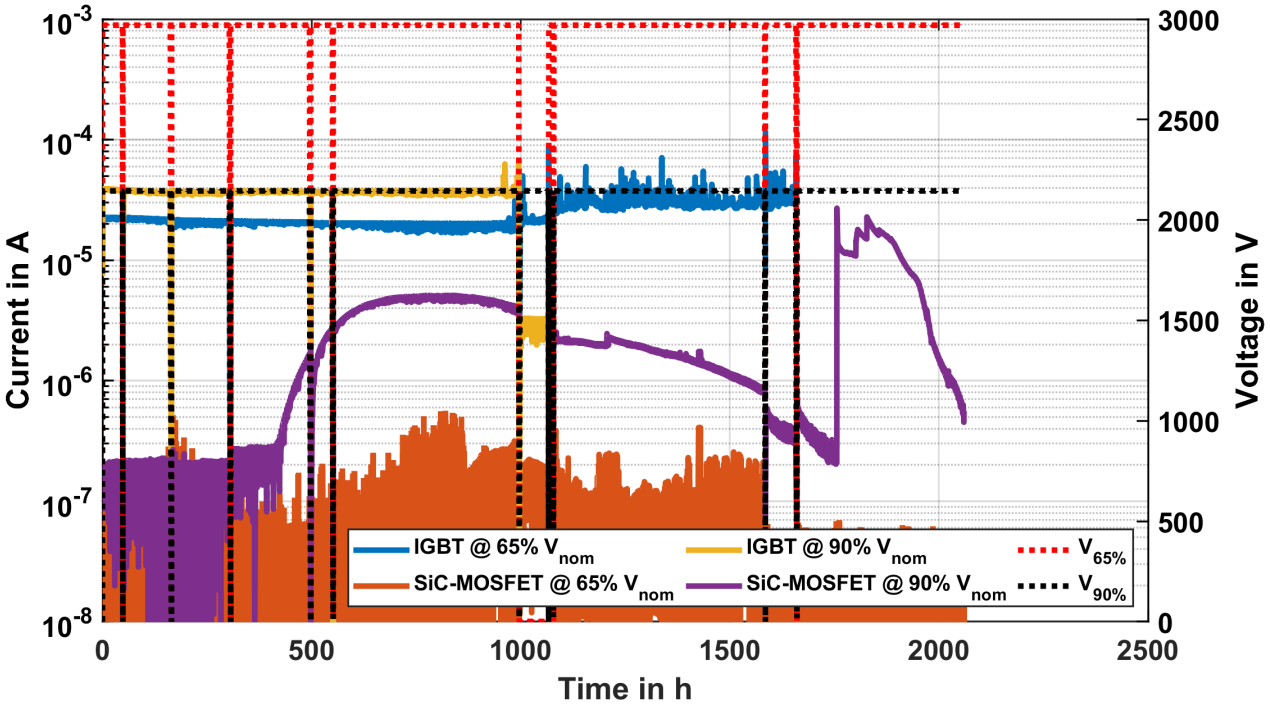

Figure 3: Leakage current monitoring with two over-current events at 996 h and 1,661 h, leading to a turn off procedure for both IGBT-channels. At 90 % V_{nom}, the SiC-MOSFETs shows oscillations on the leakage current. This phenomenon is just measurable while the climatic stress and the bias are applied and no evidence of it can be found after drying the devices.

While none of the SiC-MOSFETs showed any degradation, the bend-off-voltage of the IGBTs is significantly decreased after stressing these devices. All IGBT-modules contain a diode- and an IGBT-chip and therefore, the deterioration of both chips might be different. In this case, the diodes of two IGBT-modules were disconnected to verify the remaining blocking capability of the IGBT-chip. In fig. 4, both devices were disconnected from high voltage at the same time and have a comparable state of degradation. The leakage current of the IGBT-chips is more or less following the trend of the full module curve and is therefore, the main cause for the shifted bend-off-voltage. With these highly degraded chips, the comparison to the SiC-MOSFETs is proved meaningful due to the negligible influence of the anti-parallel diode.

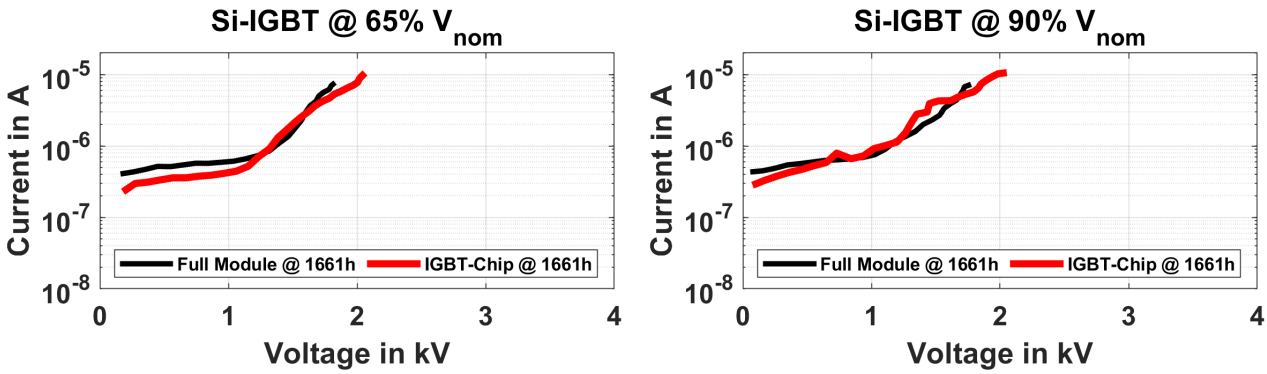

Figure 4: Blocking curves of degraded modules after disconnecting the diode inside the package. The IGBT-chip blocking curve is following the curve of the complete module, indicates it as the predominant part of the switch's degradation.

Statistical Analysis

Fig. 5 shows an approach to compare the degradation of a high number of devices and splits over testing time. The graph type illustrates the normalised bend-off-voltage, determined at the intermediate measurements, over accumulated testing time. The voltage is measured at 760 nA for

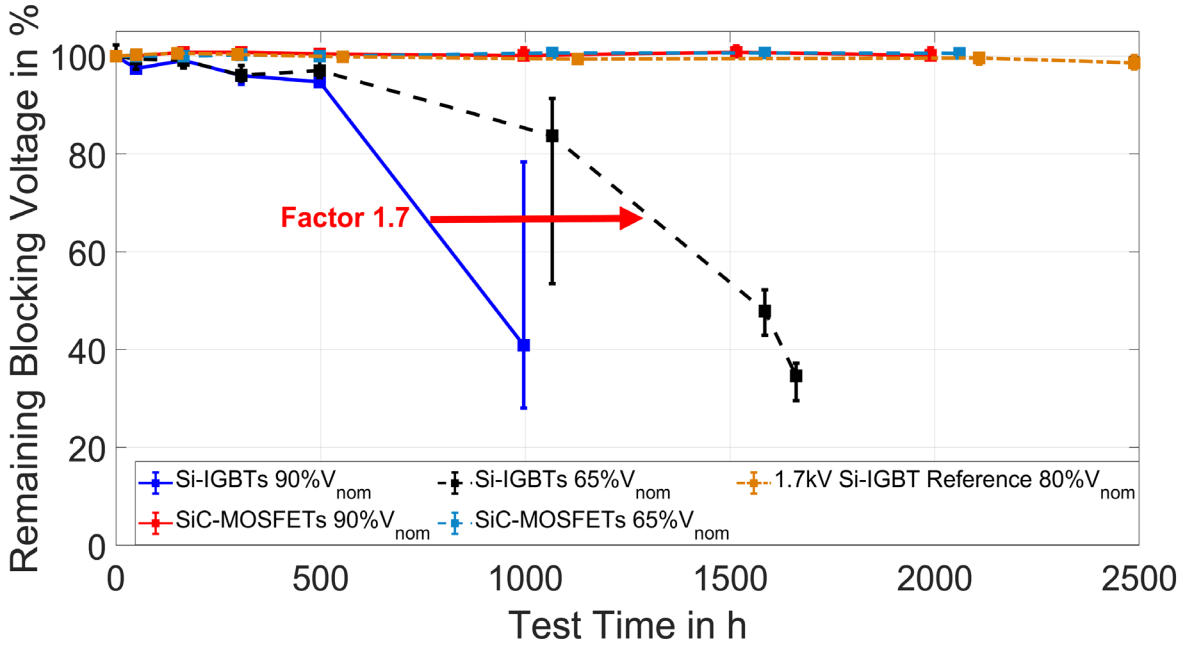

Figure 5: Normalised remaining blocking capability (voltage measured at a defined leakage current) evolution over time for 3.3 kV SiC-MOSFETs and silicon IGBTs compared to a 1.7 kV silicon IGBT benchmark [2] (at 80 % V_{nom}). The different bias voltages (90 % V_{nom}, solid lines, 65 % V_{nom}, dashed line) lead to an acceleration factor of 1.7 for the conventional Si-IGBTs

the IGBTs and 300 nA for the SiC-MOSFETs after every test cycle. Both current levels are based on the maximum voltages reached in the initial measurement over the complete device group.
Each square in the graph represents the median value of the measured voltage of the corresponding split together with the 25 and 75% quartiles as error bars. In case of the Si-IGBTs, the quartiles represent one DUT each (split size 3). Additionally, a 1.7 kV Si-IGBT-reference with the latest chip set is shown [2]. The SiC-MOSFETs are not showing any sign of decreasing blocking capability over time, while the Si-IGBTs indicate the typical degradation trend. An early voltage drop can be seen after the first 50 h of testing usually attributed to redistribution of mobile ions [12] and a second, more pronounced reduction after 500 h of test time due to aluminium corrosion and delamination of insulating layers. Beyond 500 h, the different voltage stresses can be distinguished, leading to a comparable result as documented in [6]. The two different voltage levels lead to an acceleration factor of 1.7 for the Si-IGBTs, which is in reasonable agreement with other experiments (2.1 in [6] and 1.83 in [2]).

Summary and Outlook

A highly accelerated test to determine the humidity robustness of 3.3 kV SiC-MOSFETs in comparison to 3.3 kV Si-IGBTs was carried out, showing an excellent result for the MOSFETs within an accumulated test time of 2000 h. While all of the IGBTs failed latest in the intermediate measurement, the SiC-MOSFETs do not show any kind of degradation. Even at the higher bias voltage of 90 % V_{nom}, an outstanding performance of the SiC-devices can be documented. Different, at the moment unclear events of leakage current oscillations were monitored during the test time, but no evidence of permanent damage or degradation was found at room climate. Furthermore, the direct comparison between SiC-MOSFETs and Si-IGBTs was valid due to the negligible impact of the diodes.
The single-chip package type with traction rated materials proved to be a reasonable way of testing new chip designs and especially suitable for SiC and related materials. With this method, different application relevant packaging and chip configurations can be tested at low cost and time effort.
Overall, the static testing under high humidity and voltage is not sufficient to trigger any degradation of the SiC-MOSFETs, used in this experiment, at least not in a reasonable testing time of 2,000 h. This is in line with the previously published data sets and therefore, standard testing needs to be improved for SiC-devices. Some manufactures have already published extended testing parameters [13], but as presented in this study, a test time of 2,000 h under constant conditions will not lead to significant degradation. But, there are some approaches for application relevant testing such as dynamic climate testing (e.g. AC-HTC, [12]) or thermo-mechanical-preconditioning [14] to provoke delamination and degradation of package materials.
Within the rest of the RECET4Rail project, the constant climate and voltage testing will be continued and extended to more application relevant test conditions.

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References

[1] M. Hruska, et al., Benefits of Using the NEW 1700V and 3300V High Power Modules for Traction Applications, PCIM'21 (2021)

[2] J.-H. Peters et al., Improved HV-H³TRB robustness of a 1700 V IGBT chip set in standard power modules, Microelectronics Reliability Vol. 126, 2021

[3] IEC60749-5:2017, Semiconductor devices – mechanical and climatic test methods, 2017

[4] ECPE PSRRA01, HV-H3TRB tests for Power Semiconductor, 2019

[5] ECPE AQG324, Qualification of Power Modules for Use in Power Electronics Converter Units in Motor Vehicles, 2021

[6] C. Zorn et al., Temperature-humidity-bias testing on insulated-gate bipolartransistor modules-failure modes and acceleration due to high voltage, IET Power Electronics (ISPS2014)

[7] I. Voss et al., Reliability and Ruggedness of SiC Trench MOSFETs for Long-Term Applications in Humid Environments, PCIM'18 (2018)

[8] J. Jormanainen et al., High Humidity, High Temperature and High Voltage Reverse Bias – A Relevant Test for Industrial Applications, PCIM'18 (2018)

[9] M. Hanf et al., H³TRB Test on 1.2 kV SiC MOSFETs, PCIM'18 (2018)

[10] F. Hoffmann et al., Comparison of the H3TRB Performance of Silicon and Silicon Carbide Power Modules, ECSCRM'21 (2021)

[11] P. Salmen et al., Qualifying a Silicon Carbide Power Module: Reliability Testing Beyond the Standards of Silicon Devices, CIPS'22 (2022)

[12] N. Tanaka et al., Robust HVIGBT module design against high humidity, PCIM'17 (2017)

[13] Infineon: Whitepaper 07-2020: How Infineon controls and assures the reliability of SiC based power semiconductors, www.infineon.com, 2020

[14] F. Hoffmann et al., Investigation on the Impact of Thermo-Mechanical Stress on the Humidity Ruggedness of IGBTs by Means of Consecutive PCT and H3TRB Testing, ISPSD'20 (2020)