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Reliability and Standardization for SiC Power Devices

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Abstract. The demand is rapidly increasing for SiC MOSFETs and diodes for power electronic conversion semiconductor (PECS) applications such as electrified vehicle charging and traction, energy storage systems and industrial power supplies. These applications employ a high quantity of large-area die per system while demanding high system-level reliability under aggressive electrical and environmental operating conditions. In addition, SiC devices exhibit some failure mechanisms that are more severe than, or non-existent, in Si devices. This situation demands thorough and novel device reliability characterization and quantification. It is also driving the development of industry consortia standards and guidelines at a much faster rate, and relatively earlier in the technology maturation phase, than occurred in the Si industry. In this paper, I will review some of the key published reliability performance data, stress procedure methodologies used, and implications for key applications. I will also compare and contrast the existing guideline and standard documents and suggest directions that are being explored for future documents. I will also discuss how future guidelines and standards are being developed to cover the SiC-specific failure mechanisms for representative mission profiles for some key applications, particularly electrified vehicles.

Introduction

SiC power MOSFETS and Schottky diodes are being rapidly adopted for power electronic conversion semiconductor (PECS) applications such as electrified vehicle charging and traction, energy storage systems and industrial power supplies [1]. SiC power MOSFETs are already well established in electrified vehicle on-board chargers and are gaining traction in off-board chargers. These devices offer battery electric vehicles the benefits of improved range and/or cost of the inverters as compared to the current Si IGBT solution in inverters. Devices have been shipping in high volume in server power supplies and in increasing volume in traction inverters. Although SiC MOSFETs have been in existence since at least 1987, broad adoption in such high volume and high reliability markets has taken decades. This is because orders of magnitude of improvement was needed in many aspects of the devices, especially in the gate oxide quality and reliability.

The challenge is that all these markets, particularly transportation, expect extremely high reliability at the system level. The application requirements are quite lofty: high number of SiC die and total SiC active area (hundreds to thousands of mm^2), high junction temperature (typically 175 °C and beyond) and low failure rates (< 1 ppm per year cumulative during "early adoption," with improvement expected very soon afterward.) Meanwhile, the reliability situation in SiC is unique as compared to silicon

- Some SiC failure mechanisms are more severe than in Si
- At least one failure mechanism is unique to SiC and does not manifest in Si
- The demands on SiC are in many ways higher than they have been on Si

Accepting this challenge means that SiC device manufacturers must be able to demonstrate outstanding reliability predictions in all phases of the "bathtub curve," by delivering thorough and sometimes novel characterization of the quality, random failure rate and wear-out lifetime. But it also means that industry consortia organizations, consisting of manufacturers and end-users, must develop guidelines and standards at breakneck pace, as compared to the silicon industry. In the silicon

industry, guidelines and standards took much longer to initialize and develop relative to the state of maturity and degree of wide-spread adoption of the technology.

Failure Mechanisms in SiC

Some of the failure mechanisms observed in SiC devices are similarly observed in Si devices, such as single-event burn-out (SEB, due to terrestrial neutrons) and gate oxide wear-out [2]. SiC MOSFETs display the bias-temperature instability (BTI) degradation mechanism with similar acceleration factors and time dependence as in Si MOSFETs. However, BTI in SiC devices can be much more prominent due to the higher density of interface and near-interface charge traps, so it necessitates more thorough characterization of the BTI response, including special techniques to characterize the threshold voltage (V_T) [3]. SiC MOSFETs are susceptible to bipolar degradation (increased on-resistance and possibly leakage), due to the conversion of basal plane dislocations (BPDs) to stacking faults under the influence of electron-hole recombination, which occurs in third quadrant operation. This bipolar degradation mechanism is unique to SiC and requires novel reliability characterization. Notably, the observations are consistent with bipolar degradation being an early life failure rate (ELFR) mechanism rather the intrinsic wear-out, because only devices with pre-existing BPDs experience bipolar degradation. By characterizing these mechanisms, a full reliability "bathtub curve" may be constructed, with representation of the early life failure rate / "infant mortality" (bipolar stability), constant (random) failure rate during useful life (SEB and random latent defects) and wear-out (gate oxide, V_T stability and packaging) phases of the product lifetime. The reliability data shown in this paper is from Wolfspeed Gen3 SiC planar MOSFETs, with salient features shown in Fig. 1. These reliability considerations generally also apply to trench MOSFETs, although presence and severity some of these effects may differ.

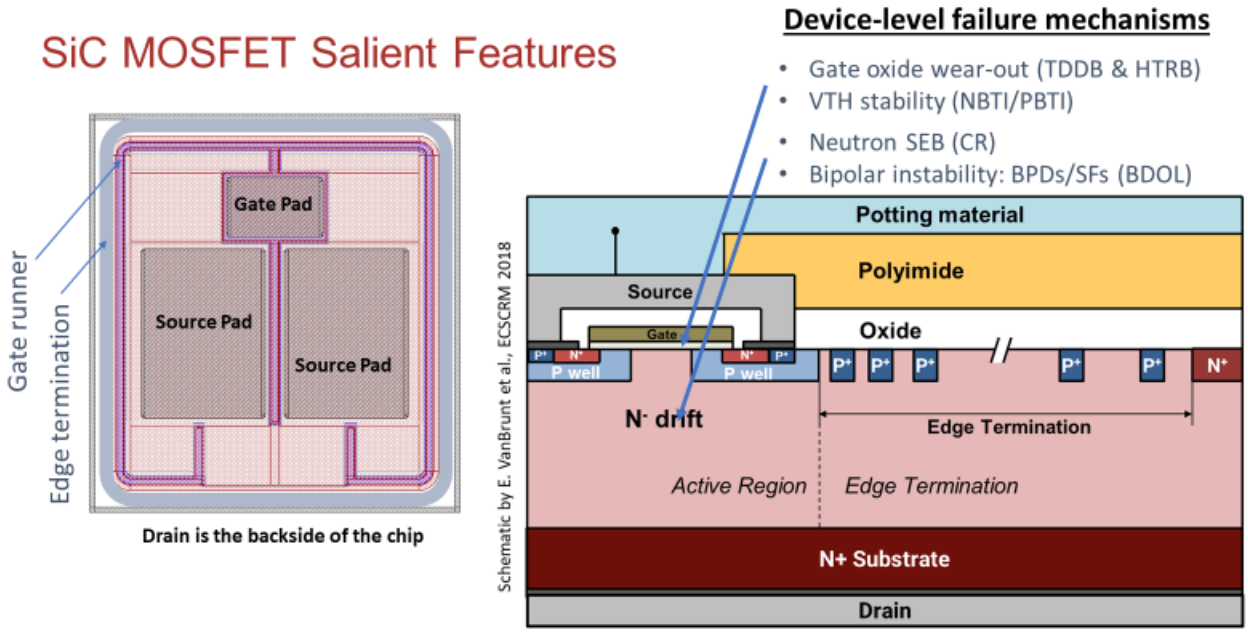

Fig. 1. Wolfspeed SiC planar MOSFET schematic plan view, cross section, salient features, and representative failure mechanisms.

Bipolar Stability. Recombination-enhanced stacking fault (SF) glide at basal plane dislocations (BPDs) [4] presents a fundamental material challenge for reliable 4H-SiC bipolar device operation in SiC MOSFETs. This occurrence can result in increased resistance and leakage. However, modern 4H-SiC substrate production practices have resulted in a massive decrease in the basal plane dislocation density, which, when combined with suitable production screening methods, enable reliable devices with extremely low BPD density, and hence low failure rate for this mechanism and little to no concern with respect to bipolar stability. The bipolar stability can be demonstrated using a body diode operating life (BDOL) stress test, in which a constant current is applied to the MOSFET

in 3rd quadrant mode, with enough heatsinking and/or duty cycle to maintain junction temperature within maximum ratings. For example, Wolfspeed, Inc., has published BDOL results on medium voltage devices with 3.3 kV and 10 kV ratings, over 60 devices of each type samples from 3 production lots, with zero failures and negligible parametric shift before and after BDOL stress (Fig. 2). [5] This result successfully demonstrates excellent bipolar stability on production MOSFETs, which may be considered as more stringent than on lower voltage devices, such as (650 – 1200) V, because the SiC epitaxial layer is thicker and therefore has a higher probability of a basal plane dislocation being present.

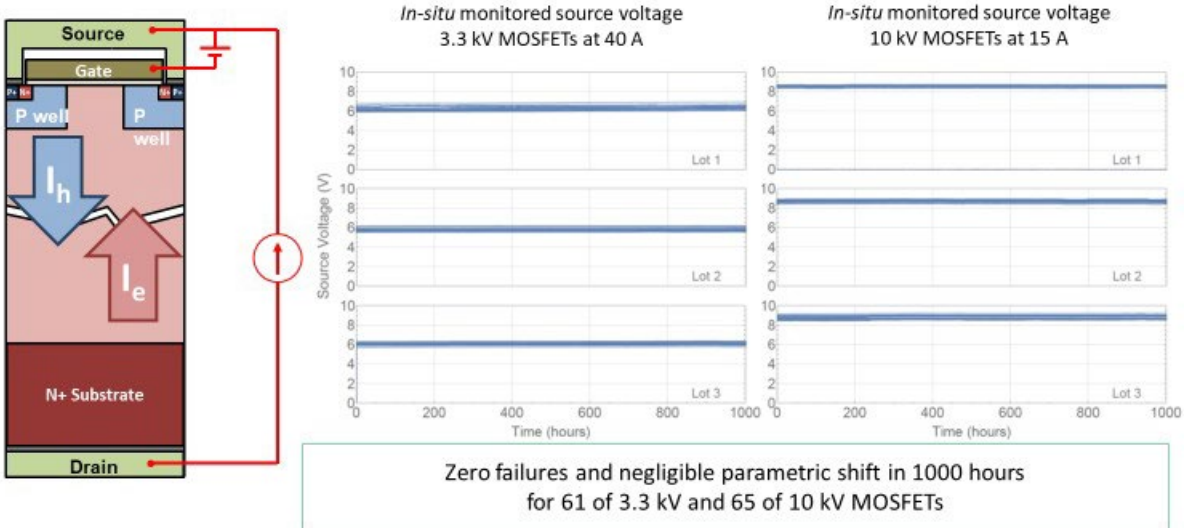

Fig. 2. (Left) Schematic of BDOL stress configuration, MOSFET active cell cross section and indication of electron-hole recombination current leading to conversion of BPDs to SFs (Right) BDOL current versus time for Wolfspeed qualification testing of 3.3 kV and 10 kV medium voltage production SiC MOSFETs (after [5]).

It is worth noting that if a SiC MOSFET does not have any BPDs to begin with, then SFs cannot nucleate and grow, and bipolar degradation will not occur. Therefore, reducing the occurrence of and screening out BPDs are very important for ensuring 3rd quadrant bipolar stability for SiC MOSFETs. Despite decades of research, the literature evidence has not yet shown how bipolar stability can be accelerated in a well-behaved fashion so that a predictive life model could be constructed, as is done for gate oxide wear-out model, for example. Fortunately, most or all bipolar stability failures occur in a relatively short period of time (hours to days, rather than months and years, of BDOL stress). Bipolar stability therefore seems to be best treated an early life failure rate mechanism, rather than a wear-out mechanism. Therefore, in order to ensure good bipolar stability reliability for applications that employ 3rd quadrant operation, manufacturers must rely on low BPD SiC epitaxy and adequate screening, and demonstrate it by testing large sample sizes and large area devices, fortunately for just relatively short periods of BDOL stress time.

Threshold Voltage Stability. Gate bias can cause the V_T stability of a SiC MOSFET to drift over time, which can change the on-state and/or blocking characteristics of the device. This effect is commonly referred to as positive/negative bias-temperature instability (PBTI/NBTI). BTI can occur in Si as well as SiC MOSFETs, but the effect is usually more pronounced in SiC MOSFETs because they have a higher density of traps at, and near, the oxide interface that are filled, emptied and/or created by oxide electric field. BTI is accelerated by electric field and temperature and displays a weak power law with time. [6] An exemplary characterization of BTI in production SiC MOSFETs by Lichtenwalner et al. shows a time exponent of ~0.12 (Fig. 3), which is similar to that of Si devices with a nitrided oxide, like SiC does. [6] This similarity indicates that the physical mechanism is the same in SiC and Si devices, namely, oxide charge trap filling and emptying. The lifetime extrapolation shows that the BTI is predicted to drift only hundreds of millivolts over thousands of hours, but it is worth noting that even this much drift is small compared to the voltage over which

such devices are typically switched in PECS applications, and is therefore not expected to appreciably affect system performance.

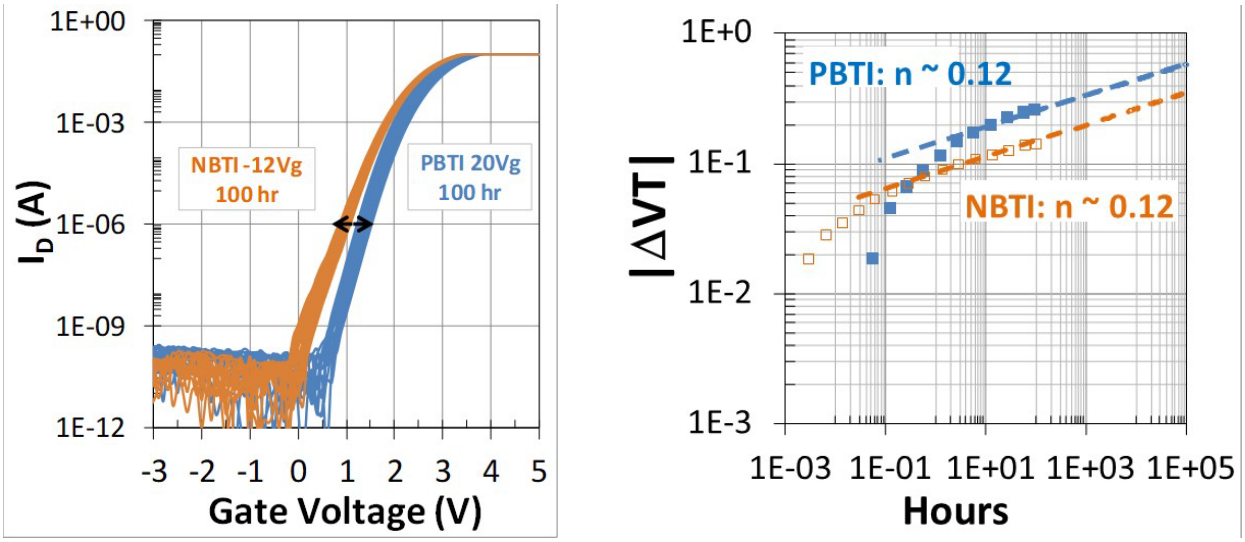

Fig 3. BTI for a representative Wolfspeed Gen3 1200 V SiC MOSFET. (Left) Drain current versus gate voltage curves drifting with constant gate bias over stress time up to 100 hours of cumulative constant gate bias stress, with intermediate read-out points. Extrapolation of the PBTI and NBTI predicts only hundreds of millivolts of drift for thousands of hours of accelerated constant gate bias stress at 150 °C.

It is noteworthy that the V_T drift observed under gate bias stress can be composed of long-term V_T drift, transient V_T changes, and V_T hysteresis or changes in hysteresis. To demonstrate this effect, Fig. 4 shows how the V_T drifts over time for constant gate bias as compared to interrupted bias, where the stress is periodically removed, and the device allowed to relax before resuming stress. The difference between these behaviors shows that recoverable transient effects dominate, and the V_T drift caused by interface degradation is relatively small. This illustrates how much of the V_T drift observed in constant gate bias stressing may not represent permanent device degradation, but rather reflects temporary parametric drift, which may be less pronounced in typical switching applications.

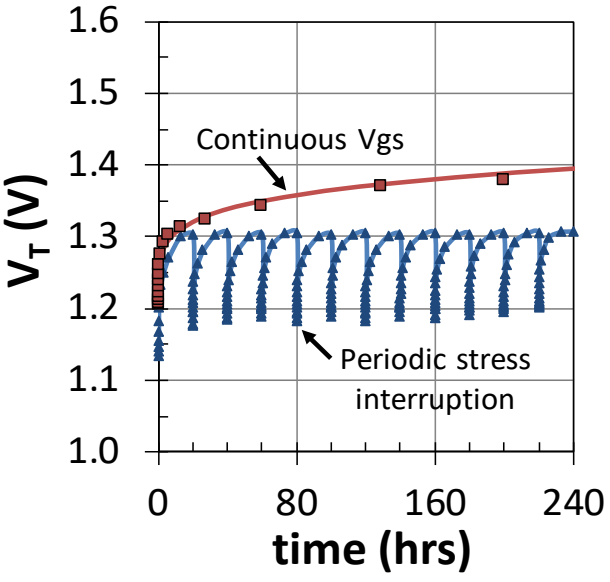

Fig. 4. V_T versus gate bias stress time for a Wolfspeed Gen3 900 V SiC MOSFET, showing PBTI at 150 °C with a continuous 19 V stress, as compared to the VT response when the stress is periodically removed. The difference reveals that recoverable transient effects dominate. [7]

Gate Oxide Wear-out. The SiC MOSFET gate oxide wear-out has been characterized by time-dependent dielectric breakdown (TDDB) testing. TDDB data on Wolfspeed Gen3 1200 V MOSFETs is well modeled by a single Weibull statistical distribution with high Weibull beta value, which demonstrates good intrinsic wear-out behavior and no evident extrinsic defect population even at highly accelerated conditions (Fig. 5). The TDDB data versus temperature and gate voltage is well described by the thermo-chemical model (Eq. 1), which has been widely used for Si MOSFETs [8],

$$t = A_0 exp\left(\frac{(\Delta H_0 - p_{eff}E)}{k_B T}\right) \quad (1)$$

where E is the gate oxide electric field, T is the temperature, ΔH_0 is the Si-O bond strength at zero applied gate electric field and p_{eff} is the effective Si-O dipole moment.

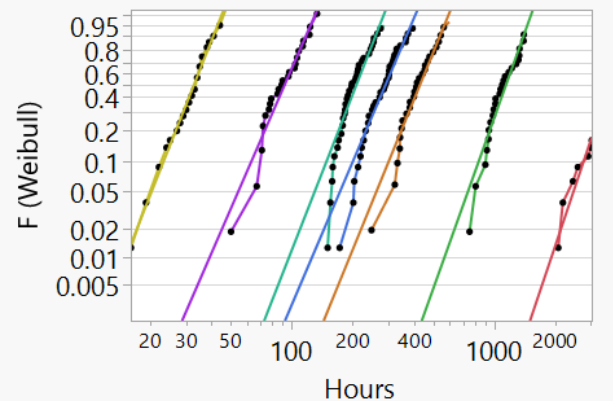

Fig. 5. TDDB lifetime distributions (Weibull scale) by stress conditions.

Applying this model to several 1200 V and 650 V full production devices gives intrinsic lifetime predictions of approximately 1E8 hours at 15 V continuous gate bias at 175 °C for all the devices. This shows that the gate oxide lifetime of Wolfspeed devices is consistent for different sizes and voltage classes (Fig. 6), which is expected due to the similarity of gate structure and wafer fabrication processing. The resulting model fit parameters are similar to those found for Si devices, which indicates that the gate oxide wear-out mechanism is similar for SiC and Si MOSFETs.

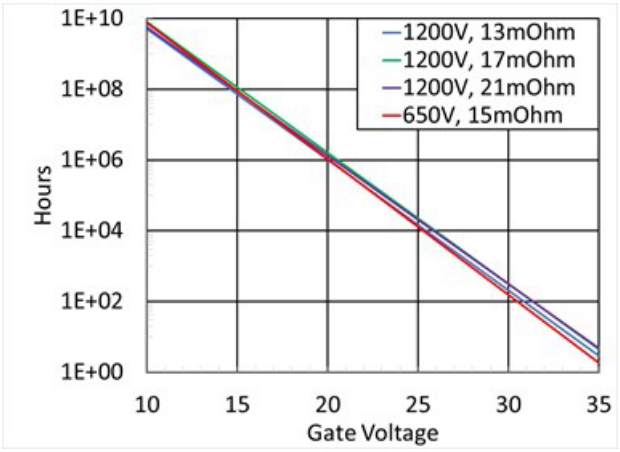

Fig. 6. TDDB intrinsic lifetime extrapolation of several Gen3 1200 V and 650 V SiC MOSFETs.

High Temperature Reverse Bias (HTRB). The SiC MOSFET lifetime under blocking conditions may be characterized by accelerated HTRB testing (ALT-HTRB), certain device design attributes permitting. SiC MOSFETs display relatively low leakage up to the avalanche voltage. Devices are typically designed with some margin between the avalanche voltage and the rated voltage of the device, in order to ensure reliability and robustness for against high drain bias voltages, especially over-voltage transients. This margin can enable accelerated drain bias testing above the rated voltage but less than the avalanche voltage. In this regime, the oxide electric field in the JFET gap of the device can be high enough to induce gate oxide wear-out. Constant bias ALT-HTRB testing shows that devices display relatively low gate and drain leakage until abrupt gate-source short failure occurs, with little to no precursor signal, similar to what happens in TDDB.

Fig. 7 shows the results of ALT-HTRB testing on Wolfspeed Gen3 1200 V SiC MOSFETs. The ALT-HTRB lifetime data was fit using Weibull statistics and a linear-V model as described above for TDDB. The results show that the predicted median lifetime is approximately 1E8 hours at 175 °C and 800 V, which is the bus voltage at which a 1200 V device is often used in typical high reliability PECS applications.

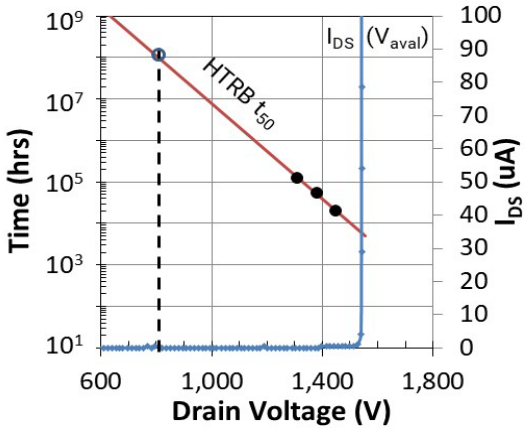

Fig. 7. (Left axis) Median ALT-HTRB lifetime versus drain bias at 150 °C, with extrapolation to ~1E8 hours at 800 V. (Right axis) Drain current versus voltage of a representative device, showing the avalanche voltage of >1450 V.

Failure analysis shows that the ALT-HTRB failure mechanism is gate oxide breakdown in the center of the JFET gap (Fig. 8). This is expected because that is the location of the highest gate oxide electric field under reverse bias. Failure analysis found no evidence of edge termination breakdown or SiC breakdown (Fig. 9), which demonstrates that gate oxide wear-out is the only failure mechanism of concern for reverse bias reliability. This supports the use of the linear-V (in this case, drain voltage, which is directly related to gate voltage) model for ALT-HTRB lifetime prediction, as described above.

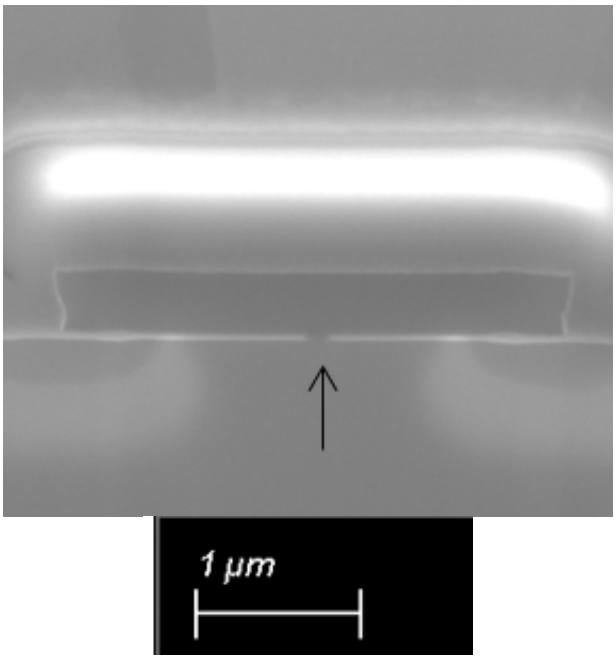

Fig. 8. Scanning electron microscope image of FIB cross section through the failure site of a Wolfspeed SiC MOSFET that has reached end-of-life in ALT-HTRB stress test. Arrow highlights the location of the oxide breakdown that occurred during that accelerated life stress test.

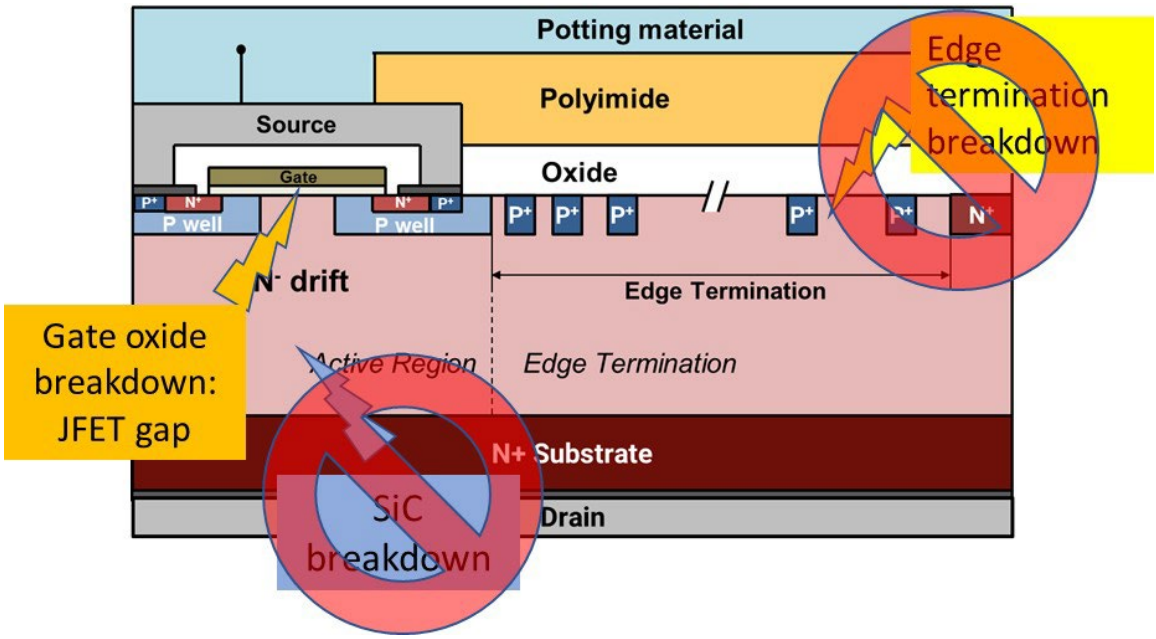

Fig. 9. Schematic cross section of Wolfspeed SiC planar MOSFET indicating that failure analysis has shown that the only failure mechanism that occurs during ALT-HTRB stressing is gate oxide breakdown, and not edge termination breakdown or SiC breakdown.

Standardization

These intriguing reliability aspects of SiC PECS devices have been driving industry consortia to urgently issue guidelines and standards for reliability testing and qualification, even while methodologies are being actively developed and new data is being published. The International Electrotechnical Commission (IEC) have published international standard reliability test method documents on bipolar degradation [9] and bias temperature instability [10]. JEDEC has published documents on bias temperature instability evaluation [11], measuring the threshold voltage of SiC MOSFETs [12], representing switching losses of SiC MOSFETs in datasheets [13], and most recently for evaluating dV/dt robustness [14]. The European Center for Power Electronics (ECPE) has revised its document on qualification of power modules for use in power electronics converter units in motor vehicles to now include an annex section on qualification of SiC-based power modules, which includes specific guidance on power cycling, high temperature gate bias, high temperature reverse bias, dynamic reverse bias, and others [15].

Even a cursory review of these documents shows that alignment between these consortia has not yet been achieved for even some of the major aspects of the reliability stress procedures, and certainly not for a standard qualification guideline such as AEC-Q101 or JEDEC JESD47K. However, it is safe to assume that these and other industry consortia continue to very actively work on revising the existing and issuing new guidelines and standards for SiC PECS. The JEDEC subcommittee JC-70.2 “SiC Power Electronic Conversion Semiconductor Standards” is actively working on documents for bipolar stability, gate oxide reliability, and HTRB. Historically, standards organizations have issued guidelines first, followed by standards. The advantage of this practice is that it is easier to first achieve broad consensus on guidelines, which can then serve as a foundational basis for aligning on standards, such as for qualification. Achieving broad alignment across manufacturers and customers is challenging but is essential for building confidence as SiC continues its impressive broad adoption into high reliability and high-volume applications.

Summary

The rapidly growing demand for SiC PECS devices in high reliability applications, in conjunction with high chip count, aggressive operating conditions and unique reliability considerations in SiC,

are resulting in a very high demand for thorough reliability characterization and industry consortia standardization. Key failure mechanisms in SiC including BTI, bipolar stability, and gate oxide (under gate bias and reverse bias) have been well characterized by manufacturers and other researchers. Good progress is being made on alignment on stress procedures, lifetime modeling and implications for field reliability. Several industry consortia have already issued a number of guidelines and standards, and many more are to come soon. The next challenge would be broader alignment between these consortia – much more work will be required and is on the near horizon.

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