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Impact of Bias Temperature Instabilities on the Performance of Power Electronics Employing SiC MOSFETs

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Abstract. In this work a reliability study of SiC power MOSFETs working as switching elements in a DC-DC Boost converter circuit is discussed. A critical parameter for a high-performance operation is the stable characteristics of the transistors employed. However, charge trapping effects such as bias temperature instabilities can affect e.g. the threshold voltage of transistors and thus lead to a variation in circuit behavior and efficiency. Furthermore, a time-dependent drift of the threshold voltage (ΔV_{th}) of the MOSFET over time can cause an increase of the on-resistance ($R_{\mathrm{DS(ON)}}$) too, and thus affect the static on-state power losses accordingly (P_{ON}). In this work, we use our physical reliability simulator Comphy to extract the threshold voltage drift of the transistor over time for various mission profiles for gate biases under device operation. Using the extracted ΔV_{th} values from the simulator, we can reproduce the measured behavior of the DC-DC boost converter circuit. With the calibrated toolset, we can obtain the ΔV_{th} values over a long operation time to predict the aged behavior of the circuit parameters employing Spice simulations, which could be beneficial for circuit design and lifetime prediction of the system.

Introduction

Power MOSFETs made from SiC are widely used in applications like motor drives, solar inverters, and charging stations for electric vehicles. These applications have something in common: they contain at least one DC-DC converter. Note that most complex electronic circuits employed in these systems are based on a few basic topologies, and their robust operation is key for long-term operational stability.

Most of the research has recently focused on the efficiency improvement of voltage converter circuits, and several power converter topologies for this purpose have been discussed [1–4]. However, literature reports usually lack reliability assessment for DC-DC power converters. Indeed, the reliability and efficiency of these converters directly impact the overall cost. Therefore, having more reliable converters means that the cost of maintenance and warranties of the system that involves power converters can be reduced.

One of the most dominant topologies is the so-called DC-DC Boost converter. To ensure a high power conversion efficiency and more reliable circuits, large carrier mobility, steep sub-threshold slope, and low on-resistance ($R_{\mathrm{DS(ON)}}$) are essential requirements from the transistors employed [5–10]. However, the transistor performance is severely affected by time-zero and time-dependent variability issues, which must be considered during circuit design. In this work, we analyze the impact of a time-dependent drift of the transistor threshold voltage (ΔV_{th}), i.e. well-known as bias temperature instability (BTI), on the performance of the Boost converter. We combine extensive experiments and physics-based computer simulations to replicate the experimental data. The decisive advantage of our approach is that with the calibrated tool set at hand, one can optimize the operating conditions towards low ΔV_{th} which finally maximizes the circuit's performance.

The schematic representation of the circuit includes a standard configuration of a synchronous boost converter, as shown in Fig. 1 (left). In this case, the circuit works in asynchronous mode using the freewheeling diode of the upper side transistor (UST), which always is in the OFF state (V_{g-U}=−4 V). The freewheeling diode ensures the current continuity into the output stage. We use our experimental setup shown in Fig. 1 (right) in this work. The device under test (DUT) is a commercially available SiC Power MOSFET C3M0075120K [11] fabricated by *Cree-Wolfspeed*.

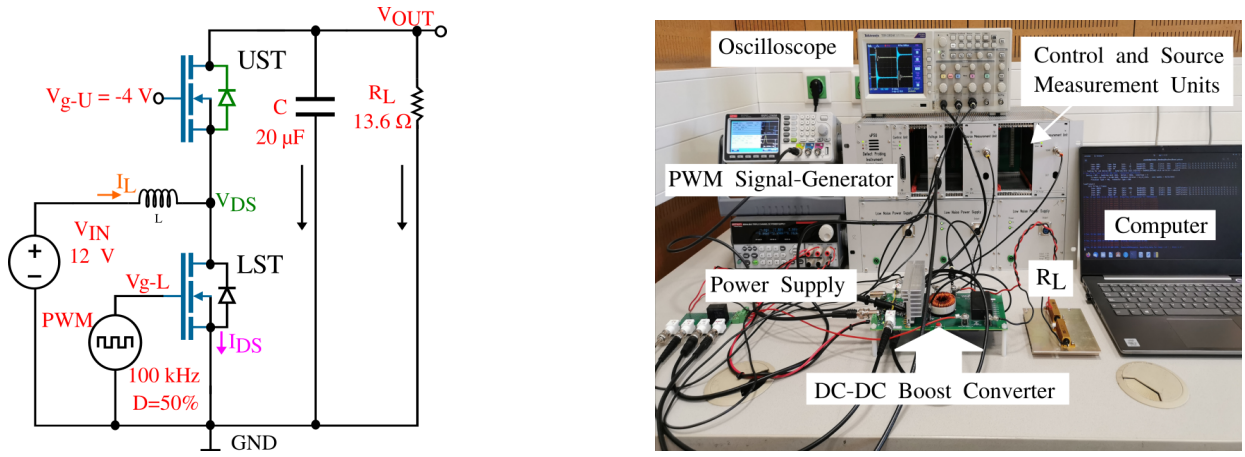

Fig. 1: Schematic representation of the Boost Converter circuit **(left)** and experimental setup for the reliability study made from general-purpose instruments and custom-made tools [12] **(right)**. The experiment is performed by setting V_{IN}=12 V, V_{OUT} ≈20 V, I_L=2.5 A, P_{OUT} ≈30 W, D≈50 % and switching frequency f_{SW}=100 kHz.

Setup Description

The measurement is performed during the power converter operation. In contrast, the power converter is interrupted to stress the lower-side transistor (LST). Measurement and stress phases are alternatively repeated following a known measure-stress-measure (MSM) technique. The switching from Boost converter operation (characterization) to stress mode and vice-versa is enabled using voltage-controlled relays. When the control signal of the relay is at Low level, the Lower-side gate voltage (V_{g-L}) is connected to the stress voltage (V_{Stress}=25 V), and the input voltage source is disconnected to ensure V_{DS} ≈100 mV. By setting V_{DS} closely to 0 we prevent undesired hot-carrier degradation-related effects and ensure a homogeneous carrier distribution along the channel at the oxide/semiconductor interface. On the other hand, when the control signal of the relay is at High-level, the stress phase is interrupted, V_{g-L} is connected to the PWM signal, and the input voltage connection is enabled, starting the characterization phase of the experiment. In this case, the transistors are not exposed to thermal stress due to the use of a heat sink, which keeps the operation temperature of the MOSFETs close to room temperature (30 °C). Both stress and characterization were performed using general-purpose instruments as well as custom-made tools [12].

Reliability Study and Charge Trapping Characterization

Although SiC devices show considerable potential for power electronics applications, the stability of these transistors is not yet comparable to that of conventional Si MOSFETs. Therefore, with increasing widespread use, the number of reliability studies on SiC devices has increased and move to the focus of research. Different die-level failure mechanisms of SiC power MOSFET have been reported recently, mainly due to time-dependent dielectric breakdown (TDDB), neutron-induced device breakdown, and avalanche breakdown, among others [13]. However, one of the most problematic reliability issues are threshold voltage degradation, gate-oxide degradation, and body diode degradation.

Threshold Voltage Degradation

Even though BTI has a negligible effect on the total switching losses [14], ΔV_{th} affects $R_{\text{DS(ON)}}$ and the static ON-state power loss (P_{ON}) of the MOSFETs. For this reason, it is crucial to account for a physical trapping model to predict the real behavior of ΔV_{th} over time to estimate the real P_{ON} during the ON-state operating time as accurately as possible.

It has been previously established that, the instability of the threshold voltage in SiC MOSFETs is due to oxide trap charging and its activation [15]. The oxide trap charging mainly occurs via a direct tunneling mechanism and structural relaxation at the defect site leading to a shift of the threshold voltage. The threshold voltage can be shifted in to both the negative and positive directions. A negative change is due to positive charges in the oxide traps resulting from electrons tunneling out of the oxide. On the other hand, a positive shift occurs when the back tunneling process neutralizes the positive oxide traps or charges neutral traps negatively in the oxide [16, 17]. A sizeable negative growth of the threshold voltage will result in device failure due to a significant increase in leakage current. Likewise, a large positive threshold voltage shift increases the device's on-resistance leading to failure of the circuit as well.

Our reliability study is divided into two steps:

(i) We extract ΔV_{th} using the physical charge trapping model implemented in our physical reliability simulator Comphy [18]. For this purpose, the trap distribution from Fig. 2 is used.

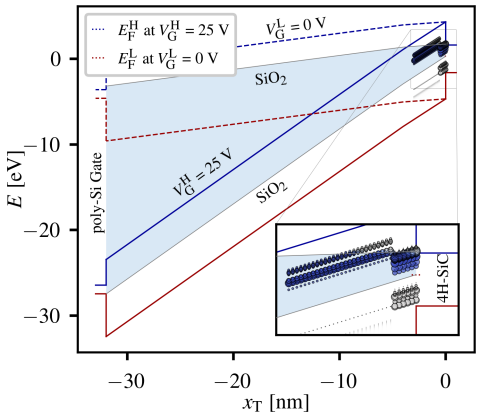

Fig. 2: Band diagram with the extracted trap levels. The Active Energy Region (AER) **(blue region)** for charge transitions are also shown. The identified traps are located in the AER, with two electron bands and one hole band.

Previous studies have observed that the SiC MOSFETs used in this work have a low concentration of donor-like defects in the lower half of the band gap. However, especially when considering PBTI, acceptor-like traps close to the conduction band have been identified [19]. The traps are located at a trap level of around E_T=2-3eV with respect to midgap and are spatially located in the oxide within a small distance (≈ 0.5 nm) from the SiC/SiO_2 interface [19]; see Fig. 2.

Comphy has been calibrated in extensive experimental studies considering DC and AC operating conditions [18, 19]. In our work, we consider an extended DC long-term measure-stress-measure (MSM) scheme, where a constant stress bias of 25 V is applied to the gate terminal of the transistor before the recovery phase is recorded [20]. Fig. 3 shows the excellent agreement between measurements and simulations for the extracted ΔV_{th} values over time. The defects in the Active Energy Region (AER), see Fig. 2, will change the device characteristics with time, leading to an according certain degradation of device performance.

(ii) We make use of NGSPICE simulations to consider ΔV_{th} within the SPICE model for the transistor to analyze the aging behavior of the DUT and the circuit parameters. The device manufacturer itself provides the SPICE model of the non-aged DUT. Each ΔV_{th} corresponds to a certain degradation with time and is considered by adapting a voltage source to the gate of the transistors [21, 22]. We analyze the impact of BTI on the circuit performance in three different cases: **A.** non-degraded, **B.**, and **C.**, stressing the DUT for 3 and 6 hours, respectively. For all the cases, we reproduce by simulation the observed behavior of the circuit as shown in Fig. 4 and 5.

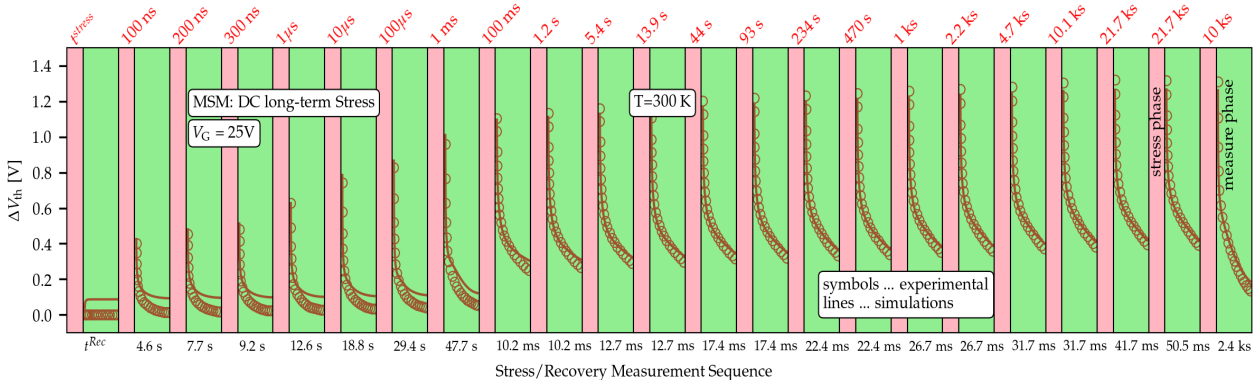

Fig. 3: Our physical reliability simulator can accurately reproduce the extracted ΔV_{th} values of the DUT over time. The extracted values can be used to enable a highly accurate analysis of the impact of BTI on the circuit performance considering a specific degradation over time.

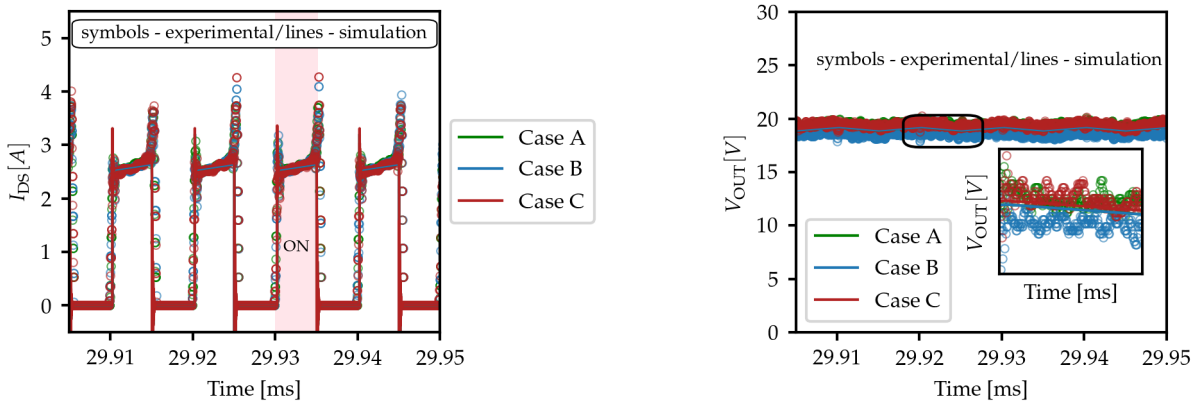

Fig. 4: Using the SPICE model of the DUT provided by *Cree*, we reproduce for all cases (A., B., and C.) the experimentally observed behavior of I_{DS} **(left)** and V_{OUT} **(right)** during the boost converter performance.

During ON-state operating time, $V_{\text{DS}}^{\text{ON}}$ drops to a higher value with time mainly due to an increase of $R_{\text{DS(ON)}}$, leading to a subsequent rise in P_{ON} according to Eq. 1:

$$P_{\text{ON}} = V_{\text{DS}}^{\text{ON}} \times I_{\text{DS}}^{\text{ON}} = [I_{\text{DS}}^{\text{ON}}]^2 \times R_{\text{DS(ON)}}. \tag{1}$$

At the same operating time, the impact of BTI on the MOSFET current (I_{DS}) can be neglected since I_{DS} will be determined by the current through the inductor (I_{L}). Therefore, considering I_{DS} as constant and extracting $V_{\text{DS}}^{\text{ON}}$ after each stress time, we can calculate and determine the $R_{\text{DS(ON)}}$ increase of the SiC MOSFET following Eq. 2:

$$R_{\text{DS(ON)}} = V_{\text{DS}}^{\text{ON}} / I_{\text{DS}}^{\text{ON}}. \tag{2}$$

Using the extracted ΔV_{th} values from Comphy, we reproduce by simulation the experimental $V_{\text{DS}}^{\text{ON}}$ behavior during circuit operation, as can be seen in Fig. 6.

Discussion of the Results

With the tool set calibrated, it is possible to estimate the aging behavior of the DUT over a long operating time, which is crucial to predict the system's lifetime. With the extracted ΔV_{th} distribution from Comphy for ten years of operating time, which is possible due to the thermal activation of charge trapping [23], we estimate the increase of $R_{\text{DS(ON)}}$ of the DUT due to the impact of BTI during boost converter operation, as shown in Fig. 7.

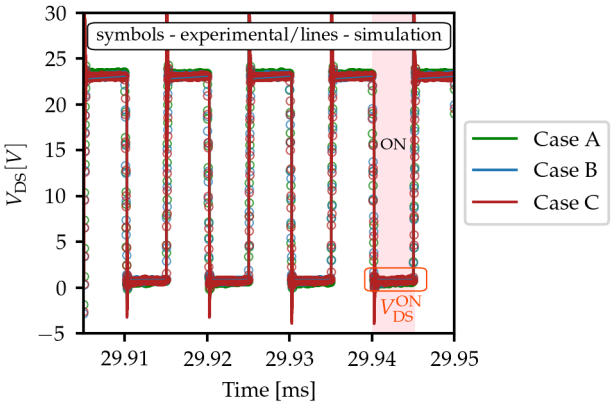

Fig. 5: With the extracted ΔV_{th} values from Comphy for the cases **A.**, **B.** and **C.** we reproduce the impact of BTI on the V_{DS} behavior of the DUT. We obtained an excellent agreement between simulations and experimental measurements, as expected.

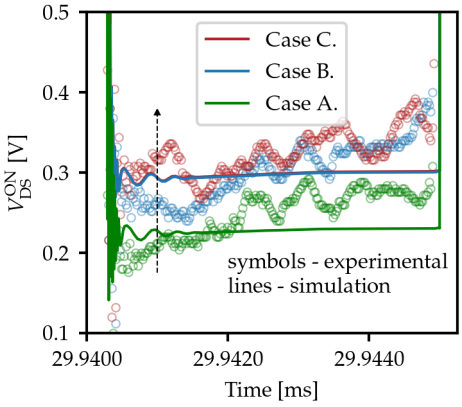

Fig. 6: During ON-state operating, BTI leads to a rise of $R_{DS(ON)}$, as I_{DS}=I_L at the same active time, the increase of the $R_{DS(ON)}$ is mainly due the addition of V_{DS}^{ON}. We reproduce by simulations the observed behavior of V_{DS}^{ON} considering the extracted ΔV_{th} values from Comphy for all the cases.

Finally, in Fig. 8, we quantify the impact of BTI on $R_{DS(ON)}$, P_{ON}, and junction temperature (T_J) of the DUT over ten years of operating time. T_J can be calculated using Eq. 3:

$$T_J = T_A + R_{\theta JA} \times P_{ON}, \tag{3}$$

where T_A and $R_{\theta JA}$ are the room temperature (25 °C) and the thermal resistance from junction to ambient (°C/W) extracted from the device's data-sheet, respectively.

The prediction of T_J could be beneficial for the design of a proper heat-sink for the DUT, which is critical for higher voltage applications (worst cases). On the other hand, for a given input power, with T_J another essential parameter estimation of the SiC power MOSFET is enabled, which is the junction to case thermal resistance (T_C). This parameter is vital for analyzing package failure mechanisms of the transistor [24].

Conclusions

We present a reliability study of a DC-DC boost converter circuit considering the impact of BTI on its switching element, a commercially available SiC power MOSFET. For this study, we calibrate our physical reliability simulator Comphy to estimate the time-dependent threshold voltage drift over a long operating time. With the tool set calibrated we reproduce the non-aged and aged circuit performance. Using SPICE simulations, we can use these values to determine the aging behavior of the MOSFET's electrical parameters to analyze the impact of BTI on the circuit's response with time.

From the analysis, we found that one of the most serious concerns related to BTI is the increase of power loss of the device. While BTI has no significant effect on the switching loss, the transistor performance causes an undesirable increase of the static ON-state loss (P_{ON}) due to a rise of the ON-resistance ($R_{DS(ON)}$).

An increase of the MOSFET static ON-state loss with time could increase the MOSFET junction temperature (T_J) accordingly. An accurate calculation of the junction temperature is crucial for the

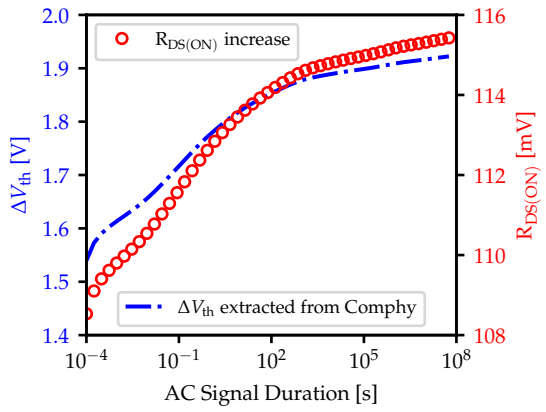

Fig. 7: We extract ΔV_{th} for a long operating time (ten years) to determine the ON-resistance increase over time as $R_{\text{DS(ON)}} = V_{\text{DS}}^{\text{ON}} / I_{\text{DS}}^{\text{ON}}$. Using the $R_{\text{DS(ON)}}$ change with time, we can analyze the aging behavior of the DUT during Boost Converter operation.

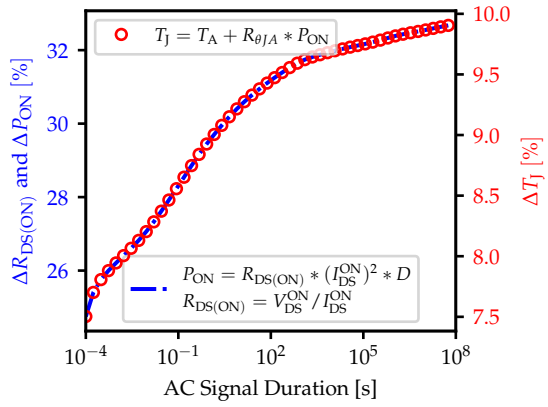

Fig. 8: Impact of BTI on $R_{\text{DS(ON)}}$, P_{ON} and junction temperature (T_{J}) of the DUT expressed in percent over long operating time. In the inset, we show the typical formulas to calculate these parameters. ΔV_{th} can reach values of up 2 V under real operating conditions, this leads to a rise of 30% and 10% for P_{ON} and T_{J}, respectively.

lifetime prediction of the system. Likewise, accurately estimating both ON-resistance and junction temperature over time could be very beneficial for designing a matching heat sink for the MOSFET. This is essential especially for higher voltage applications where the MOSFET could reach higher operating temperatures for which a proper heat sink and airflow dissipation play a vital role.

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