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Proven Power Cycling Reliability of Ohmic Annealing Free SiC Power Device Through the Use of SmartSiC™ Substrate

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Abstract. The Smart Cut™ technology enables the combination of a high quality single crystal SiC layer onto a low resistivity handle wafer (<5mOhm.cm), allowing device optimization as well as the reduction of device's conduction and switching losses. On this new SmartSiC™ substrate, the sheet resistance of the back side contact after metal deposition, without anneal, is about 10x lower than the annealed back side contact on 4H-SiC. Schottky-barrier vertical structures thinned down to 250µm were prepared for power cycling tests (PCT) measurements. Up to 250 k cycles, the devices remained within the specifications of AQG324 for samples prepared from SmartSiC™ substrates. We are demonstrating here that in addition to a higher current rating (up to 20%), the SmartSiC™ substrate enables a device fabrication simplification by skipping the annealing of the back-side ohmic contact, without compromising either the back-side contact resistance or the assembly PC_{sec} reliability.

Introduction

Power electronics based on Silicon Carbide (SiC) technology is now considered as a crucial key technology for the electrification of mobility and the efficient use of renewable energies. Despite continuous improvement in 4H-SiC material quality and supply, the availability of high quality wafers, enabling very high yields, is still inadequate.
The Smart Cut™ technology enables the integration of high quality SiC layer transfer for device yield optimization, combined with a low resistivity handle wafer (<5mOhm.cm) to improve device conduction and switching losses [1,3]. The SmartSiC™ engineered substrate is composed of a thin (between 350 and 800nm) high-quality 4H-SiC layer bonded (conductive bonding) on top of a 350µm thick polycrystalline SiC handle wafer.

Experimental conditions for back side ohmic contact

Metal/SiC contacts are generally non-ohmic after metal deposition due to the high Schottky barriers at the interface, resulting in a rectifying behavior. The most commonly used method to form an ohmic contact to SiC devices, mainly to contact a device from its back side, includes the deposition of a metal layer followed by an annealing (at approximately 1000°C) to induce a reaction of the metal with the SiC (i.e. with the formation of silicides, carbides, or ternary phases), with a consequent reduction of the barrier height or the barrier thickness [8]. For backside contacts, a laser annealing process is carried out after wafer thinning, at the end of the fabrication flow, in order to prevent unwanted alterations of the front side devices.
The polycrystalline SiC substrate has a nitrogen dopant concentration higher than the standard level of 4H-SiC. Due to this high N concentration, it is thought that, merely by depositing metal, ohmic

contact is obtained by means of a tunneling current, since the barrier between the metal and the semiconductor is thin.
In addition to forming an ohmic contact, the annealing modifies the adhesion of the metal on the back side, and hence improves the reliability of the die attach stack inside the power module. A proper anneal will improve the mechanical strength of the interface, while a poorly tuned anneal may result in graphitization and subsequent peeling of the metal. "Polytec Model 333A" four-point probe mapping system from "Four Dimensions Inc." was used to measure the metal sheet resistance.

Results of ohmic contacts on the substrate back side.

In the case of 4H-SiC substrate, we measured an expected sheet resistance mean value of 10.02 Ω/sq on 70 nm as-deposited $NiAl_{2.6\%}$. By annealing at different energies based on results from [4], we created homogenous ohmic contacts at energies of 2.4 J/cm² and above with a sheet resistance between 0.39 and 0.43 Ω/sq: see fig.1a and 1b.

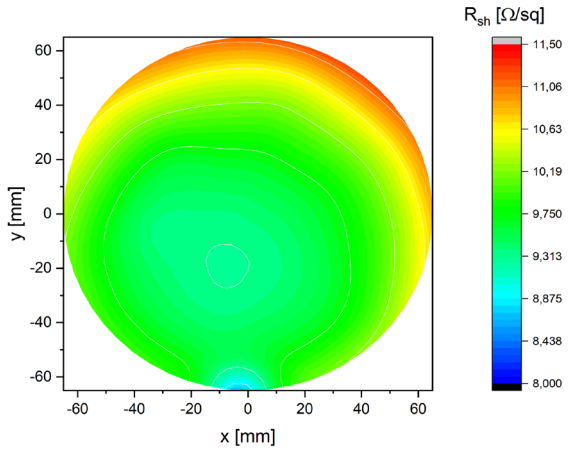


Fig. 1a: Sheet resistance of 70 nm NiAl2.6% on 4H-SiC substrate as-deposited with 225 data points measured.

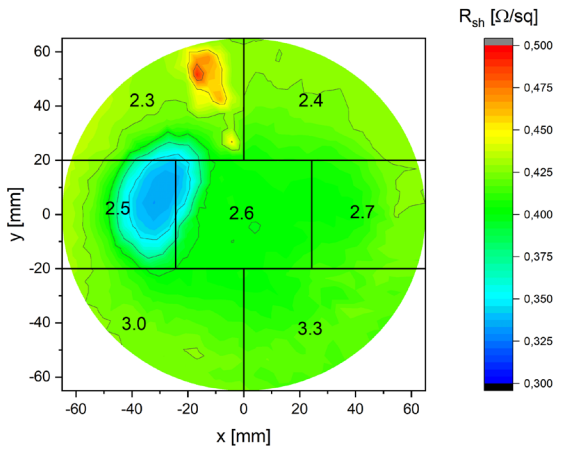


Fig. 2b: Sheet resistance of laser annealed 70 nm NiSi on 4H-SiC substrate with different laser energies, ranging from 2.3 – 3.3 J/cm² and a non-annealed area with 625 data points measured.

Table 1 shows the different sheet resistance values after laser annealing of $NiAl_{2.6\%}$ on 4H-SiC, creating a NiSi/4H-SiC ohmic contact, with an overall average Rsh of 0.41 Ω/sq.

Table 1: Mean sheet resistances and relative standard deviation for different laser energies on 4H-SiC substrate.

Laser energy [J/cm²]	2.3	2.4	2.5	2.6	2.7	3.0	3.3
Mean R_{sh}[Ω/sq]	0.430	0.424	0.393	0.398	0.416	0.419	0.415
σ/mean [%]	3.86	1.03	9.32	3.93	1.88	1.51	1.09

On the highly doped polycrystalline SiC, the initial sheet resistance after $NiAl_{2.6\%}$ deposition with an average value of 0.045 Ω/sq, was very significantly lower (over 200x) than non-annealed $NiAl_{2.6\%}$/4H-SiC and about 10x lower than the annealed NiSi/4H-SiC sheet resistances. This led to the assumption of having an ultra low ohmic contact resistance between metallization and polycrystalline SiC after deposition. Laser energy was explored to assess a wider spectrum of energies.

As shown in figure 2a and 2b, laser annealing with energies from 1.2 – 3.3 J/cm² did not influence the measured Rsh values on polycrystalline SiC wafers and the average sheet resistance remained unchanged compared to as-deposited $NiAl_{2.6\%}$/PolySiC and 10x lower than annealed ohmic contact on 4H-SiC.

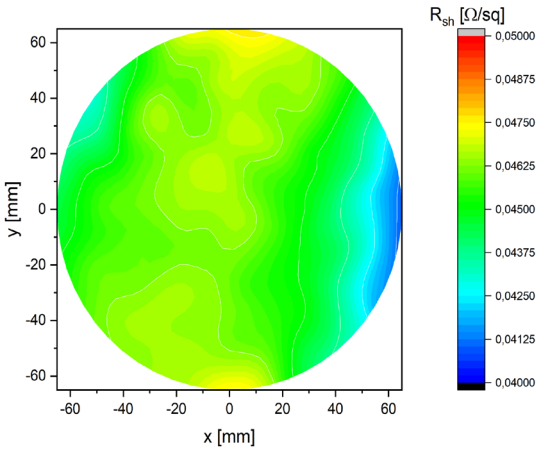


Fig. 2a: Sheet resistance of as-deposited 70 nm NiAl2.6% on polycrystalline SiC substrate.

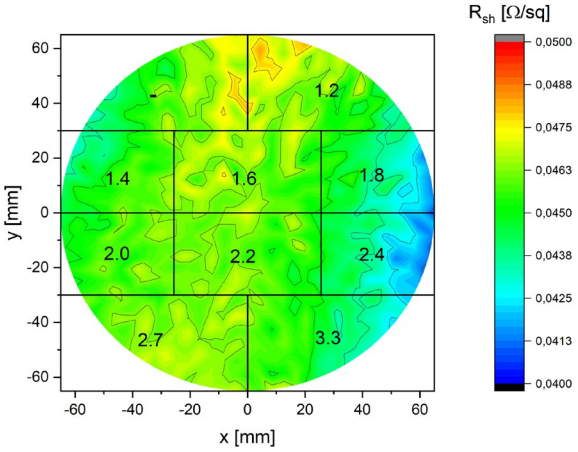


Fig. 2b: Sheet resistance of laser annealed 70 nm NiAl2.6% on polycrystalline SiC substrate with different laser energies, ranging from 1.2 – 3.3 J/cm² and a non-annealed area.

The sheet resistance results for every laser energy zone used on PolySiC wafers are shown in table 2.

Table 2: Mean sheet resistances and relative standard deviation for different laser energies on PolySiC substrate.

Laser energy [J/cm²]	-	1.2	1.4	1.6	1.8	2.0	2.2	2.4	2.7	3.3
Mean Rsh [Ω/sq]	0.042	0.044	0.043	0.045	0.046	0.045	0.046	0.046	0.045	0.044
σ/mean [%]	2.36	1.84	2.00	1.62	1.11	1.40	1.02	1.13	1.18	1.57

These results lead to the conclusion that after $NiAl_{2.6\%}$ deposition on polycrystalline SiC, the metal semiconductor barrier is already low enough to neglect the contact resistance in comparison to the measured sheet resistance of the polycrystalline substrate. In contrast to 4H-SiC an annealing step for ohmic contact creation does not seem to be required.

Experimental conditions for die assembly and power cycling assessment

In order to assess the reliability of devices fabricated on SmartSiC™ substrates, reliability testing according to AQG 324 [2] was used with the objective to generate targeted stress situations in a power electronic device under strongly accelerated conditions using QL-01 power cycling (PCsec). By limiting the t_{on} (on-time of the load current) to a value of ton < 5s, the test exerts targeted stress on the chip – near interconnections (die-attach and top side) and any other structure within the chip itself – thus studying the potential impact of SmartSiC™ materials properties in a conventional module setup (see Fig. 3).

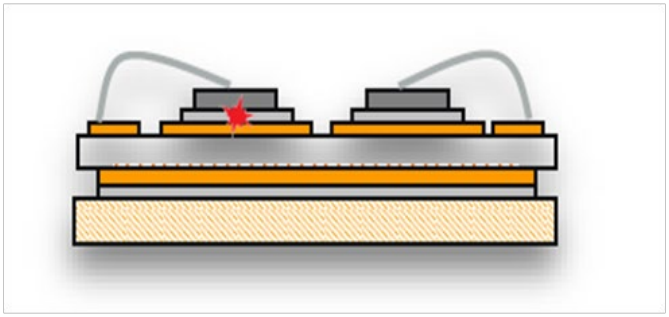


Fig. 3: Schematics of conventional setup of power modules used for the AQG324 PCsec test [2] and the expected location of failures close to the chip marked red (from ECPE training by A. Schletz).

Current is injected in the devices under test (DUT) through a Schottky contact built on the top side of the substrate. These Schottky contacts act as semiconductor junctions used for heating and temperature sensing within the power cycling test. After thinning down to 250µm, a sinterable metal stack was deposited on NiSi/4H-SiC and $NiAl_{2.6\%}$/PolySiC respectively. The NiSi/4H-SiC contact was laser annealed (see previous paragraph for details), $NiAl_{2.6\%}$/PolySiC was not annealed.

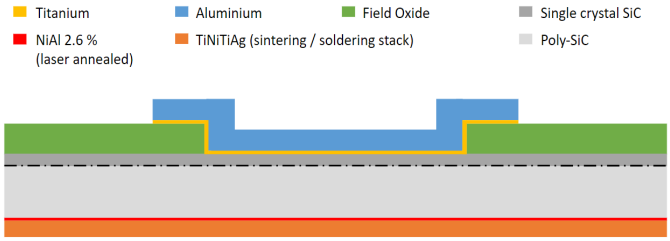


Fig. 4: Schematics of Schottky-Contact on SiC devices used for reliability testing.

Substrates were diced into individual chips of 5mm x 10mm. DUTs are mounted onto conventional DCB-substrates by silver-sintering with jetted sinter-paste. The top-side contact is connected through multiple Al bond wires with a diameter of 125 micrometer [6] (see Fig. 5 and 6).

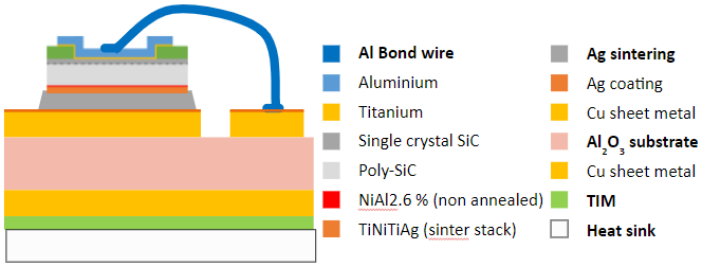


Fig. 5: Schematics of Schottky-Contact on SiC devices, Ag sintered to DBC substrate.

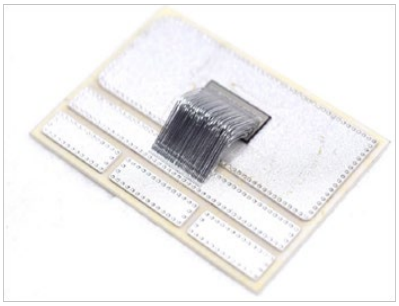


Fig. 6: Silver-sintered on DCB with silver surface; top-side contact by 125um Aluminum bond wires

The active power cycling tests were performed to compare the lifetime of the SmartSiC™ substrate (using a low resistivity wafer as a handle) compared to standard SiC reference using a well-validated setup [5, 7].

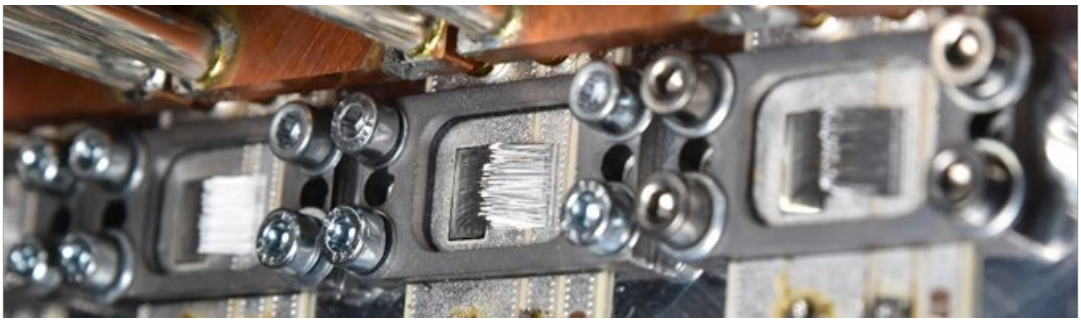


Fig. 7: Mounting on heatsink for direct cooling of backside of DCB-substrate.

The DUTs are mounted to a water-cooled Aluminum heatsink (see Fig. 7) with coolant temperature of 40°C. The backsides (opposite to the sintered chip) of each individual DCB-substrate are direct-cooled by water-glycol coolant, thus eliminating the implications of aging of thermal interface material during the lifetime testing and thermal characterization. Calibration of a typical device voltage drop at a given low current (30mA, to avoid self heating) at various temperatures allows for direct measurement of junction temperature of the device under test. The Power Cycling (PC) test is designed to characterize the lifetime of the semiconductor itself using short cycles (PCsec) with 3 seconds heating (t_{on}) and 6 seconds cooling (t_{off}) with a temperature swing ΔT targeting 120 K: see Fig. 8.

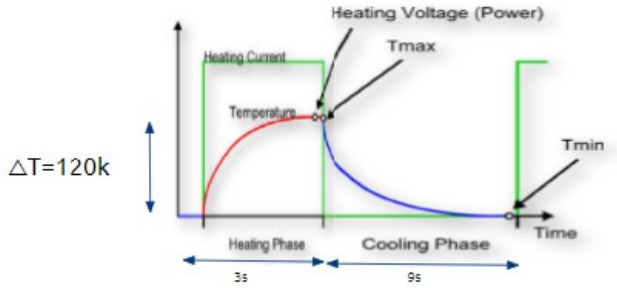
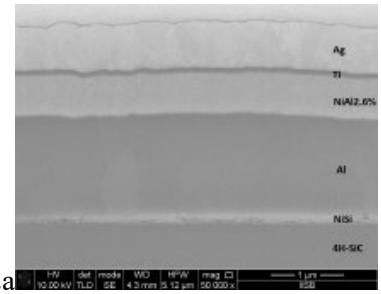


Fig. 8: Schematic of typical Heating and Cooling Cycling within active power cycling PCsec test.

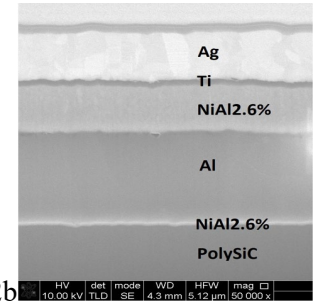
Results for Assembly and Power Cycling

Schottky barrier vertical structures thinned down to 250µm were prepared for PCT measurements. Figures 9a & b show SEM images of these metal stacks after FIB cross-sections.



2a

Fig. 9a: FIB cross-section of a sinterable metal stack on laser-annealed NiSi on 4H-SiC.



2b

Fig. 9b: FIB cross-section of a sinterable metal stack on as-deposited $NiAl_{2.6\%}$ on PolySiC.

The material characteristics of the SmartSiC™ translates into a forward resistance of the Schottky-contact mounted diodes at 200A (curve tracer Agilent B1505), significantly lower with regards to the conventional 4H-SiC. The comparison of the ohmic contribution to the forward resistance derived by fitting of the differential resistance in the conductive regime exhibits 1.9 mOhm for the Standard SiC and 0.8 mOhm for the SmartSiC™. (see Fig. 10)

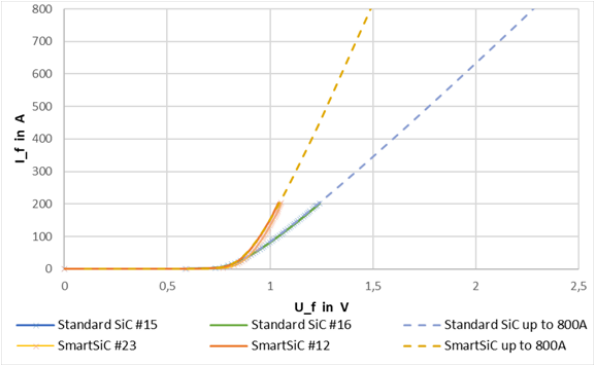


Fig. 10: Forward resistance and differential forward resistance of Standard SiC and SmartSiC™

The mounted Schottky contact dies during the heating phase of the power cycling test exhibits a voltage drop in our configurations of typically 1V yielding a temperature swing ΔT of 120 K with a heating current of 138A for the Standard SiC material (with $U_{heating}$ of typ. 0.92V), whereas the SmartSiC™ wafer required a heating current of 146 A (with $U_{heating}$ of typ. 0.83V) to achieve the same temperature swing.

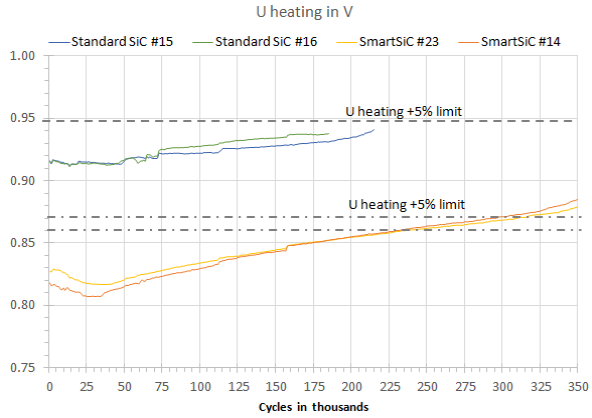


Fig. 11a Left: Evolution of voltage drop (U) of standard 4H-SiC and SmartSiC™ samples.

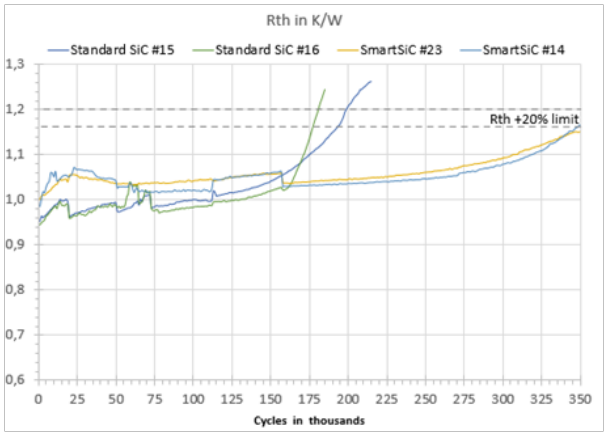


Fig. 11b Right: Evolution of thermal resistance (Rth) of standard 4H-SiC and SmartSiC™ samples. AQG324 limits are shown.

PC_{sec} has been validated up to 350k cycles (fig.11a & b) at least for 10 samples prepared from 2 different SmartSiC™ substrates. All SmartSiC™ devices are within the specifications of AQG324 standards (2021 revision): drift of Rth and Tmax below 20%, drift of voltage drop below 5% up to 250k Cycles. In parallel we have observed earlier Rth failures (between 174k and 187k cycles) for reference samples prepared on 4H-SiC. It shall be mentioned that those reference samples exhibit the same aging with respect to U_heating, but fail earlier due to accelerated degradation of the thermal resistance. This will require further investigations and failures analysis.

Summary

As a conclusion, we are demonstrating here that in addition to a higher current rating (up to 20% as already published [2,3]), the SmartSiC™ substrate is enabling a device fabrication simplification by skipping the ohmic contact annealing without compromising either the backside contact resistance, or the assembly PCsec reliability. This evaluation has been pushed to 350k cycles with a temperature swing of 120K. All SmartSiC™ devices are within the specifications of AQG324 standards (2021 revision: drift of Rth and Tmax below 20%, drift of voltage drop below 5%) up to 250k Cycles.

Acknowledgments

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