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SmartSiCTM Substrates: A Boon to Drain Metallization Process

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Keywords: Silicon Carbide (SiC) Epitaxy, SmartSiC^{TM} substrate, Schottky Barrier Diodes (SBDs) material characterization, ohmic metallization, contact resistivity.

Abstract. We present results of epitaxial characterization and benchmarking of Silicon Carbide (SiC) epitaxial layers grown on both 6-inch commercially available SiC substrate and on SOITEC's new generation SmartSiC^{TM} substrate. Multi wafer reactor was utilized to avoid run-to-run variation. Schottky Barrier Diodes (SBD) and electrical test vehicles were fabricated to extract ideality factor, barrier height and ohmic contact resistance for benchmarking.

Introduction

Silicon carbide (SiC) is becoming the front runner in the advancement of the power electronic devices. It has enabled a game-changing generation of power devices with superior performance as compared to traditional Si-based devices [1]. This is due to its outstanding physical properties such as wide bandgap (E_g), high saturation velocity (v_{sat}), high thermal conductivity (k), and high critical electrical field (E_c) that push forward the limits reached by Si-based power electronics (Fig.1)[2]. Formation of ohmic contacts with low contact resistivity is one of the key factors and should be low enough (<1% of the total resistance between two main terminals) to improve device performance and decrease the cost.

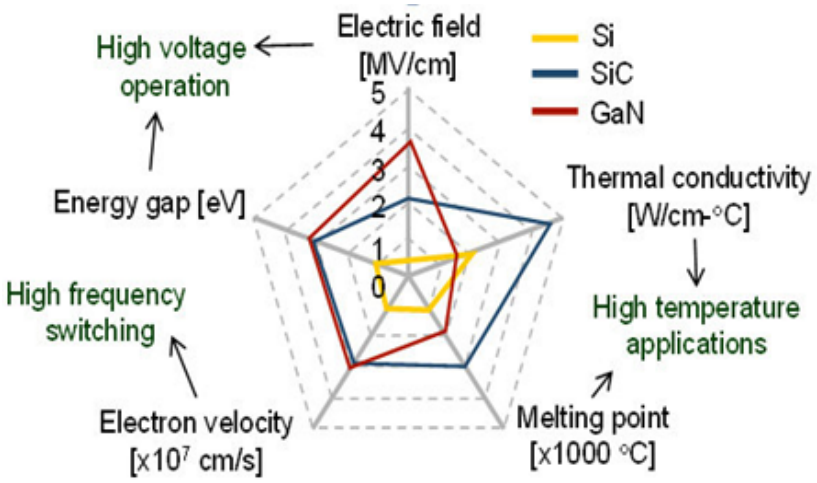

Fig. 1. Relevant material properties of Si, GaN & SiC[2].

The SiC substrate is the single largest contributor to the cost of power devices. Fig.2 shows the cost breakdown for a SiC power MOSFET for a commercial 1200V/100A device produced on 6-inch substrates [4], which needs to be decreased. Moreover, the doping in single crystal SiC ingots is an order of magnitude lower than the solid solubility limits of nitrogen in SiC, which keeps substrate resistivity high (≥15 mΩ-cm).

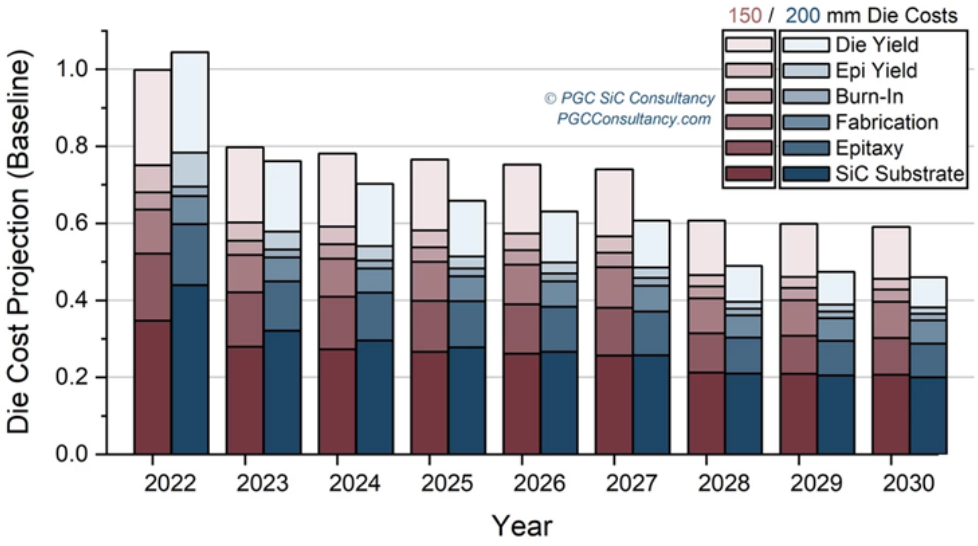

Fig. 2. SiC die cost projections [4].

Soitec's SmartSiC™ technology enables the engineering of SiC substrates, providing prime quality 0.6 µm single-crystal 4H-SiC transferred on a 350 µm polycrystalline SiC substrate. Due to its low resistivity (< 5 mΩ-cm), this poly-crystalline SiC (pSiC) substrate enables enhanced performance by improving it's conducting properties and decreasing switching losses [5]. Another beneficial features of pSiC substrates are lower bandgap and higher carrier concentration (> 10^{20}cm^{-3}) which serves a lower barrier height compared to single crystal SiC substrate and promotes Field Emission (FE) which results in lower contact resistance.

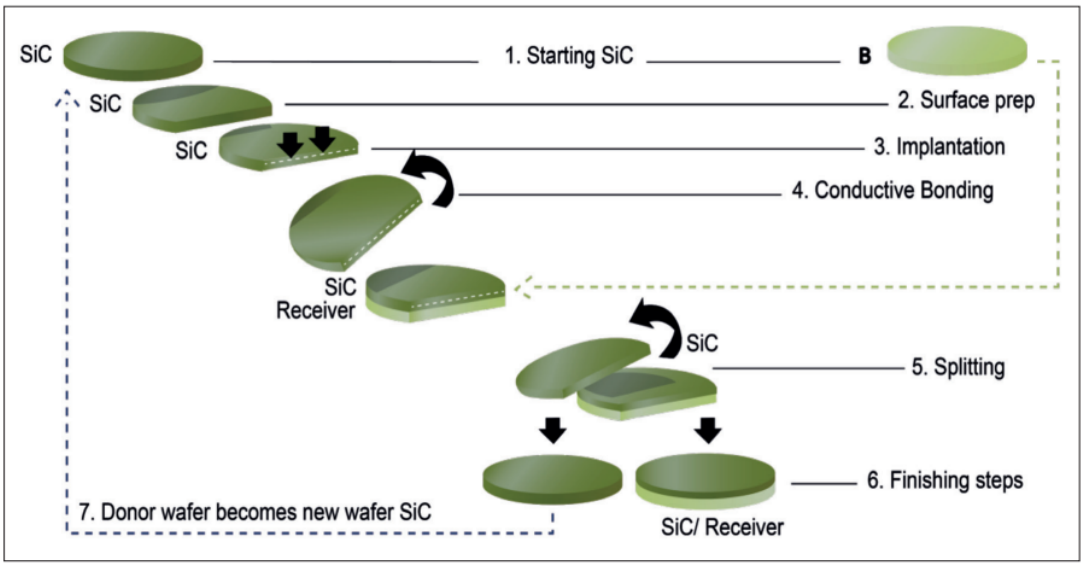

Fig. 3. Smart Cut process schematics for engineered SiC substrates

Experimental

In this paper, Soitec's new generation SmartSiC™ substrates have been used for epitaxial growth. The SiC epi-stack comprises 1µm of the buffer layer and 12µm of the drift layer with doping of

$1\times10^{18}cm^{-3}$ and $0.9\times10^{16}cm^{-3}$, respectively. All SiC epi-wafer were grown in a single run using multi-wafer CVD reactor to avoid run-to-run deviation in epilayer quality. Commercially available production-grade SiC substrates were used for comparison as shown Fig.4., below.

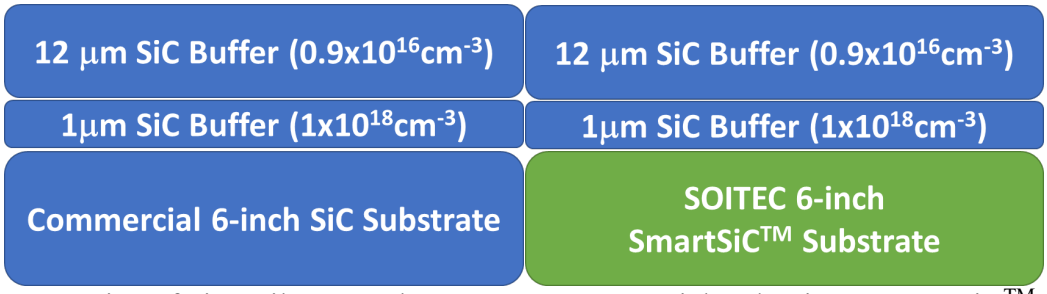

Fig. 4. Cross-section of SiC epilayer stacks grown on commercial and Soitec's SmartSiC™ substrates

Epitaxial growth, presented here, were performed in a RF-heated reactor temperature between 1600ºC and 1700ºC. Hydrogen serves as carrier gas, silane and propane are the reactive gas precursors, while nitrogen was used as n-dopant. Epitaxial growth took place at ~100 mbar. The deposition rates range from 9 to 16 μm/h. Commercially available (0001)-oriented Si-face n-type 4H SiC wafers with a 4° off-orientation towards the <11-20> direction were used as substrates. SBD were fabricated using Ti and Al as a Schottky metal deposited by sputtering. Cox-Stract method utilized to extract ohmic contact resistivity.

Results and Discussion

Hg-probe and Fourier-transform infrared spectroscopy (FTIR) measurements revealed that SiC epitaxy on Soitec's SmartSiC™ substrates exhibited excellent [6] doping and thickness uniformities (σ/μ) ≤3.3% and ≤1.0%, respectively. Differences in FTIR thickness measurement were also observed and attributed to the distinct transparencies of SmartSiC™ substrates. Wafers were then diced into $16\times16mm^2$ pieces for further analysis and test vehicle processing. Scanning electron microscopy (SEM) cross-sections analysis were conducted to validate FTIR thickness measurement by using an in-lens detector to capture the contrast of different doping regions. The epilayer thicknesses were almost the same for all samples and around 12.1μm. Atomic force microscope (AFM) measurements were performed on a surface of $5\times5\ \mu m^2$ for surface roughness and RMS values were below 0.3 nm for all samples

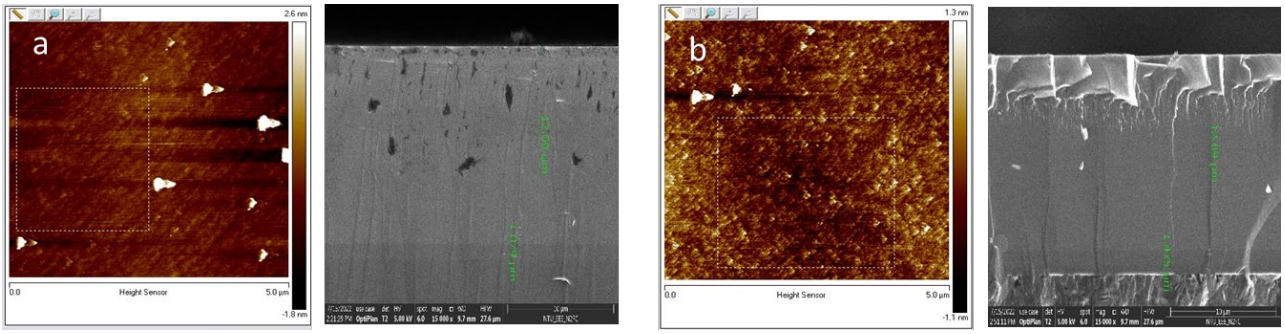

Fig. 5. AFM & SEM Cross-section of SiC epilayer stacks grown on commercial (a) and SOITEC 6-inch SmartSiC™ substrate (b).

Schottky barrier diodes (SBD) have been fabricated on 16×16 mm2 coupon samples. Ti/Al metals were used for Schottky metal contacts and Al, Ti and Ni were used for non-alloyed ohmic contacts. Fig.5 shows almost 2-order of magnitude increase in the forward current density (J_f) for SBDs fabricated on SmartSiC™ substrates compared to the commercial substrates which is attributed to very low ohmic contact resistances (ρ_c). By the time of the conference, modelling and experimental methodology will confirm low ρc already observed and attributed to high doping of polycrystalline SiC handle wafer, in agreement with reported values by E.Guiot[7].

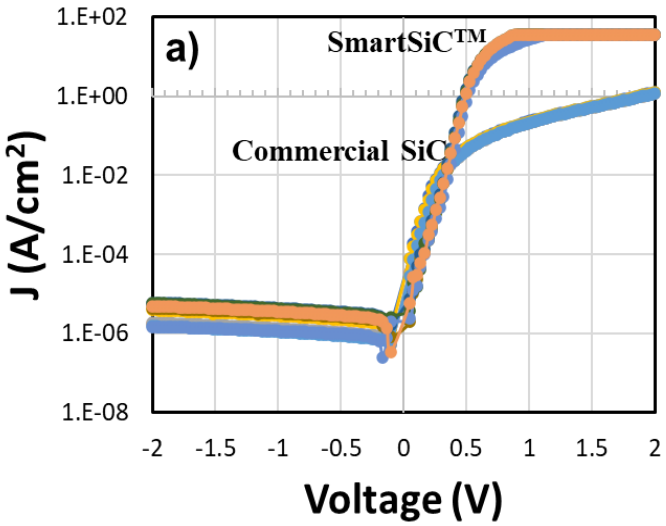

Fig. 5. a) J-V characteristics of fabricated SBDs on SmartSiC™ and commercial substrates

Ideality factors and Schottky barrier heights of the fabricated SBDs on SmartSiC™ substrates were tabulated in Table_1. Similar epilayer and surface properties observed for SiC epitaxial layer grown on SmartSiC™ and engineered substrates.

Table 1. Barrier height and the ideality factor of the fabricated SBDs on SmartSiC™ and commercial SiC substrates

	Schottky Metal	Ideality Factor (h)	Schottky Barrier Height (eV)
SBD on SmartSiC™ subst.	Ti/Al	1.1	0.75
		1.17	0.72
SBD on commercial SiC subst.		1.2	0.73

Specific contact resistivity of the non-alloyed ohmic contact to SmartSiC™ substrates extracted by using C_{ox}-Strack method. The extracted value of ρ_c is $2.0E^{-4}$ Ωcm^2 for SmartSiC™ substrates without annealing, as shown Fig.6 (b)., below. A benchmarking of the specific contact resistivities obtained at different annealing conditions is shown in the Fig.6 (c)., below.

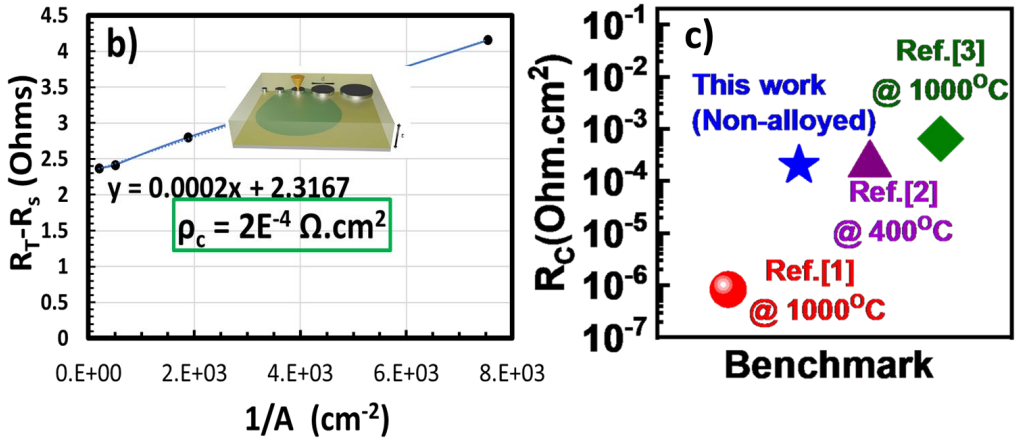

Fig. 5. Specific contact resistivity extracted by C_{ox}-Stract method (b) and Benchmarking plot of R_c (c).

Summary

The SmartSiC™ substrate exhibited similar SiC epilayer quality (thickness uniformity &doping uniformitiy) as compared to the conventional SiC substrates. Moreover, similar defect profiles were obtained for both substrates. Higher J_f for SBDs fabricated on SmartSiC^{TM} substrates attributed to the very low ohmic contact resistance obtained for non-alloyed Al contact to p-SiC substrate. Non-alloyed ohmic contacts to p-SiC substrate is paving the path for non-alloyed ohmic contact technology by skipping high cost and risky laser and thermal annealing processes

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