HYPREZ Wafering Solutions: A Novel Approach of SiC Wafering Solution

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Abstract A novel approach for processing SiC wafers has been developed to grind then polish 150 and 200mm SiC wafers without lapping. The purpose of this work was to optimize the processing of SiC wafers sliced from boules to finished epi-ready wafers by grinding and chemical-mechanical polishing (CMP). Diamond vitrified wheels were used for coarse and fine grinding to correct the irregular shape of SiC wafers before reducing surface roughness by CMP. 4H-SiC wafers were sliced by diamond embedded/slurry wire saw and laser split techniques. Incoming wafer condition was seen to affect coarse grinding wheel performance depending on incoming surface roughness and shape. Wheel characteristics, including abrasive size, abrasive concentration, and bond structure, were adjusted to improve grinding efficiency based on incoming conditions. Coarse grinding wheels were able to reduce wafer total thickness variation to 3-5um and average surface roughness to 20-30nm (Ra). Fine grinding wheels were optimized to reduce total thickness variation (TTV) below 2um and surface roughness to 1-2nm Ra and peak-to-valley height of 20-30nm (Rt). Coarse and fine wafering time was less than 30 minutes total to remove 50 microns on both Si and C-face per wafer. Surface damage from grinding was removed after one hour of polishing each wafer by CMP, achieving surface roughness of 0.4nm Ra and 5-7nm Rt. The benefit of optimizing coarse and fine grinding of 150 and 200mm SiC wafers is demonstrated by producing flat wafers, which reduced overall processing time to prepare an epi-ready condition by CMP.

Introduction

Semiconductor devices made using silicon carbide (SiC) instead of silicon substrates for applications in high-power devices or extreme environments are well documented and require high quality wafers with low flatness [[1]-[5]]. The challenges of processing SiC compared to silicon wafers are also well known and need to be addressed to reduce the substantial manufacturing cost from wafering steps [[6], [7]]. In addition to the inherent challenges of SiC material characteristics, the variety of manufacturing technology used to process SiC wafers before planarization introduces quality variation. Characteristics attributed to incoming wafer quality, including wafer size, shape, and surface condition, vary depending on the method of wafer slicing, such as wire saw or laser split [[8]-[11]. Traditional methods of planarization by mechanical and chemical-mechanical means are widely used to process and finish sliced wafers [12]-[13]. These methods require high stock removal by lapping to flatten wafers, followed by CMP to remove surface damage creating an epi-ready surface. Despite current diamond lapping methods achieving low surface roughness, which helps to reduce CMP process time, they do not easily flatten SiC wafers and still require long polishing times for planarization [14][19].

Engis, a world leader in superabrasive finishing systems, builds and services machines to be used with HYPREZ® accessories and consumables, including the newest offering of 'Grind-to-CMP' total solution for SiC wafers. Engis has previously demonstrated the capability of fine HYGRIND wheels to remove coarse grinding surface damage and improve wafer flatness on 150mm SiC with reduced processing time [20]. Engis has also demonstrated CMP solutions for 50mm SiC after fine grinding to achieve epi-ready surfaces. The objective of this work was to reduce CMP process time of 150mm

4H-SiC wafers by reducing wafer thickness variation and surface roughness before CMP through grinding with HYPREZ wafering solution. However, incoming wafer surface condition was found to affect wheel performance, so HYGRIND wheels were optimized based on performance of baseline coarse and fine wheels grinding SiC wafers of 150 to 200mm sliced by wire saw and laser split methods. HYGRIND wheels offer this unique benefit compared to resin or metal bond wheels by optimizing the vitrified structure to improve cutting ability of varying surface conditions. The hard but brittle glass bond structure allows coarse wheels to break down, effectively self-dressing, and fine wheels to hold #30,000 grit size abrasive. The effect of wheel characteristics, such as abrasive size and bond structure, on grinding performance indicators were investigated by evaluating grind ratio, wafer total thickness variation, and grind force with different incoming SiC wafer conditions. Then, 150mm SiC wafers planarized by HYPREZ grinding wheels were polished by HYPREZ CMP to investigate the effect of reducing wafer thickness variation and improved CMP processing time. CMP performance was evaluated by processing time required to completely remove surface damage from wafers and achieve epi-ready surface condition on 150mm 4H-SiC.

Experimental Methods

SiC wafers of 150 to 200mm size were ground using the Engis EAG grinder shown in Fig. 1 below with coarse and fine HYGRIND wheels. HYPREZ EAG-28DANX is a fully automated cassette-to-cassette handling, dual-spindle grinding system based on a single chuck design. It utilizes a confocal optical sensor to measure wafer thickness before, during, and after grinding. Wafers were also measured by contact gauges before and after grinding to verify non-contact measurements. Wheel wear was measured by tracking the amount of work required by the wheel to remove the corresponding target amount from wafers as wheel depth with <1um accuracy. Grind ratio was evaluated by comparing material removal from the wafer before and after grinding to the amount of work as wheel wear (1).

$$Grind - ratio = \frac{Volume \text{ of wafer removed (microns)}}{Volume \text{ of work amount (microns)}}$$
(1)

Grinding load force was observed as torque resistance experienced by the grinding wheel as a percentage of the rated spindle power, 9.5kW. Wafer shape and true thickness were measured by FRT with CWL sensor for total and local thickness variation. Surface roughness average (Ra) and total peak-to-valley (Rt) were measured before and after grinding by Zygo NewView 6300 optical profilometer.

The Engis EJW-610 CMP machine was used to polish 150mm SiC wafers with HYPREZ M900 pad and PA2014 slurry in Fig. 1. After polishing, a contact gauge was used to measure thickness variation and general flatness. Wafers were weighed before and after polishing since removal rates were within the tolerance of contact gauge accuracy, +/- 1um. Surface roughness was also measured by Zygo optical profilometer.



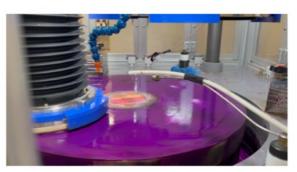


Fig. 1. HYPREZ EAG-28DANX dual spindle, cassette-to-cassette wafering system for 150 to 200mm SiC and EJW-610 CMP machine with HYPREZ SiC pad and slurry.

Results and Discussion

SiC wafers from 150 to 200mm were planarized by HYPREZ grinding wheels on an EAG-28DANX, then polished by CMP to epi-ready surface condition. Performance of HYGRIND wheels is summarized in Table 1. The average total cycle time to remove 50 microns on both Si and C-face by grinding was 30 minutes with removal rates of ~10um/minute by coarse wheels and ~1um/minute by fine wheels. This compares to traditional planarization by lapping, with removal rates from 1 to 15um/minute; however, the shape of wafers processed by HYPREZ fine grinding was improved with global TTV <1um, as seen in Fig. 2, compared to literature values of 2-4um [15],[18], [19]. Surface roughness was ~20nm Ra by coarse grinding and 1-2nm Ra by fine grinding as shown by Fig. 3. Wheel performance was evaluated by comparing grind ratio and wheel load. Coarse wheels were found to have average grind ratios of 3 to 5 while fine wheels had 0.5. This performance indicates that approximately 3 to 5um of a 150mm wafer can be removed per 1um of a coarse wheel and 1um of a wafer can be removed per 2um of a fine wheel. Wheel load was stable for both coarse and fine wheels, ~15% for coarse and ~10% for fine, shown in Fig. 4. Performance indicators for process of record HYPREZ grinding wheels are comparatively worse when grinding 150mm 4H-SiC with lower grind ratios of 2-3 for coarse and 0.1-0.3 for fine while grinding load was higher overall with ~20% for coarse and ~12% [20]. HYPREZ grinding wheel performance was also evaluated on 200mm SiC and shown to be stable, although grind ratio decreased for both GV135 and GV562.

The surface condition of incoming wafers was seen to vary greatly depending on the slicing method used and had a large effect on grinding performance. Wafers sliced by multi-wire saw had visually smooth surfaces but high bow and warp, 50 to 100um of thickness variation and 100 to 300nm Ra [8]. This was contrasted by laser split wafers, which had more uniform thickness, varying within 10um, but highly interrupted surfaces with over 2000nm Sa [9][11]. The HYPREZ coarse wheel, GV135, was used to grind both laser split and wire saw surfaces to establish the baseline. Then, wheels with slightly different characteristics were used to grind laser split or wire saw surface and observe any effects of incoming condition by comparing the grinding performance of wheels. HYPREZ wheels GV140 and GV121 were adjusted to act harder and softer, respectively; GV140 was used to grind laser split surfaces while GV121 used to grind wire saw surfaces. The grind ratio of GV135 reduced from 5 when grinding wire saw surfaces to below 2 when grinding laser split surfaces and wheel load remained similar. Laser split surface grinding performance was affected by increasing wheel hardness, giving GV140 a grind ratio over 2 compared to GV135 with similar wheel load. Wire saw surface grinding performance was affected by decreasing wheel hardness, giving GV121 a grind ratio of 1 compared to GV135, but GV121 wheel load was 50% lower than GV135. Increasing grind ratio of coarse wheels has the obvious benefit of better grinding efficiency, but managing wheel load is also important to reduce thickness variation wafer to wafer which reduces the amount of material required to be removed by fine grinding.

Table 1. HYGRIND Wheel Performance Grinding 150 to 200mm SiC Wafers

Process			Coarse				Fine	
Wheel	GV140	GV121	GV135	GV135	GV135	GV531	GV562	GV562
Wafer Size [mm]	150	150	150	150	200	150	150	200
Incoming Wafer Surface	Laser Split	Wire Saw	Wire Saw	Laser Split	Wire Saw	Coarse Grind	Coarse Grind	Coarse Grind
Grind Ratio	2.2	1.0	5.1	1.8	2.2	1.0	0.6	0.5
TTV [um]	4	4	3	-	5	1	1	3
Grind Load	16%	8%	16%	13%	15%	8%	11%	13%

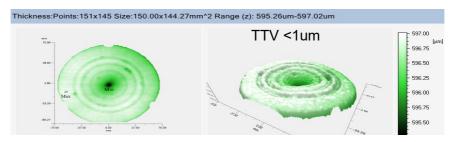


Fig. 2. Global thickness variation result by FRT instrument with high density wafer thickness measurement of 150mm SiC wafer after planarization using HYGRIND fine wheel GV531.

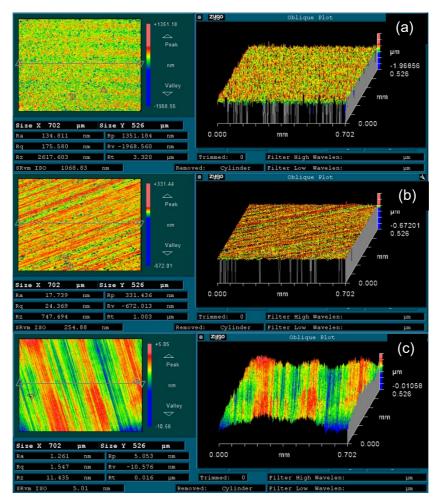


Fig. 3. Comparison of surface roughness measurement by Zygo NewView profilometer of SiC wafers (a) as-cut by wire sawing, Ra = 140nm; Rt = 3700nm, (b) after GV135 coarse grinding process, Ra = 18nm; Rt = 1000nm, and (c) after GV531 fine grinding process, Ra = 1nm; Rt = 22nm.

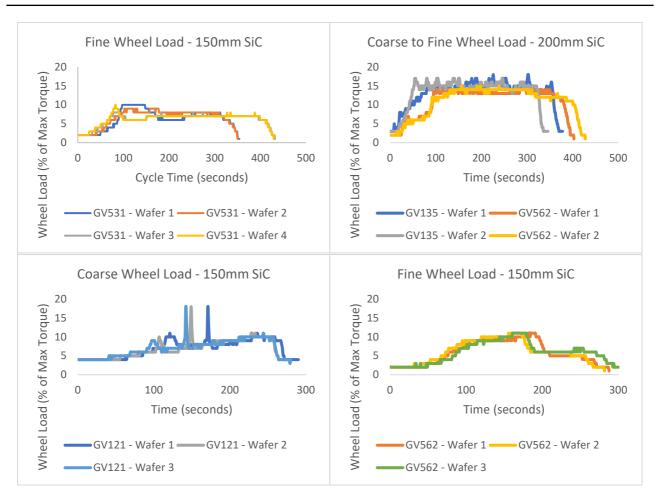


Fig. 4. Grinding wheel spindle load over cycle time of coarse and fine grinding 150mm and 200mm SiC wafers on EAG-28DANX.

150mm SiC wafers planarized by HYGRIND wheels were polished until surface damage was removed. Polishing with HYPREZ consumables and Engis CMP tool fully cleaned up wafer surfaces after removing 1-2 microns in 1 hour. Surface roughness of 150mm wafers after CMP was <0.5nm Ra, as shown in Fig. 5 and Fig. 6. The benchmark processing time by HYPREZ CMP planarization to remove 1-5um of surface damage from process of record fine grinding has been at least 3 hours of polishing and compares to extensive polishing times found in literature [14], [16], [20]. Additionally, processing time did not vary depending on incoming wafer quality, since all wafers were planarized by HYGRIND fine wheels before CMP to below 2um TTV and 30nm Rt. Therefore, planarization of 150mm SiC wafers with HYGRIND coarse and fine wheels effectively reduced CMP planarization time because of the highly uniform surface with minimal deep scratching and low flatness.

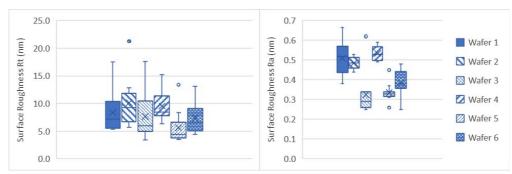


Fig. 5. Distribution of raw surface roughness measurements by Zygo NewView 6300 of six 150mm SiC wafers planarized by HYGRIND wheels and after HYPREZ CMP processing.

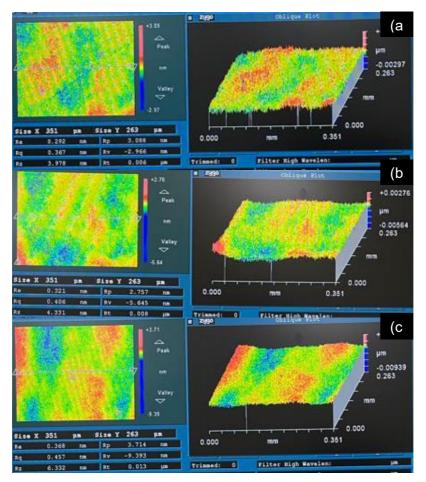


Fig. 6. Surface roughness measured by Zygo NewView 6300 of 150mm SiC wafers after HYPREZ CMP processing, Wafer 3: Ra = 0.3nm; Rt = 7.7nm (a), Wafer 5: Ra = 0.3nm; Rt = 5.6nm (b), and Wafer 6: Ra = 0.4nm; Rt = 7.4nm (c).

Conclusion

Wafering solutions developed by Engis to planarize SiC wafers were used to reduce CMP process time and the effect of incoming surface condition on grinding wheel performance was investigated. 150mm 4H-SiC wafers sliced by wire saw and laser splitting were planarized by HYGRIND coarse and fine wheels, then polished by HYPREZ CMP to epi-ready condition. Grinding 150 to 165mm SiC wafers achieved 1-3um TTV, ~1nm Ra, and ~22nm Rt using the HYPREZ EAG-28DANX wafering system and GV531 HYGRIND fine wheel. HYPREZ CMP process achieved <1um TTV, 0.4nm Ra, and 7nm Rt with processing time reduced by 66% compared to the Engis benchmark and literature. The novelty of minimizing TTV and surface roughness by HYPREZ wafering 'Grind-to-CMP' capability provides a commercially ready solution to prepare 150 to 165mm epi-ready SiC wafers. Development of the HYPREZ wafering solution has continued to scale up for >200mm wafer processing and is expected to also reduce CMP planarization time by minimal subsurface grinding damage and improved wafer flatness.

References

- [1] J. Baliga, High Voltage Silicon Carbide Devices. MRS Online Proceedings Library. 512, (1998) 77–88.
- [2] C.R. Eddy Jr., D.K. Gaskill, Silicon carbide as a platform for power electronics, Science. 324 (5933) (2009) 1398–1400.
- [3] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, J. Rebollo, A survey of wide bandgap power semiconductor devices, IEEE Trans. Power Electron. 29 (5) (2014) 2155–2163.
- [4] P.G. Neudeck, Electrical Impact of SiC Structural Crystal Defects on High Electric Field Devices, NASA/TM. (1999) 209647.
- [5] T. Ohmi, M. Miyashita, M. Itano, T. Imaoka, I. Kawanabe, Dependence of thin-oxide films quality on surface microroughness, IEEE Trans. Electron Devices. 39 (3) (1992) 537–545.
- [6] T. Kimoto, & J. A. Cooper, Physical Properties of Silicon Carbide, in: Fundamentals of Silicon Carbide Technology: Growth, characterization, devices and applications, Wiley-IEEE Press, 2014, pp. 11–38.
- [7] B. Matović, T. Yano, Silicon Carbide and Other Carbides: From Stars to the Advanced Ceramics, in: S. Somiya (Eds.), Handbook of Advanced Ceramics (Second Edition), Academic Press, 2013, pp. 225-244.
- [8] H. Maeda, et. al., High-Speed Slicing of SiC Ingot by High-Speed Multi Wire Saw. Materials Science Forum. 778-780 (2014) 771-775.
- [9] Y. Li, et. al., Surface micromorphology and nanostructures evolution in hybrid laser processes of slicing and polishing single crystal 4H-SiC, Journal of Materials Science & Technology. 184 (2024) 235-244.
- [10] M. Swoboda, et. al., Laser Assisted SiC Wafering Using COLD SPLIT. Materials Science Forum. 897 (2017) 403–406.
- [11] Y. Zhang, et. al., Internal modified structure of silicon carbide prepared by ultrafast laser for wafer slicing, Ceramics International. 49 (3) (2023) 5249-5260.
- [12] W. Cheng, et. al., Discussion on the lapping and polishing process of 4H-SiC wafer, The 8th Annual IEEE International Conference on Nano/Micro Engineered and Molecular Systems, Suzhou. (2013) 841-844.
- [13] H. Yashiro, et. al., Development of Lapping and Polishing Technologies of 4H-SiC Wafers for Power Device Applications. Materials Science Forum. 600–603 (2008) 819–822.
- [14] G. Ma, et. al., A Review on Precision Polishing Technology of Single-Crystal SiC. Crystals. 12 (2022) 101.
- [15] S. Jiang, et. al., Recent progress in SiC monocrystal growth and wafer machining. Pan Tao Ti Hsueh Pao/Chinese Journal of Semiconductors 28 (2007) 810-814.
- [16] W. Cheng, et. al., Discussion on the lapping and polishing process of 4H-SiC wafer, The 8th Annual IEEE International Conference on Nano/Micro Engineered and Molecular Systems, Suzhou. (2013) 841-844.
- [17] S. Jiang, et. al., Recent progress in SiC monocrystal growth and wafer machining. Pan Tao Ti Hsueh Pao/Chinese Journal of Semiconductors 28 (2007) 810-814.
- [18] J. Deng, et. al., Optimisation of Lapping Process Parameters for Single-Crystal 4H–SiC Using Orthogonal Experiments and Grey Relational Analysis. Micromachines. 12 (2021) 910.
- [19] F. Guo, et. al., Shape modulation due to sub-surface damage difference on N-type 4H-SiC wafer during lapping and polishing, Materials Science in Semiconductor Processing. 152 (2022) 107124.
- [20] R. Vacassy, et. al., Surface Engineering of SiC through Nano-Grinding and CMP, Materials Science Forum. 924 (2018) 539–42.