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Poly-SiC Characterization and Properties for SmartSiC™

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Abstract: SmartSiC™ products developed by Soitec in the past four years consist of a high quality monocrystalline silicon carbide (m-SiC) on the top of an ultra-low resistivity polycrystalline silicon carbide (p-SiC or poly-SiC), the interface being electrically conductive. These engineered substrates are intended to bring added value for vertical power devices compared to standard m-SiC, by leveraging the wide bandgap (WBG) properties of the m-SiC and the enhanced p-SiC properties of the base substrate. Thus, it is of paramount importance to understand and monitor the p-SiC properties. In this paper, we present its electrical resistivity, microstructure and texture measurements through SEM and EBSD, thermal conductivity through Laser Flash Anneal (LFA), and Young modulus measurements.

Introduction

Silicon carbide (SiC) power devices are increasingly becoming pivotal components for high-power electronics, encompassing photovoltaic (PV) and traction inverters, power supplies, and motor drives across various markets such as electrical mobility, industry, data centers and renewable energy. Among its unique properties, high electric field breakdown capability and high thermal conductivity make SiC the material of choice for power devices within the 600V to 3,300V range [1].

SiC power electronics devices have been developed for decades using 4H-SiC bulk wafers produced via the Physical Vapor Transport (PVT) method, in which boules are grown at temperatures as high as 2400°C for more than a week. Such a process is known to be energy-intensive and difficult to scale up for larger wafer diameters. Additionally, the electrical resistivity is limited to values greater than approximately 15 mΩ.cm to mitigate stress and minimize the occurrence of defects during growth and cooling.

In the past four years, SOITEC has adopted the Smart Cut™ technology to SiC, enabling the transfer of a thin layer of commercially available monocrystalline Silicon Carbide (m-SiC) onto a 3C polycrystalline Silicon Carbide (p-SiC) substrate, available in both 150mm and 200mm sizes, as illustrated in Fig. 1. With the bonding interface being electrically conductive, it becomes possible to advantage from the wide bandgap properties of the m-SiC on a substrate characterized by a very low electrical resistivity, high thermal conductivity, and mechanical compatibility with device processing methods such as drift epitaxy and annealing for dopant activation, famously recognised as SmartSiC™. Moreover, our p-SiC is obtained thanks to a manufacturing process that is less energy intensive compared to commercially available 4H bulk.

In this paper, we present the material knowledge-driven development performed by Soitec, and its ability to control and ensure excellent p-SiC properties and repeatability of the latter, both in 150mm

and 200mm wafer sizes. These substrates intend to allow high-volume p-SiC supply at targeted electrical resistivity, thermal conductivity, compliant with the SmartCut™ process integration [2,3].

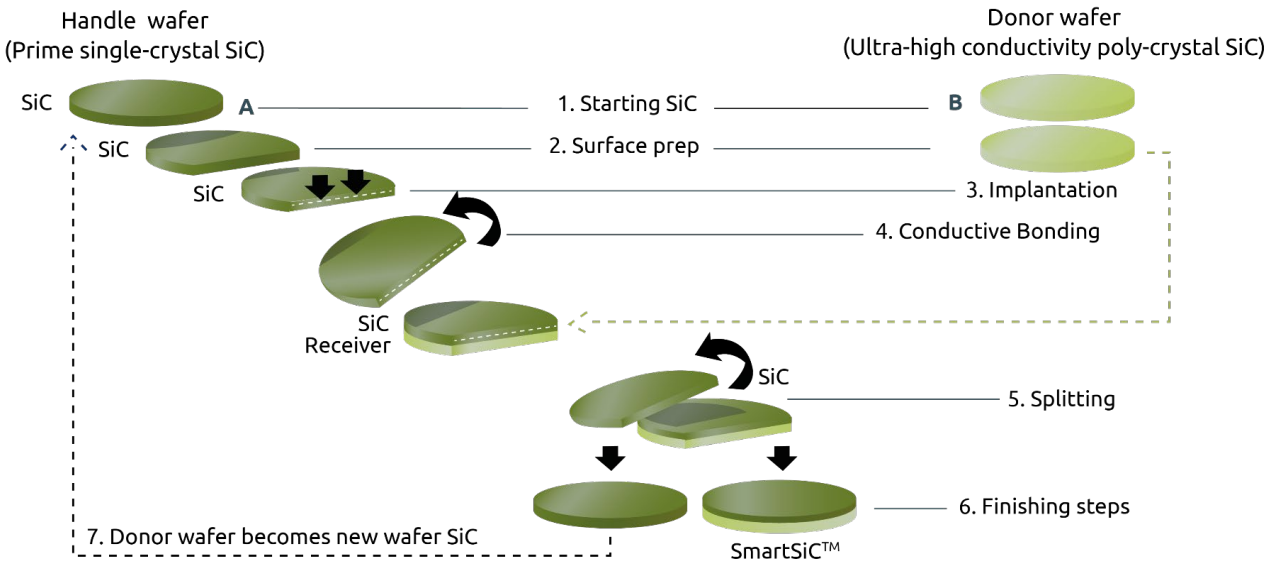

Fig. 1. Smart Cut™ process description [4].

Ultra-low resistivity, a key addvalue of SmartSiC™.

The polycrystalline nature of the material allows for an *n*-type doping level (nitrogen) higher than 10^{20} at/cm^3 and a specified resistivity below 5 mΩ.cm. In Fig. 2, we display the resistivity from wafer to wafer and batch to batch for three different p-SiC flavors. The excellent repeatability ensures consistent device performance. Furthermore, electrical characterizations are conducted on SmartSiC™ substrates, using the same methodology as described in [2]. As depicted in Table 1, ultra low electrical resistivity is confirmed for different p-SiC flavors, demonstrating the excellent compatibility of these composite substrates for the intended power applications.

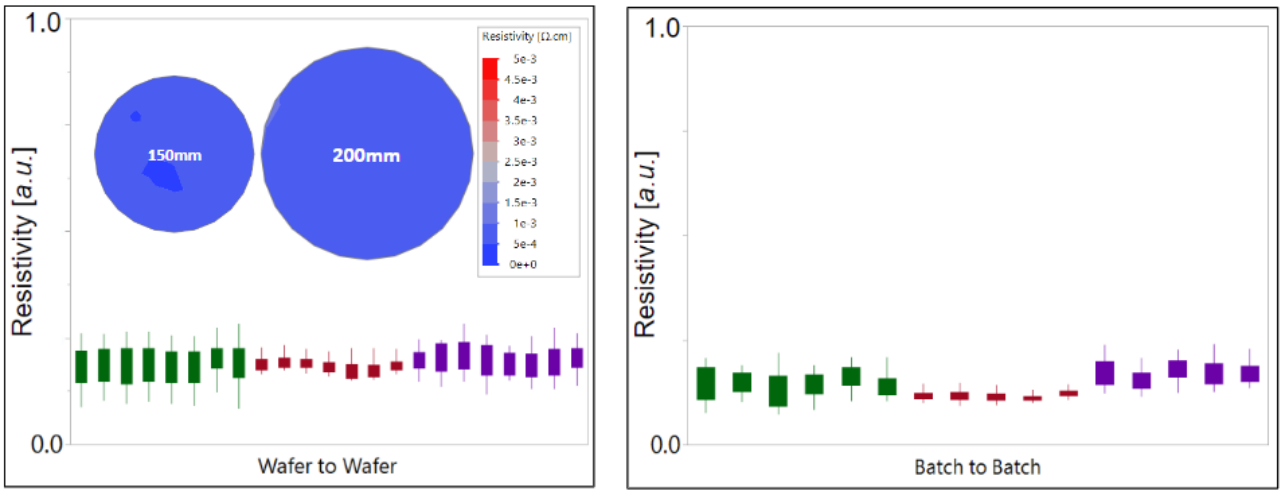

Fig. 2. Electrical resistivities for (a) Wafer to wafer and (b) batch to batch of some of the 10k wafers processed at Soitec in the past four years. The insert depicts examples of electrical mapping for a 150 mm and a 200 mm wafer.

Table I. Electrical resistivity values of p-SiC measured post SmartSiC process: bulk resistivity & Smart Cut bonding interface resistivity for different p-SiC flavors.

Measurement	Resistivity
ρ_{bulk}	1.1 – 2.4 mΩ.cm
$\rho_{interface}$	3.10^{-6} – 1.10^{-5} Ω.cm²

Microstructure and Texture Stability

In Fig. 3, we present SEM cross-section observation and the corresponding EBSD used to control the regularity of the 3C p-SiC microstructure. For all of our p-SiC flavors, the grain size range in micrometers and the regularity of the texture of the polycrystalline material are verified to ensure consistent behavior and compliance with the SmartSiC™ targeted properties throughout the entire device fabrication process. Thus, we ensure the repeatability of each p-SiC bulk. Please note that for confidentiality reasons, the different Miller indices (*hkl*) are anonymized. Therefore, the EBSD image depicted in Fig. 3b is shown only to differentiate the grains from each other and illustrate their good stability.

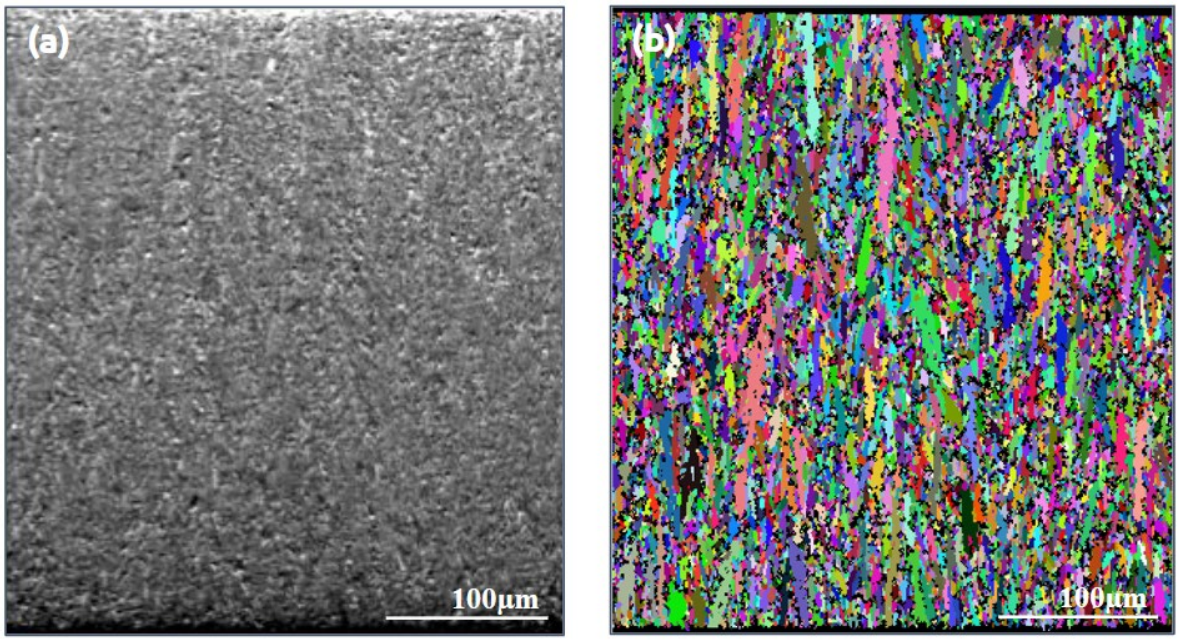

Fig. 3. SEM cross section observation (a) and the corresponding EBSD (b) are part of the standard Soitec Product Control Plan, and are routinely used to check the regularity of the 3C p-SiC microstructure. Harris method is used to determine the texture coefficients from XRD and EBSD measurement.

Thermal conductivity monitoring.

Thermal conductivity of p-SiC is known to be lower than that of standard m-SiC. Various parameters such as grain size, texture, and doping level can impact this important property and were thus tailored to achieve an optimized result. In Fig. 4, we present representative thermal conductivity measurements of both m-SiC and p-SiC. As shown, the difference in thermal conductivity between the two materials decreases with temperature, reaching around 6% at 200°C. Thus, the high conductivity behavior of standard m-SiC bulk is closely approached. Moreover, the thermal interface between m-SiC and p-SiC has been characterized and proven to be highly conductive [5].

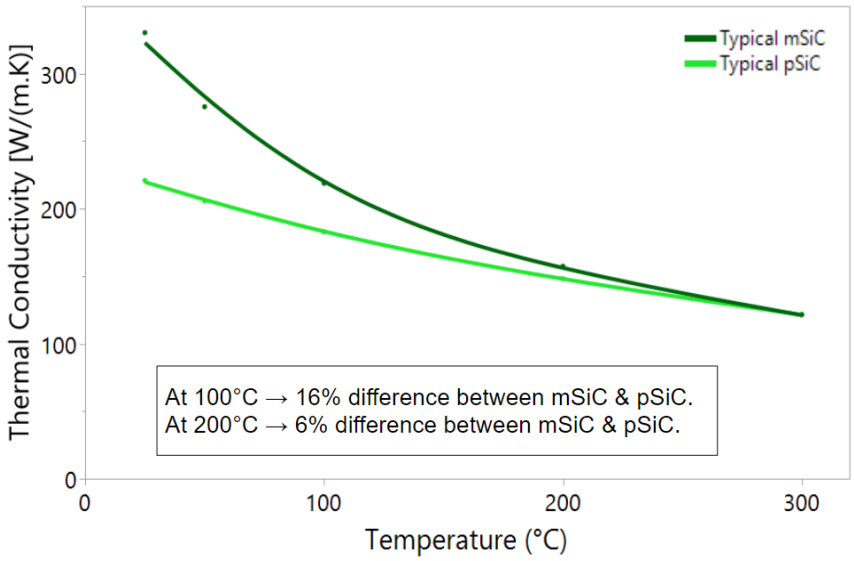

Fig. 4. Thermal conductivity measurement using Laser Flash Anneal (LFA) technique for standard m-SiC bulk and ultra-low resistivity p-SiC.

Young Modulus.

Silicon Carbide's Young modulus is far superior to that of Silicon. This important mechanical parameter is considered significant for the packaging step and the associated device lifetime [6]. In collaboration with Mécanium (France), we implemented a repeatable setup based on a 3 point-bending test to evaluate the Young modulus of p-SiC with good repeatability and standard deviation of 1% from the average value. Moreover, the average values of p-SiC are 7% lower compared to those of m-SiC measured with the same setup. Furthermore, we observed an increased lifetime of the silver sintered die assembly when using our SmartSiC™ as compared to conventional SiC wafers [7,8].

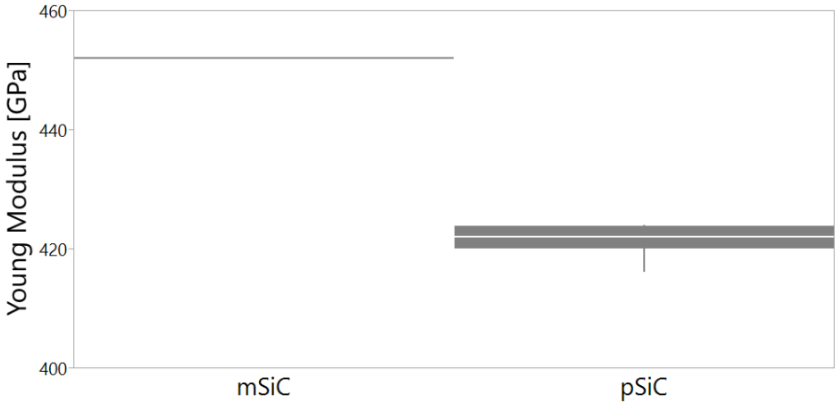

Fig. 5. Young Modulus measurement on standard m-SiC bulk and ultra-low resistivity p-SiC.

Summary

We have demonstrated that the SmartSiC™ engineered substrates are a key asset for the SiC power industry, with proven high crystal quality and ultra-low electrical resistivity. Moreover, the multiple re-use of the standard 4H m-SiC substrate, while maintaining its crystal quality, enables cost-effective manufacturing, as well as a drastic increase in supply for the industry. The properties of the p-SiC used are monitored through different characterizations, some of which are disclosed here, enabling Soitec to tailor our engineered substrate performance. Finally, a new fab has been operational since September 2023 at Soitec dedicated to the production of 150 mm and 200 mm products [9].

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