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Application of Advanced Characterization Techniques to SmartSiC™ Product for Substrate-Level Device Performance Optimization

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Abstract. A review of the specific characterisation techniques developed and customized for SmartSiC™ substrates is given. A focus is made on thermal characterization of this engineered structure as well as its beneficial features with regards to bipolar degradation.

Introduction

SmartSiC™ - an innovative engineered substrate design - has proved to be a competitive option for increased device performance due to its lower on-state resistivity, easier process integration and defect reduction [1-2]. Recently this concept also showed very promising robustness to bipolar degradation [3]. It is based on Smart Cut™ technology, using wafer bonding and hydrogen implantation to transfer a thin high-quality 4H-SiC layer from a donor substrate onto a handle wafer. To address these challenges and opportunities linked to its unique design, specific characterization techniques have been adapted or developed to assess and monitor these key parameters required for high-quality substrates. This paper focuses on two of these characterization techniques, time-domain thermoreflectance (TDTR) and UV illumination/PL vizualisation ("E-V-C"), putting forth the unique properties of the SmartSiC™ design.

SmartSiC™ product features and challenges

The SmartSiC™ process and main features have been detailed in the last few years as illustrated in Fig. 1, it consists of a high-quality engineered substrate whereby a sub-micronic 4H-SiC single crystal layer (typical thickness 600nm) is bonded onto a high electrical conductivity substrate by means of ion implantation and bonding/slicing without the need of epitaxial relationship between the said transferred layer and the said substrate. For optimum compatibility with subsequent epitaxy and device processing, along with cost-effectiveness, this substrate material is typically a 3C-SiC polycrystal. Soitec has been mastering layer transfer on a variety of materials for decades and has recently successfully optimized this versatile technology to 4H-SiC. Smart Cut™ enables the replication of the high crystal quality of the single crystal 4H-SiC donor wafers [4] allowing the same donor wafers to be re-used multiple times. Device results confirmed reduced on-state resistivity values (around -20%) [5] thanks to low bonding interface resistivity and high substrate conductivity. It also brings the opportunity of device fabrication simplification owing to the possibility to remove ohmic contact annealing [6].

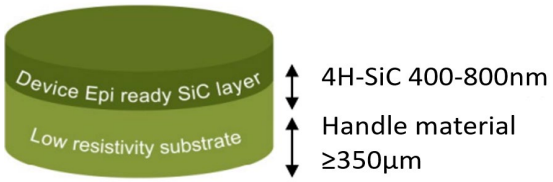

Fig. 1. Typical 150 mm SmartSiC™ stack.

The thin single-crystal 4H-SiC layer, along with the polycrystalline nature of the handle substrate, pose new challenges for the diverse optical metrology already used and well established for bulk-SiC (such as differential interference contrast (DIC) microscopy or photoluminescence (PL)), and adds new critical parameters of interest due to the presence of a discontinuity (namely the bonding interface) between the transferred layer and the host substrate. Therefore, a unique control plan, along with ad-hoc characterization techniques, for such an engineered structure needs had to be identified and developed.

Substrate-level characterization is very important to guarantee the right substrate quality over time and provide quick feedback for substrate process optimization without requiring time-consuming device validation. Table 1. summarizes the main key parameters of the SmartSiC™ substrate considered critical for the subsequent device processing and performance and details the associated techniques. It is noteworthy that all these controls can be done at the wafer level, except for bipolar degradation that requires homoepitaxy, but *not* device processing.

Table 1. SmartSiC™ main critical parameters & associated wafer-level control

Location	Key parameter	Target	Technique	Comment
4H-SiC	Structure defects density (layer integrity, voids etc)	lowest defect density	Deep ultraviolet (UV) scanning laser inspector [7]	-shorter laser wavelength -optimized detection & classification
	Crystal defects	lowest critical defect density	- DIC & PL line microscopy [1], [8] - adapted KOH etch [1]	-optimized classification -optimized chemical etching and classification
	Bipolar degradation (post epitaxy)	lowest SSF expansion	UV illumination+PL observation (this work)	- *substrate-level* - E-V-C (UV illumination)
	Layer thickness	stable vs. optimal value	Ellipsometry	optimal fitting algorithm vs. 4H-SiC layer/3C-SiC
	Metal contamination	lowest value	Inductively coupled plasma mass spectrometry	same as bulk SiC
	Surface roughness	lowest value	Atomic force microscopy (AFM)	same as bulk SiC
Bonding interface	Thermal Boundary Resistance (TBR)	lowest value	TDTR (this work)	submicronic layer challenge
	Electrical Resistivity Barrier	lowest value	Current-voltage (I-V) [1], [9]	use specific structure with mesa isolation
3C-pSiC substrate	Low electrical resistivity	lowest value	Eddy current, 4PP [1], [9]	
	High Thermal Conductivity	highest value	Laser Flash Analysis [9]	
	Microstructure control & mechanical	stable vs. optimal value	Electron backscatter diffraction, X-Ray diffraction (2Th-Th) 3-point flexion, Indentation [10]	
	Wafer shape	lowest value	interferometer [1]	

The following part of this paper will focus on two of these techniques, used for the first time in our knowledge on SmartSiC™ substrates: TDTR for TBR characterization and UV illumination (E-V-C technique) for bipolar degradation.

Focus on SmartSiC™ thermal characteristics & modeled device impact

By essence, SmartSiC™ substrates have a bonding interface separating the single-crystal 4H-SiC layer and the main polycrystalline substrate. It is critical that this interface, induced by the bonding process (surface treatment and/or used materials) does not add a significant thermal boundary resistance (TBR) as this can impact subsequent device performance [11].

Time domain thermal reflectance (TDTR) principle

TDTR has been demonstrated as a suitable technique to investigate the thermal boundary resistances in thin film structures by several studies [12,13]. It is an optical pump-probe technique utilizing a powerful pulsed laser – the *pump* laser – to deliver thermal excitation to the sample, and the resulting temperature transient is monitored by a second, low-power laser, the *probe* laser, which is reflected from the surface and the reflected intensity is measured by a photodetector. The core assumptions are: 1) the pump laser pulse is absorbed near the surface, 2) the electron-phonon thermalization occurs on a (sub)picosecond time scale, resulting in an instantaneous local temperature rise and 3) the reflectivity of the surface is a linear function of the surface temperature. The heat generated by the pump pulse diffuses into the underlying layer structure, and the surface temperature decays at a rate governed by the thermal properties of the materials and boundaries present in the structure. This temperature transient is mirrored by the temporary change in reflectivity recorded by the photodetector. The measured thermoreflectance transients are analyzed using the transmission line model of heat transport [14] and the unknown thermal properties of the structure are determined via nonlinear curve fitting.

To ensure the validity of assumptions 1-3, as well as to improve signal-to-noise ratio it is common to coat samples with a suitable thin metal layer which serves as a transducer: converts the energy of the pump pulse into heat and reflects the probe laser with a strong temperature dependence, i.e. it has a high thermo-optic coefficient. The samples in this work were coated with 10 nm Cr to improve adhesion and 150 nm Au transducer via thermal evaporation.

A probe laser wavelength of 532 nm and pump laser wavelength of 355 nm (pulse FWHM: 1 ns), which are ideal for the Au transducers due to the high thermo-optic coefficient of Au at 532 nm and high absorption at 355 nm. The schematics of the setup used in this work is shown below in Fig. 2a.

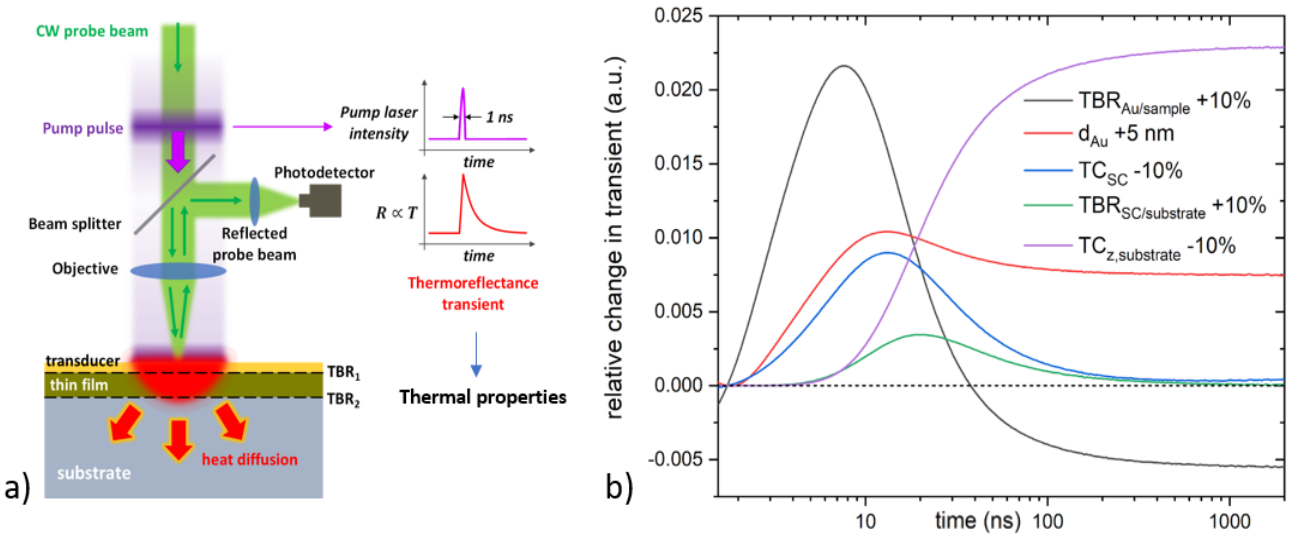

Fig. 2. a) Principle and the schematics of the nanosecond-TDTR setup used in this work. b) TDTR sensitivity to different parameters in a typical SmartSiC™ structure.

The pump laser spot $1/e^2$ radius was ~85 μm, while the probe beam was focused on the sample with a radius of ~3 μm. This reduces uncertainties from spot size variation and results in a quasi-1D heat flow across the thin film ensuring selectivity to the cross-plane thermal conductivity component.

TDTR results and fitted values

The nanosecond-TDTR measurements were performed on three different Smart Cut™ samples: 1) an unannealed sample with monocrystalline 4H-SiC substrate, 2) an annealed sample with monocrystalline 4H-SiC substrate and 3) an annealed sample with polycrystalline 3C-SiC substrate (SmartSiC™ design); at room temperature and 175°C. The samples annealing was performed at 1700°C for 30mn under Ar atmoshpere in order to highlight the sensivity to defect/interface healing. The thermal conductivity (TC) of the Smart Cut™ SiC layer and the TBR represented by the bonding interface – denoted as TBR_2 in Fig. 2.a – were determined by treating them as variables and fitting the measured transients with the solution of the theoretical heat flow model, while other properties of the structure were fixed input parameters. The TC and specific heat capacity of the SiC substrates were measured by Differential Scanning Calorimetry (DSC) and Laser flash Analysis (LFA), respectively. These values refer to the cross-plane thermal conductivity, TC_z. Although 4H-SiC is anisotropic, due to the laser spot configuration the measurement has low sensitivity to the in-plane TC component of the substrate, hence the same values were assumed for TC_r as well. Values for the properties of the Au transducer and the density of the SiC materials were taken from the literature. A further auxiliary fitting variable was the thermal boundary resistance between the transducer and the Smart Cut™ layer, denoted as TBR_1 in Fig. 2.a. This TBR is a limitation of most TDTR techniques, as its value strongly depends on adjoining materials and the surface termination, cleanness etc., hence it typically needs to be treated as a variable. This additional variable may be correlated with other fitting variables to some degree; hence it can increase the uncertainty of the obtained results. The uncertainties of other input parameters also need to be taken into account. The sensitivity of the TDTR transient to some parameters are shown in Fig. 2.b. The sensitivity curves of the thermal conductivity of the Smart Cut™ layer (TC_{SC}) and the TBR of the bonding interface ($TBR_{SC/substrate}$) are very similar and have a strong overlap, i.e., these variables are correlated, and their exact value cannot be independently determined. The Smart Cut™ layer behaves similarly to a 2D thermal resistance in TDTR due to its low thickness, which makes it challenging to separate it from the adjacent TBR. There is an infinite number of combinations of $TBR_{SC/substrate}$ and TC_{SC} values that would all result in indistinguishably good fits of the measured transients. Therefore, in this work the possible ranges for $TBR_{SC/substrate}$ and TC_{SC} were determined, rather than their exact values. The results are listed in Table 2. below. The measured transients are shown in Fig. 3. The first ~5 ns of the transients is characteristic of the heat transport in the transducer layer and across the boundary between the transducer and the sample, then the following ~300 ns is characteristic of the heat transport in the Smart Cut™ SiC layer and across the boundary between the layer and the substrate, while the remaining part of the transient is mainly affected by the thermal properties of the substrate. However, these regions overlap.

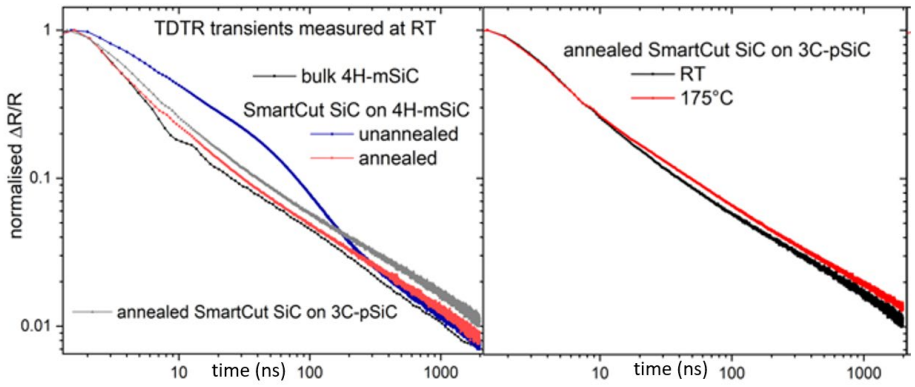

Fig. 3. TDTR transients measured on different SmartSiC™ samples at room temperature and 175°C.

The boundary between a bonded layer and its substrate could act as a bottleneck for thermal transport, which would show up as a shoulder – i.e., a reduction of the cooling rate – on the TDTR transients. The presence of a thermally significant boundary is evident from the transient of the unannealed SmartSiC™ sample, when compared to the transient measured on the bulk 4H-SiC sample where the boundary is absent. The unannealed sample displays a pronounced shoulder in the transient, which corresponds to a TBR of ~12-14 m^2K/GW. The analysis also indicated that the TC_{SC} was low in this sample, ~ 45-55 W/mK which is most likely due to remaining damage due to the layer transfer process. The comparison of the transients also suggests annealing reduces the high thermal resistance of the bonding interface and increases the TC of the as-transferred Smart Cut™ layer. The transient of the annealed sample with 4H-mSiC substrate indicated a TBR between 0.5-3.0 m^2K/GW and a TC_{SC} >175 W/mK. Using 3C-pSiC substrate instead of 4H-mSiC does not seem to significantly increase the TBR of the bonding layer, the corresponding transient can be fitted with values between 0.5-5.0 m^2K/GW and TC_{SC} >100 W/mK. The difference visible between the annealed 4H-mSiC and annealed 3C-pSiC samples is due to the lower TC of the polycrystalline SiC, which results in a lower rate of cooling.

The measurements at 175°C showed a weak temperature dependence of the TBRSC/substrate which is a typical behaviour for thermal boundary resistances. The results indicated a slight decrease of TBRSC/substrate with temperature, as illustrated by the results shown in Table 2. below. The main visible difference between the transients taken at RT and 175°C is due to the reduction of the SiC TC with increasing temperature.

In conclusion, SmartSiC™ achieves low, <5.0 m2K/GW bonding interface thermal resistance on both 4H-mSiC and 3C-pSiC substrates. The annealing is a key step of reducing $TBR_{SC/substrate}$. The temperature dependence of the bonding interface thermal resistance appears to be weak between 25-175°C.

Table 2. TC and TBR values determined from thermoreflectance transients

Temperature	RT (25°C)		175°C	
	TC (W/mK)	TBR (m^2K/GW)	TC (W/mK)	TBR (m^2K/GW)
Unannealed Smart Cut™ SiC on 4H-mSiC	45-55	12.0-14.0	35-45	9.0-11.0
Annealed Smart Cut™ SiC on 4H-mSiC	>175	0.5-3.0	100-130	0.5-3.0
Annealed Smart Cut™ SiC on 3C-pSiC (SmartSiC™)	>100	0.5-5.0	100-200	0.5-4.5
Bulk 4H-SiC (LFA values)	330	N/A	177	N/A

Thermal device simulation results

To evaluate the thermal performance of devices built on SmartSiC™ a 3D model was constructed in COMSOL Multiphysics, a Finite Elements Method (FEM) modeling software. A typical 1.2kV, 400A power module design [11] with 4 almost identical quadrants with 3 diodes and 4 MOSFETs each, was used. It is modeled as a chip mounted on a Direct Bonded Copper (DBC) soldered on a copper heat spreader with a cooling system described as a heat sink (Fig. 4).

The 3D FEM model is a steady-state study, solving heat conduction equations, with a power of 100 W applied on each MOSFET (no power dissipated by the diodes) and a heat sink described by a reference temperature (Tref) and a cooling heat transfer coefficient (hc). Most material properties outside of the chip are taken from [11], and TCs and TBR for the chip are from the present paper.

A reference model, with a 180 µm thick 4H-mSiC chip, with two cooling system hypotheses to create a room temperature and a high temperature operating condition, is used. The room temperature condition assumes a single-phase liquid cooling system (hc = 50 $kW/m^2 \cdot K$) and leads to a maximum working temperature (Tj) around 60°C, on the top surface of the chips. The high temperature

condition assumes a weaker cooling system (hc = 4 kW/m²·K) and leads to Tj around 175°C. For this, the materials properties of the SiC chip measured at 175°C are used. The module temperature distribution shows some significant spreading below the chips, as seen in Fig. 5.
Then the bulk 4H-SiC is replaced by the SmartSiC™ structure measured earlier (taking the thermal worst-case scenario) and the results are compared in Table 3.

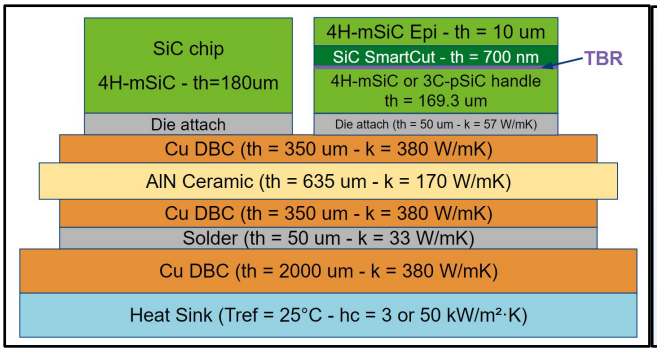

Fig 4. Materials stack of the power module

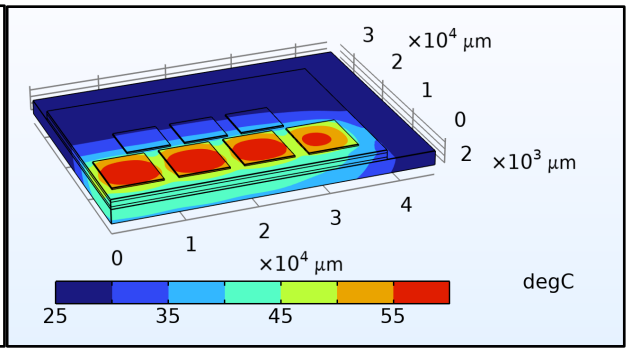

Fig 5. 3D view of temperature distribution

Table 3. Maximum junction temperature from the simulation results

Temperature	Room Temperature (25°C)				High Temperature (175°C)			
	TC (W/mK)	TBR (m²K/GW)	Tj (°C)	Tj increase (%)	TC (W/mK)	TBR (m²K/GW)	Tj (°C)	Tj increase (%)
Bulk 4H-mSiC	330	-	59.68	-	177	-	179.08	-
Unannealed SmartCut SiC	45	14	59.71	0.04%	35	11	179.10	0.01%
on 4H-mSiC	330				177			
Annealed SmartCut SiC	175	3	59.69	0.01%	100	3	179.08	0.00%
on 4H-mSiC	330				177			
Annealed SmartCut SiC	100	5	60.86	1.97%	100	4.5	179.91	0.46%
on 3C-pSiC	170				130			

As a conclusion, the simulations confirm that the increase in thermal resistance from the added layers and interface of the SmartSiC™ substrate does not have a significant impact on the device thermal performance, with a maximum increase of the junction temperature of about 1°C.

SmartSiC™ behavior versus bipolar degradation

Bipolar degradation is a well-known issue detrimental to the reliability of 4H SiC-based bipolar devices [15]. It is caused by the growth of Schokley stacking faults (SSF) initiating from basal plane dislocations (BPDs), induced by electron-hole pair recombination. It is typically characterized by testing bipolar diodes in forward-current conditions with different current densities. It causes a significant reduction in the carrier lifetimes thus increasing the forward voltage drop in SiC bipolar devices, increasing diode resistance in ON state and severe leakage current path in the reverse-biased junction. Therefore, it is very important to be able to characterize new substrate designs and potential related process or design issues in terms of bipolar degradation.

The comparison between bulk 4H-SiC and SmartSiC™ was done on 2 epitaxy runs (6 months apart) processing SmartSiC™ and bulk 4H-SiC wafers within the same epitaxy batch in an AIXTRON G5 WW C planetary reactor in 8x150 mm configuration. The homoepitaxy design was a typical 2µm n+ buffer (nitrogen doping at 1E18 at/cm3) followed by a 10µm n- (1E16 at/cm3) drift layer. The 4H-SiC single crystal layer within the SmartSiC™ stack and the reference 4H-SiC bulk wafer were obtained from the same vendor and crystal quality capability for direct comparison.

Bipolar degradation through UV illumination

Bipolar degradation post epitaxy without diode processing was carried out on these wafers using the E-V-C technique developed by ITES, Co. (Japan). This consists in triggering SSF-driven bipolar degradation with UV illumination followed by selective band-pass filter (BPF) (~420 nm)

photoluminescence review [16]. Different UV intensities with a wavelength of 355 nm were used (38, 75 and 150W/cm²). For wafer set #1 (first run), a static test was performed whereas for wafer set #2 (second run), a scanning approach was used in order to improve the irradiance uniformity at a scan speed of 5 mm/s.

A binning and statistical counting process was carried out to compare the two different substrates designs: 3 sites were taken few mm apart at 3 different random wafer locations several cm apart.

Behavior comparison between bulk and SmartSiC™ towards UV illumination

Fig. 6. presents the corresponding results. As the UV illumination power increases, SSFs develop, with a rate 4 to 12 times faster in the case of bulk SiC compared to SmartSiC™ (ratio of linear regression of SSF area over illumination between the 2 wafer designs). A typical comparison between the 420nm BPF observation fields is given in Fig. 7 for wafer set #1.

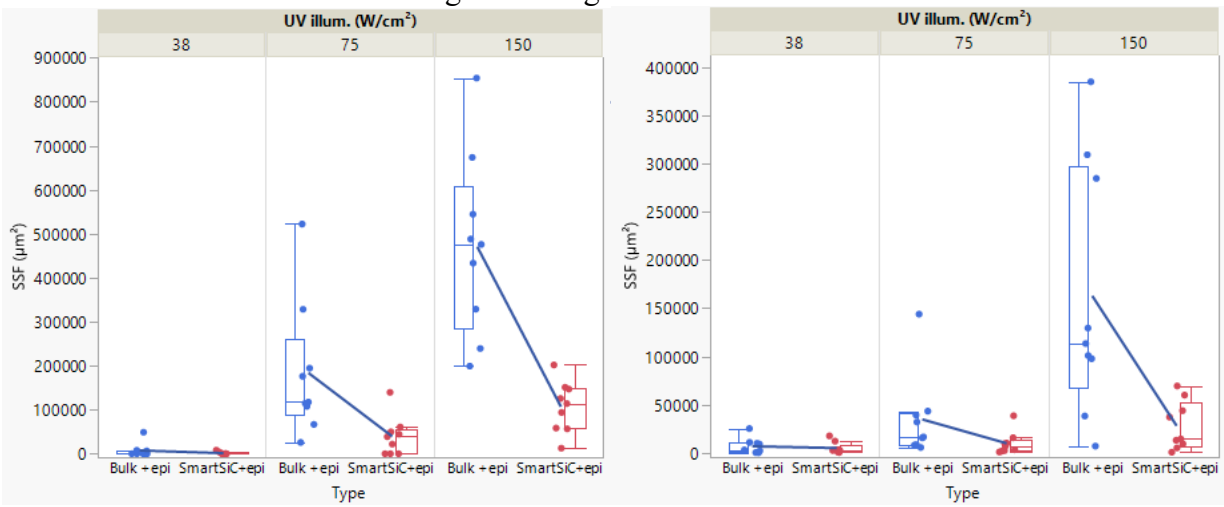

Fig. 6. Statistical comparison of bipolar degradation severity (SSF area obtained by pixel thresholding) for different UV illumination intensities and wafer locations, between bulk 4H-SiC+epi (blue) vs. SmartSiC™+epi (red) for wafer set #1 (left) and wafer set #2 (right) .

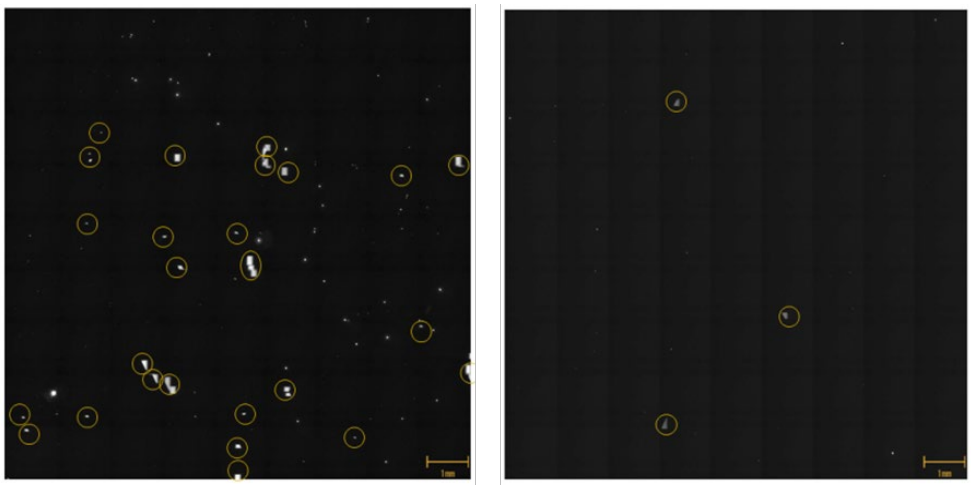

Fig. 7. Typical 10x10mm observation fields post UV illumination (here 150 W) 420nm BPF PL of bipolar degradation severity between bulk+epi (left) vs. SmartSiC™+epi (right).

Discussion about SmartSiC™ Bipolar degradation through UV illumination

The results seem to confirm the intrinsic advantage of SmartSiC™ design over bulk in terms of bipolar degradation robustness previously characterized by forward-current stress test in a similar type of bonded engineered substrate [3]. In the present case, it appears that both the number of SSFs

and their typical size are lower in the case of SmartSiC™ compared to bulk. One hypothesis [3] is based on the role of the discontinuity that constitutes the bonding interface as a blocking point for the TED-BPD translation during the downwards glide process. Recently, the pinning role of hydrogen in the bipolar degradation limitation was put forward in the case of epitaxial bulk SiC with a proton implantation [17]. Given the significant proton dose used in the Smart Cut™ process to obtain SmartSiC™ wafers, this hypothesis seems probable in the present case.

Summary

A review of the SmartSiC™ control plan was given, with a focus on two important features: a very low thermal boundary resistance, leading to a negligible impact on simulated temperature elevation and the confirmation of the interesting robustness to bipolar degradation of this structure. The latter paves the way to device performance improvements and associated in-depth study on the physical mechanisms at play.

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