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Dicing Process for 4H-SiC Wafers by Plasma Etching Using High-Pressure SF_6 Plasma with Metal Masks

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Abstract. Since SiC is hard and brittle, dicing by normal grinding process not only requires a long time for processing, but also reduces chip strength due to microcracks. The use of highly efficient and damage-free etching with high-pressure plasma as a chemical processing method for dicing rather than mechanical processing was investigated. The results of groove processing using a combination of a metal mask with slit-like apertures and plasma etching with high-pressure SF_6 plasma showed that the processing speed decreased with decreasing slit width and increasing groove depth. The results of electrostatic field calculations suggest that this is due to a decrease in plasma intensity caused by electric field decreasing.

Introduction

Although SiC power devices have been installed in railways and high-end vehicles, their widespread use requires their lower costs. However, the high hardness and brittleness of SiC make mechanical processing, such as grinding and polishing, time consuming, and lead to lower yields due to microcracks and residual stresses on the surface after machining, which increases the cost. Currently, diamond blade grinding is commonly used in the dicing process, where wafers are cut into chips after device formation, but high efficiency without cracks and chips is difficult to achieve. Furthermore, cracks introduced on the cut faces may reduce the chip strength. Ultrathin wafers after backside thinning are even more susceptible to cracking and chipping. To address these challenges, we investigated the use of highly efficient and damage-free etching with high-pressure plasma as a chemical processing method for dicing rather than mechanical processing.

Initially, cutting by plasma localized around the wire electrode was explored. However, as the power increased to boost removal rate, it was difficult to achieve high-speed and narrow cuts due to the plasma's tendency to spread, leading to wider groove widths [1]. Subsequently, a method using an insulating material mask to restrict the plasma generation area was tested so that the plasma does not spread even with increasing power was investigated. This method allowed for high-speed and narrow groove width machining on a small piece sample [2-3]. However, generating stable plasma proved challenging when increasing plasma length, making it difficult to apply the method for wafer-level cutting. Recently, high-speed etching of SiC has enabled removal rates of over 10 μm/min at the wafer level using high-pressure SF_6 plasma [4]. Based on this advancement, we propose a novel dicing method that uses a mask with an aperture formed only in the cutting area, combined with high-speed etching using high-pressure SF_6 plasma.

Experimental Setup

An overview of the experimental setup is shown in Fig. 1. The sample used in this study composed of a small piece of a C-face 4H-SiC (0001) substrate with a metal mask featuring a slit-like apertures. After setting the sample, the chamber was initially evacuated and filled with SF_6 gas up to 2.5 kPa. Thereafter, while supplying SF_6 from inside the electrode at 250 sccm, 13.56 MHz RF power was applied to the electrode to generate plasma. The processing gap was set to 1.7 mm. During processing, the pressure was kept at 2.5 kPa by controlling the opening of the exhaust valve. After processing, the chamber was exhausted one more time, and then it was purged with nitrogen gas, and finally, the sample was taken out. The grooves formed by the processing were assessed for depth by confocal laser microscopy.

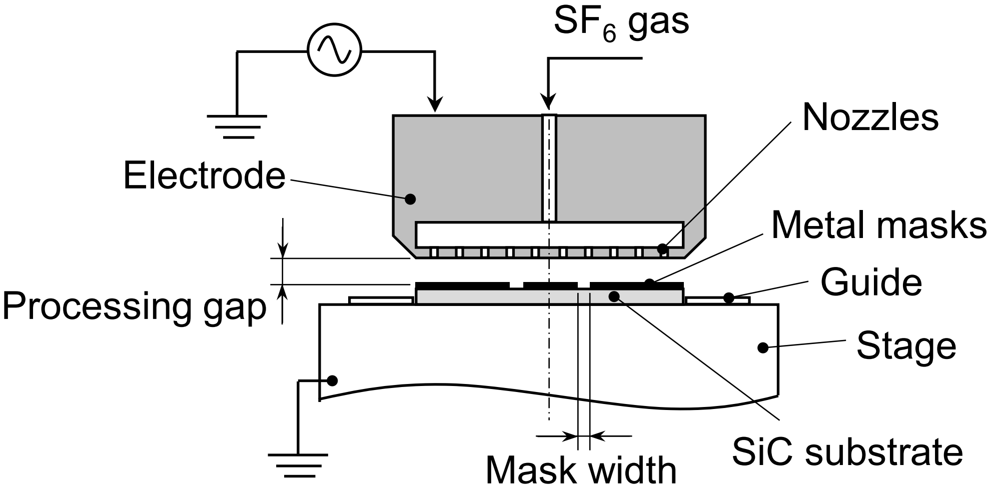

Fig.1 Schematic diagram of the experimental apparatus.

Results and Discussions

Dependence of Groove Depth on Mask Width. First, the dependence of the groove depth on the mask width was investigated when processing at 500 W for 10 min. Mask widths of 20, 40, 70, 100, 150, and 200 μm were used. The results are shown in Fig. 2. The removal rate was approximately 2 μm /min at a mask width of 200 μm consistent with the thinning speed at the same power [4]. However, it was observed that the removal rate decreased as the mask width decreased. To consider the cause of the decrease, electrostatic field calculations were performed using EStat (Advanced Science Laboratory. Inc.), a two-dimensional finite element method electrostatic field analysis software. The electric field intensity near the SiC substrate surface (indicated as the "Evaluation point") was calculated for a groove depth of zero and a groove depth of 10 μm (Fig. 3(a)). The results are shown in Fig. 3(b). Before the grooves are formed, there is almost no effect of mask width, but after the grooves are formed, the electric field intensity decreases with decreasing mask width, which qualitatively agrees with the experimental results in Fig. 2.

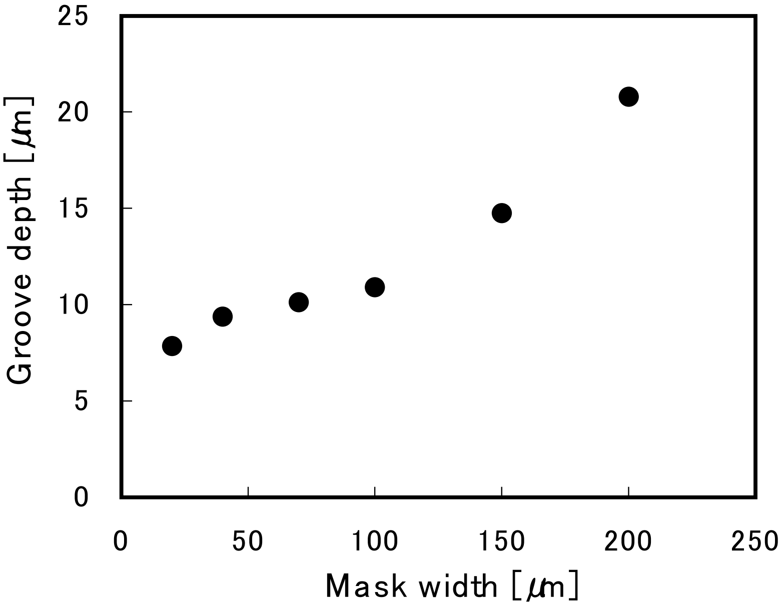

Fig. 2. Relationship between mask width and groove depth.

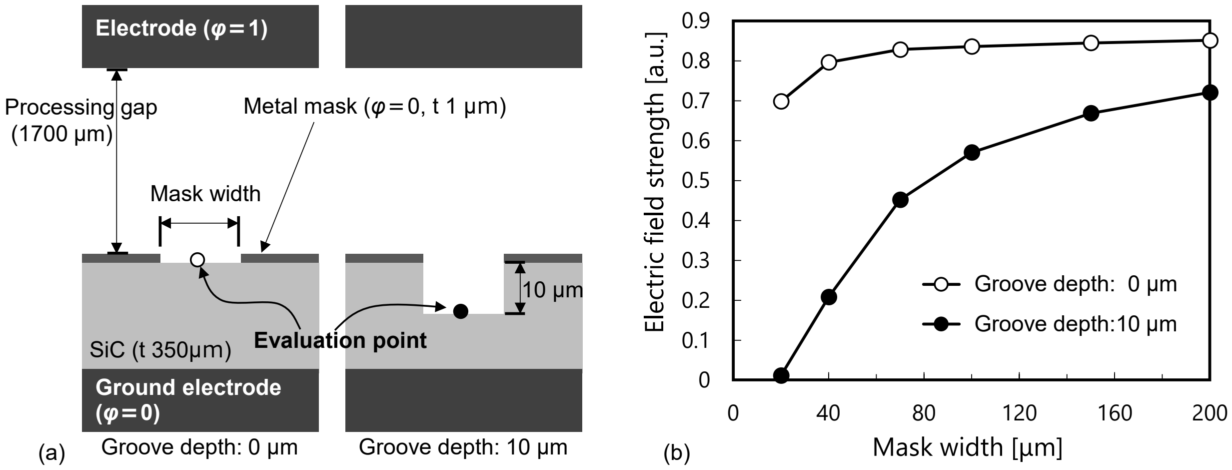

Fig. 3. Calculation of electrostatic field strength: (a) calculation model and (b) results.

Dependence of Groove Depth on Processing Time. Next, to investigate the dependency of the groove depth on machining time, a mask width of 30 μm and a power of 700 W were used. The results presented in Fig. 4 indicate that the machining speed decreased with increasing machining depth and tended to saturate around the mask width. Looking at the area near the mask width of 30 μm in Fig. 3(b), it can be seen that there is no significant decrease when the groove depth is zero, but the electric field intensity decreases significantly as the groove depth increases to 10 μm. The decrease in processing speed with processing time is thought to be because the narrow groove structure weakens the electric field intensity, making it difficult for plasma to be generated at the bottom of the groove.

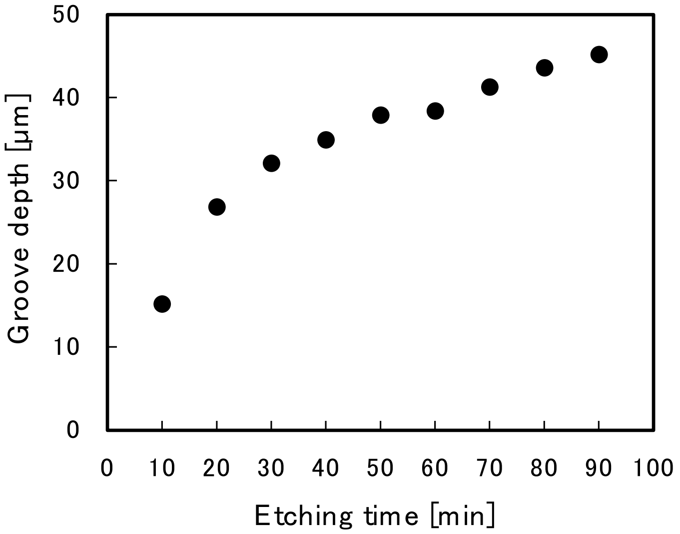

Fig. 4. Dependence of groove depth on etching time.

Wafer-level Experiment. Finally, a 2-inch wafer was used instead of a small sample and processing was carried out at 700 W of power for 15 min using the same mask width with the former section. Fig. 5 shows a photograph of the wafer with the mask removed after processing, which proves that the groove shapes were formed on the entire surface. Also, the groove depth was found to be ~ 20 μm everywhere almost consistent with the results in Fig. 4.

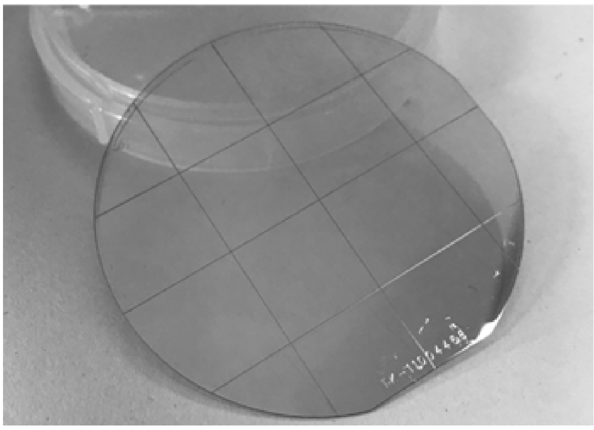

Fig. 5. A photograph of the 2-inch SiC wafer after a dicing experiment.

Summary

The combination of metal masks with slit-like apertures and plasma etching using high-pressure SF_6 plasma shows potential for damage-free high-efficiency SiC dicing processes. In the future, the groove width will be evaluated and the removal rate will be improved by increasing the RF power. While a similar technology called "plasma dicing" has been successfully applied to silicon using reactive ion etching (RIE) [5][6], there are no reports of plasma dicing applied to SiC. This may be due to the slow removal rate of SiC in RIE, which is performed in a high vacuum atmosphere, and the lack of a practical removal rate for dicing.

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