*Materials Science Forum*
*ISSN: 1662-9752, Vol. 1124, pp 67-76*
*doi:10.4028/p-Cb7qw4*

*Submitted: 2023-09-29*
*Revised: 2024-05-02*
*Accepted: 2024-05-02*
*Online: 2024-08-21*

# Demonstration of SiC-on-Insulator Substrate with Smart Cut™ Technology for Photonic Applications

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**Keywords:** SiC-on-insulator (SiCOI), Smart Cut™, transferred layer, bow compensation, photonic devices, simulation.

**Abstract.** Silicon-carbide-on-insulator (SiCOI) is a promising platform for photonic integrated circuits. However, the development of this new photonic platform is hindered by the lack of high-quality commercial SiC-on-insulator substrates. In this study, we present a demonstration of the transfer of a single crystalline semi-insulating 4H-SiC thin film on a $SiO_2$ insulated substrate at 150 mm wafer scale using the Smart Cut™ technology. We describe the development of SiCOI substrates and their characterization at each key step of the process. In particular, we provide a detailed study of bow compensation related to the implanted SiC donor substrate. The quality of the transferred SiC layer was investigated as a function of the final annealing temperature applied. The optical indices of the bulk SiC were measured using spectroscopic ellipsometry, and an advanced model has been used to take into account the strong birefringence of the silicon carbide film. Finally, simulations were conducted to design a preliminary set of basic and advanced photonic devices.

## Introduction

For several years, silicon carbide (SiC) has been identified as a material of choice for many applications in power electronics [1-4] because of its remarkable properties, such as its high physical hardness, exceptional thermal conductivity (480 $W.m^{-1}.K^{-1}$), chemical inertia and wide band gap (2.4-3.2 eV). These unique characteristics mean that SiC power semiconductors can increase energy conversion efficiency, withstand higher voltages and currents as well as a higher operating temperature than conventional silicon-based devices [1]. Recent demonstrations show that SiC is a promising material for the realization of quantum and nonlinear photonic circuits [5-8]. Indeed, it combines many interesting optical properties: a wide transparency window (UV to mid-IR), high second and third order optical nonlinearity coefficients ($\chi(2)$, $\chi(3)$), a high refractive index and no

two-photon absorption (TPA) at near infrared wavelengths. SiC also exhibits point defects (colored centers) which are promising for Qubit realization due to their long spin coherence time and room temperature operation.

SiC photonics has been explored for some years, with very recent breakthrough demonstrations [9] such as low-loss waveguides, high quality factor resonators, efficient on-chip frequency conversion via $\chi(2)$ and the integration of single spin Qubits with nanophotonic cavities. This brings SiC to the forefront of efforts towards a monolithic platform combining quantum and nonlinear photonics [10]. However, these developments are hampered by the lack of commercial SiC-on-insulator (SiCOI) wafers. In fact, the aforementioned demonstrations rely on extremely expensive and experimental SiCOI dies obtained by the bonding and thinning method [10, 11]. While offering better performance in terms of material quality, with the lowest measured optical losses (< 0.38 dB/cm [12, 13]), the bonded SiC layer thickness exhibits high variability across the wafer [10], while being extremely cost ineffective since most of the material is lost. Inspired by the fabrication of silicon on insulator wafers (SOI), SiCOI substrates fabricated with the ion cutting (also named Smart Cut™) method are getting a growing interest. Despite higher material optical losses due to the ion implantation, microrings with reasonable Q-factors up to $7.3\times10^4$ [14, 15] (~ 7 dB/cm) have recently been demonstrated in academic facilities, leaving room for further improvements. Thus, the good thickness uniformity as well as a limited cost are significant advantages for the realization of future commercial devices. However, the healing of the transferred SiC layer seems to be the key to the future of this technology. Building upon extensive experience and expertise in the Smart Cut™ process for fabricating substrates used in power components [16-19] and optical devices [9-10, 14-15, 20-21], this study seeks to showcase the cost-effective production of high-quality SiCOI wafers.

The paper focuses on the Smart Cut™ SiCOI manufacturing process. The key process steps are described, developed and punctuated by detailed characterizations. Building on the work of Rouchier *et al*. [16] and Gelineau *et al*. [17] on transferred SiC substrates for power electronics, we will show how we adapted this fabrication process for photonic applications. In this study, we chose to work with a monocrystalline SiC (mSiC) handle substrate (instead of Si) in order to understand the effects of high-temperature annealing (between 1200°C and 1600°C) on the healing of the transferred SiC layer as well as on its optical properties. This study would not have been possible if we had chosen a Si handle, due to the Si melting temperature of 1410°C as well as the strong CTE difference between Si and mSiC. With a view to industrialization, this handle monocrystalline SiC substrate can be replaced by a polycrystalline SiC one. The second part of this paper will be devoted to the design of the first components and the simulation of guides and resonators.

## Process flow of SiC-on-Insulator Substrate Fabrication

The fabrication process for the SiCOI substrates developed here using the Smart Cut™ technology is schematized in Fig. 1.

First, semi-insulating donor wafers of high-purity 4H-SiC (N-doped $\approx 5\times10^{11}$ $cm^{-3}$), 150 mm diameter and 500 µm thick (from SICC) and receiver wafers of N-doped ($\approx 5\times10^{18}$ $cm^{-3}$) monocrystalline 4H-SiC 150 mm diameter and 350 µm thick (from DOW CORNING) were used. A protective, electrically insulating layer of silicon oxide is deposited by PECVD (Plasma Enhanced Chemical Vapor Deposition) on the front side of the donor substrate (550 nm) and on both the front and backside of the receiver substrate (3500 nm) to compensate for the important wafer curvature. Then, $SiO_2$ layers are densified by annealing at 1100°C for 1 h under $N_2$ at atmospheric pressure.

Hydrogen ions ($H^+$) are implanted at room temperature (RT) on the front side of the donor substrate through the 550 nm oxide layer. During the implantation step, the substrate is tilted by 7° to minimize the channeling effect. $H^+$ ion implantation creates a damaged layer below the implanted surface - the so-called "fracture zone" - the depth of which can be controlled according to the implantation energy [10, 18]. After front side $H^+$ implantation, a curvature compensation technique has been developed by counter hydrogen-implantation on the backside with a fluence inferior to Smart Cut™ one (low enough to prevent blistering of the backside of the wafer). This key step was characterized by bow measurements. It is extremely important since such curvature would degrade the bonding quality and complicate the use for future photonic platform processing equipments that work in automatic mode. To ensure a high-quality bonding, we polish the PECVD oxide on both substrates to reduce surface roughness. The two substrates are brought into contact for direct $SiO_2/SiO_2$ bonding. Then, the bonded substrates undergo a thermal annealing at a temperature below 1000°C under $N_2$ to achieve spontaneous fracture (also called splitting) (Fig. 1) and transfer of a layer of semi-insulating 4H-SiC onto the $SiO_2$/SiC receiver substrate. Then, one of the SiCOI substrate was annealed at 1200°C under $N_2$ at atmospheric pressure for 1 h to improve the bonding strength and heal the ion implantation-induced defects in the transferred SiC layer crystal [18]. Another SiCOI substrate was cleaved into 2×3 cm² samples. One of these samples was annealed at 1300°C, one at 1400°C, one at 1500°C and one at 1600°C, for 30 minutes. The last sample was left untouched in order to characterize the initial state of the transferred layer. Finally, chemical-mechanical polishing (CMP) is performed (on wafer and on samples) to remove the defect zones induced by ion implantation and to achieve a very low final surface roughness of the transferred mSiC layer. Thickness and uniformity of the transferred layer were monitored by spectroscopic ellipsometry. Surface topography of the transferred layer was characterized by atomic force microscopy (AFM). We also perform wafer warpage measurements at each step using a dual chromatic white light (CWL) sensor. The crystalline quality of the transferred 4H-SiC layer was characterized using X-ray diffraction (XRD).

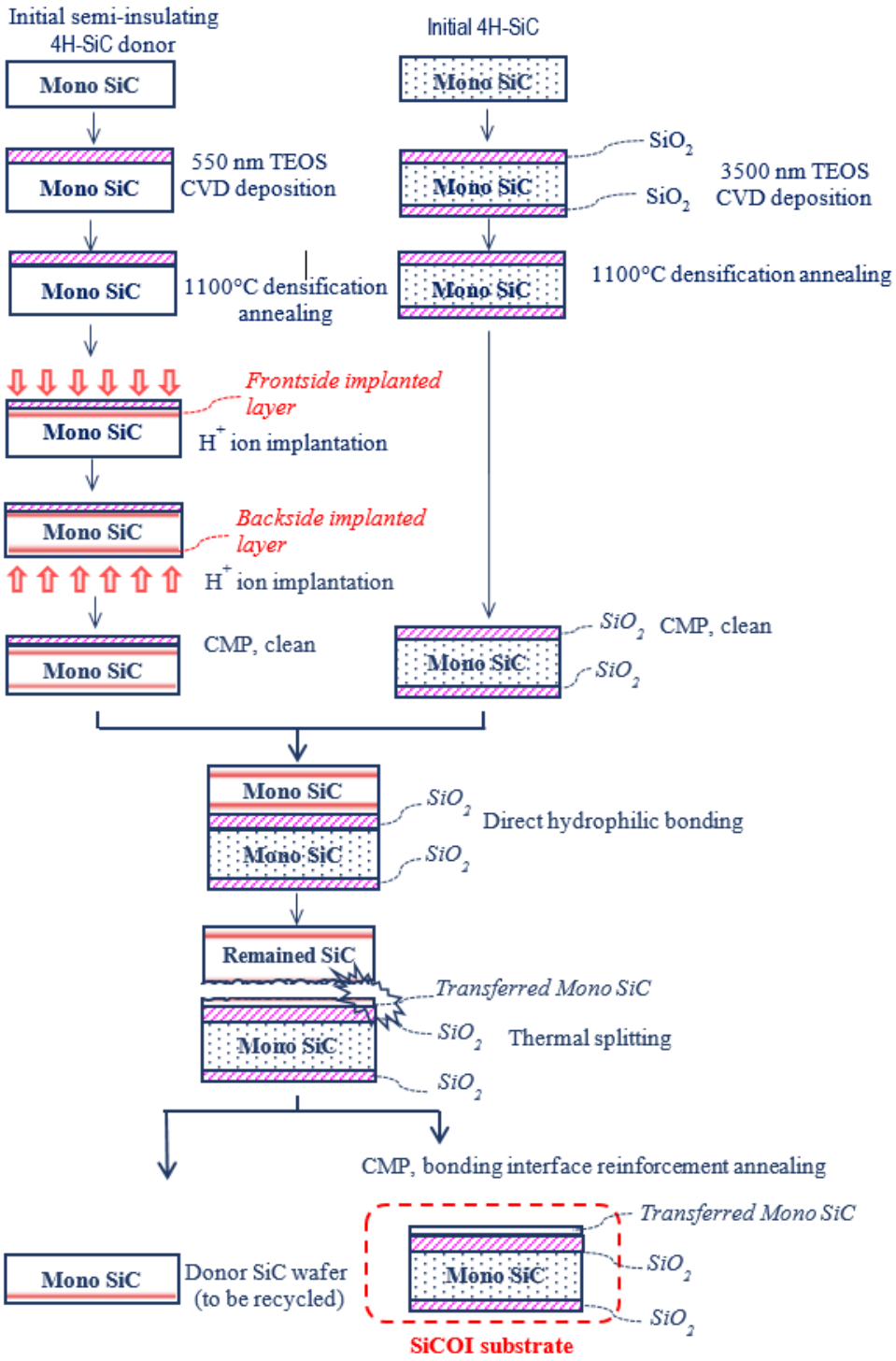


**Fig 1.** Technological flow of the SiC-on-insulator substrate

Thus, once the SiCOI substrate was obtained, photonic devices are defined using e-beam lithography. The patterns are then transferred to the SiC layer using $SF_6/O_2$ via reactive ion etching (RIE).

## Results and Discussions

We have produced 150 mm SiCOI wafers with a 400 nm-thick mSiC layer transferred onto a monoSiC receiver substrate using a direct $SiO_2/SiO_2$ bonding process. Fig. 2 shows a schematic cross-section of the resulting SiCOI substrate and a picture of the wafer after splitting. These substrates are visually of very good quality, with only very few bonding defects and with a thin edge exclusion (< 3 mm).

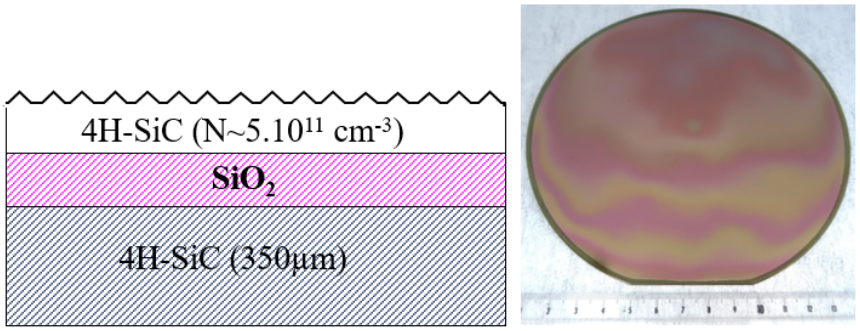


**Fig 2.** Picture and cross-sectional scheme of a 6'' SiC-on-insulator substrate post splitting.

**Thickness measurement.** The thicknesses of the buried oxide layer (Fig. 3(a)) and the mSiC layer (as-transferred Fig. 3(b) and post-CMP Fig. 3(c)) were determined using spectroscopic ellipsometry. The average thickness of the oxide layer measures 3.6 µm. The average thickness of the as-transferred 4H-SiC film is 640 nm, exhibiting excellent uniformity (< 2.5%) over the entire wafer surface as illustrated by the 25-point thickness map in Fig. 3(b). After polishing, the wafer's uniformity worsens to 14.3% and the average thickness reduced to 376 nm. As we will discuss later, an optimal mSiC thickness for optimal optical performance is targeted at 500 nm. Our ongoing efforts are focused on optimizing the polishing process to minimize material removal and achieve a final thickness of approximately 500 nm.

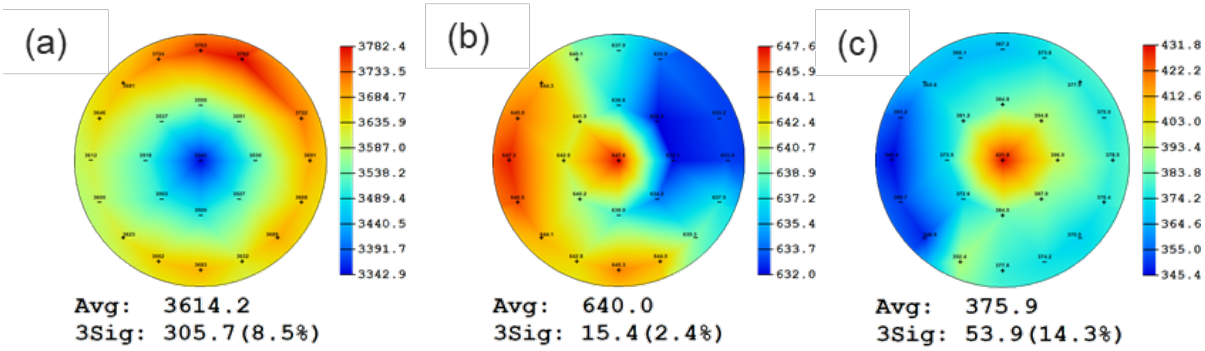


**Fig. 3.** 25 points thickness maps of the (a) buried oxide, (b) as-transferred 4H-SiC and (c) post CMP transferred 4H-SiC layers obtained by spectroscopic ellipsometry.

**AFM measurement.** Surface roughness of the transferred 4H-SiC film was measured by AFM at the center and edge of the 150 mm SiCOI wafer as shown in figures 4(a)-(d). Post splitting, the surface roughness is important at both the edge and the center of the wafer (as shown in Fig. 4(a) and Fig. 4(b), respectively) with a root mean square (RMS) roughness of about 6 nm on a scan of 5×5 µm$^2$. To obtain a smoother surface compatible with optical components fabrication, the surface of the SiCOI substrate is optimized by CMP over the entire 150 mm area as shown in Fig. 4(c)-(d). After the CMP step, the RMS roughness value is reduced to 0.16 nm at the wafer edge (Fig. 4(c)) and 0.18 nm at the center (Fig. 4(d)). The final substrates show a very good post-CMP surface finish.

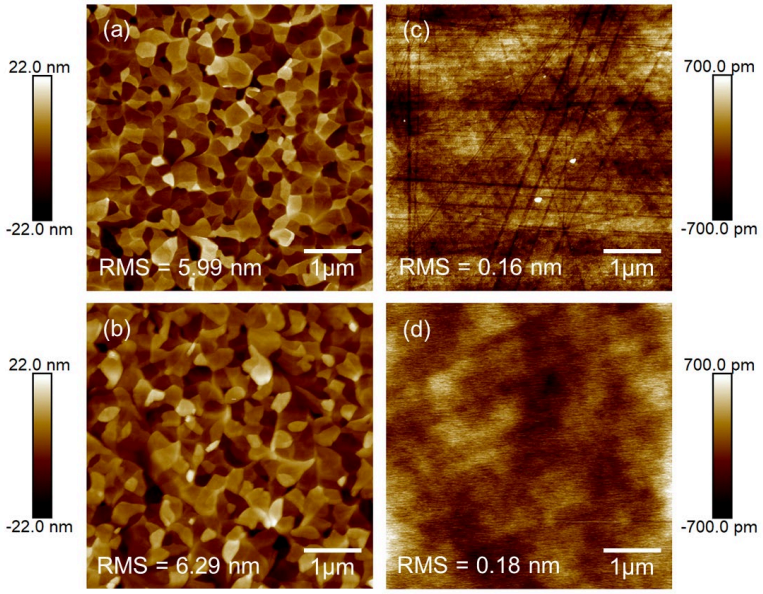


**Fig. 4.** AFM height measurement images of as-transferred 4H-SiC film at (a) substrate edge and (b) center. (b) AFM images of 4H-SiC film post CMP at (c) substrate edge and (d) center.

**Bow compensation before direct bonding.** In its original state, the SiC wafer shows little curvature (Fig.5, "initial wafer"). However, some process steps such as the oxide film deposition or the ion implantation step can cause bow due to mechanical stress. We monitored the bow of the donor wafer after each step by a dual CWL with two identical sensors placed above and below the sample. Fig. 5 shows the results of bow measurements of the donor wafer after 500 nm $SiO_2$ deposition and annealing, front side $H^+$ ion implantation and backside $H^+$ ion implantation. $H^+$ front side implantation generates a large bow of 233.2 µm with which the subsequent bonding step (see Fig. 1) would be difficult to carry out on un-optimized equipments. After backside H+ implantation at a lower dose than that used for front side implantation (to prevent the donor substrate from blistering on the backside), the bow measurement is 36 µm, which is compatible for direct bonding (Fig. 5). Thus, this technique can compensate for the strong curvature induced by hydrogen ion implantation in SiC and produce to a low final substrate curvature (< 40 µm).

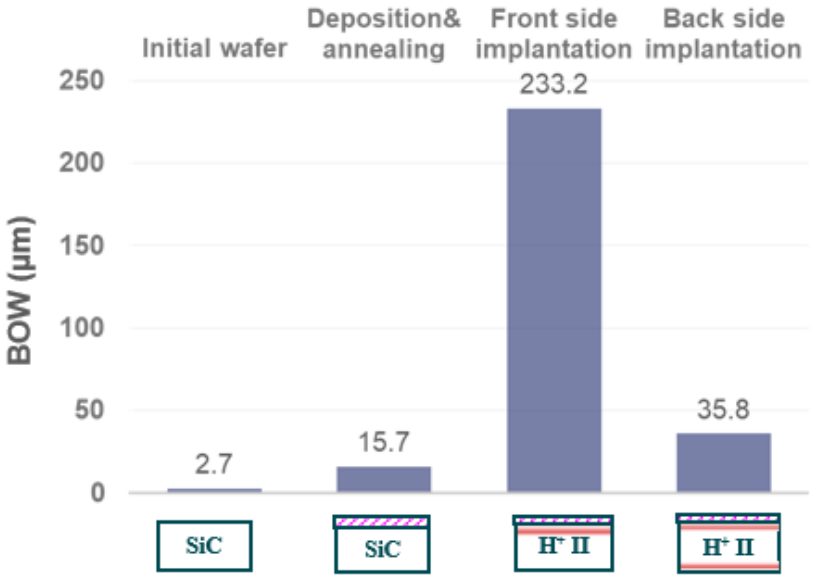


**Fig. 5.** Bow measurements of the donor wafer as received, after 500 nm $SiO_2$ deposition and annealing, after front side $H^+$ ion implantation and finally after backside $H^+$ ion implantation.

**XRD measurement.** In order to understand the effect of temperature on the crystalline quality of the transferred SiC layer, we carried out high temperature annealing (between 1200°C and 1600°C) on dedicated samples. XRD rocking curves (RCs) were compared between a bulk mSiC reference substrate and SiCOI substrates annealed at different temperatures: after splitting, post 1200°C, post 1300°C and post 1500°C. (Fig. 6(a)). We can see that the full width at half maximum (FWHM) of the RCs is much larger post-splitting and decreases with the application of annealing. However, even after annealing at 1500°C, the FWHM remains higher than that obtained on bulk mSiC. This means that the top mSiC material crystalline quality has not been completely healed even after annealing at 1500°C. The crystal quality of the transferred SiC layer was also investigated using XRD Reciprocal Space Mapping (RSM) of the (0004) 4H-SiC Bragg peak established on samples post splitting step (Fig. 6(b)) and post-annealing at 1200°C and at 1500 °C (Fig. 6(c) and Fig. 6(d) respectively). One can immediately assess the important asymmetry in Qz post splitting (Fig. 6(b)) – corresponding to an important strain gradient in the transferred SiC layer. For T ≥ 1200°C however, a full relaxation of the crystal is observed, without any deformation gradient. The presence of residual hydrogen in the mSiC transferred layer post-splitting, as confirmed by SIMS analysis [17], is highly likely to be the root cause of the observed non-uniform crystal deformation. Nevertheless, the reasons behind the inadequacy of 1500°C annealing for healing the transferred layer and the specific defects implicated remain unclear. To gain deeper insights into this phenomenon, optical assessments of components fabricated on these substrates following annealing at various temperatures will be indispensable.

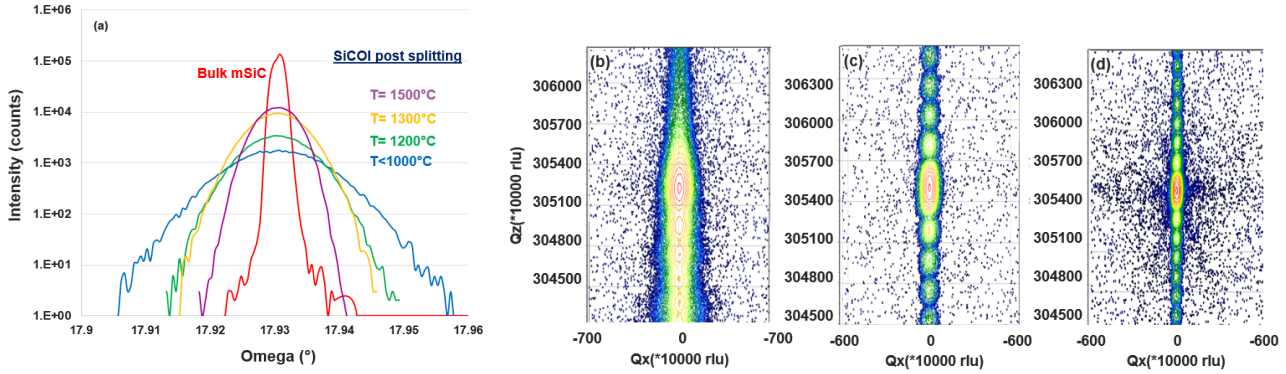


**Fig. 6**. (a) The (0004) XRD rocking curves for the bulk monocristalline 4H-SiC, for SiCOI post splitting (T < 1000°C) and for the SiCOI substrates post-annealing at 1200°C, 1300°C and 1500 °C. (b) XRD-RSM of the (0004) 4H-SiC Bragg peak established on samples post splitting step, (c) post-annealed at 1200°C and (d) at 1500 °C.

**Development of photonic devices.** First and foremost, the characteristics of the SiC guiding layer must be known in order to design the photonic devices. The optical indexes of the bulk SiC have been measured on a wavelength span from the visible to the near-infrared by ellipsometry. A model has been used to take into account the strong birefringence of the silicon carbide. As shown on Fig. 7(a), the extracted ordinary and extra-ordinary refractive indices are in good agreement with previously reported values [22]. The thickness of the SiC layer has been fixed to 500 nm as a compromise between the waveguide propagation losses, devices compactness and nonlinear properties.

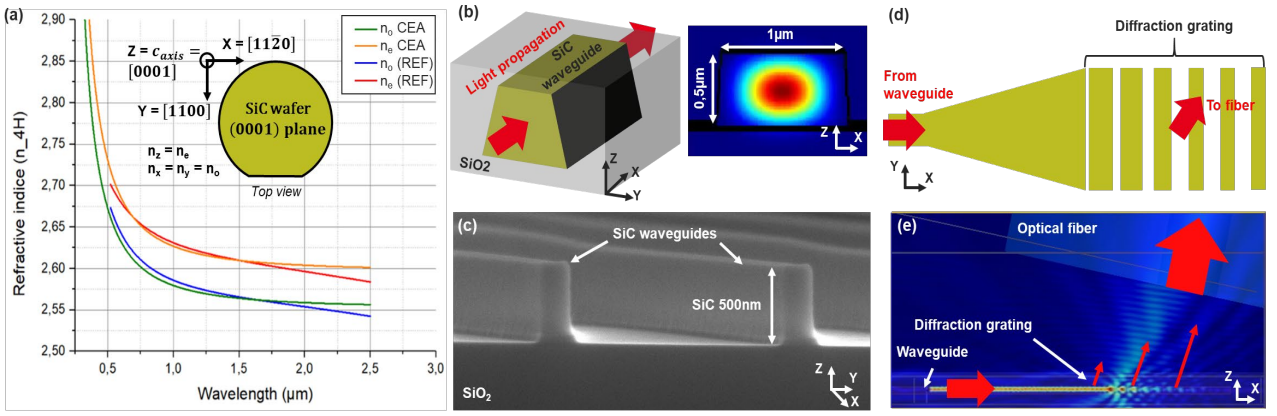


**Fig. 7.** (a) 4H-SiC refractive indexes measurement by ellipsometry, in comparison with [22] (b) SiC waveguide geometry and the associated modal simulation (electric field magnitude, Lumerical™ software from ANSYS [23]). (c) Scanning electron microscope view of fabricated SiC waveguides on SiCOI substrates (d) Chip-fiber coupler geometry and (e) the associated light propagation simulation [23].

Knowing the thickness and refractive index of the guiding layer, the conception of the basic photonic devices can begin with the more fundamental one: the optical waveguide. As shown on Fig. 7(b), the modal behavior of a SiC waveguide with typical dimensions (1×0.5 µm²) has been simulated in order to estimate its optical characteristics (effective optical index, chromatic dispersion, propagation losses, etc.). Using e-beam lithography and a standard etching process, waveguides were patterned and structured on SiCOI substrates as illustrated on Fig. 7(c). Another key component is the chip-fiber coupler which is used to transfer light to/from the small SiC waveguides (typical core size of the order of 100 nm) to/from standard optical fibers (typical core size of about 10 µm) which can then be connected to an external light source (laser) or photodetectors. As shown on Fig. 7(d), it consists of an enlarged waveguide coupled to a diffractive grating that will extract the light into free space. Using optical simulations (Fig. 7(e)), its dimensions (period of the grating, width of the structure) can be tuned in order to maximize the waveguide-fiber coupling efficiency.

As mentioned in the introduction, by combining (i) a strong nonlinear coefficient $\chi(3)$, (ii) a high refractive index and (iii) low propagation losses, silicon carbide is a material of choice for the realization of efficient optical nonlinear functions [12]. In particular, the generation of stable and intense Kerr frequency combs (ultra-stable multi spectral laser source) is of growing interest due to the vast field of applications [24]. As shown on Fig. 8(a), the light from an external continuous wave (CW) laser is injected to a feeding waveguide that is evanescently coupled to a looping waveguide (ring) that will act as a resonator. By tuning the optical power coupled to the resonator from the feeding waveguide (simulation Fig. 8(b)), an extremely high power density can be reached, which is key to trigger the generation of the frequency comb.

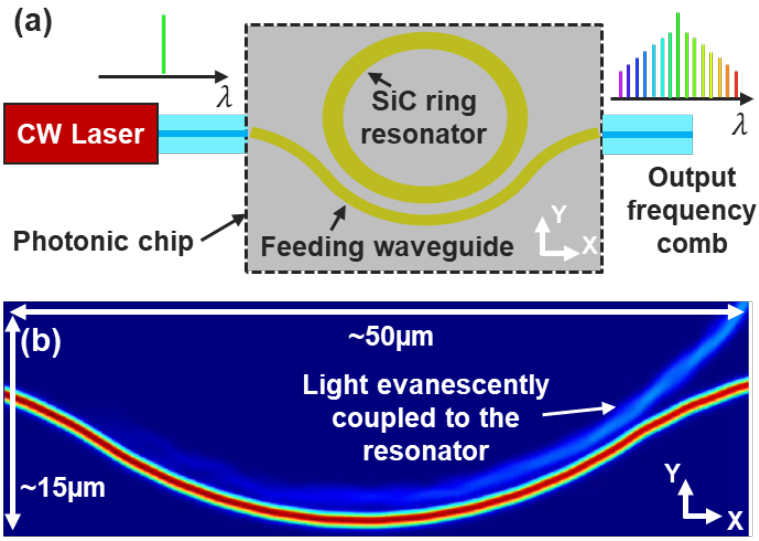


**Fig. 8.** (a) Principle of the generation of a Kerr frequency comb (multi spectral laser source) using a SiC microring resonator. (b) Simulation of the feeding waveguide – ring light coupling efficiency.

## Summary

This work presents the 150 mm SiCOI substrates fabricated using the Smart Cut™ technology. A 400 nm mSiC layer was successfully transferred onto a thick (> 1 µm) $SiO_2$ layer. The SiCOI substrates, obtained through a technologically optimized process involving the use of the Smart Cut™ technology and a meticulous bow compensation technique, are devoid of bonding defects, exhibit a final low surface roughness value (< 0.2 nm) and present a thin edge exclusion. XRD measurements show that the transferred mSiC layer post splitting exhibits a significant strain gradient. For T ≥ 1200°C, the transferred SiC layer completely loses this deformation gradient and as the annealing temperature increases, the crystalline quality of the layer improves. Thanks to advanced optical simulations, photonic devices will be fabricated on all these SiCOI substrates, enabling us to determine the impact of the quality of the transferred layer on the optical properties of these devices. In the previous literature, the reported maximum annealing temperature of SiCOI substrates made by Smart Cut™ is 1200°C due to their Si handling. With the studies reported in this paper, we expect to see a significant improvement of the optical performances of the fabricated SiC photonic devices by going up to 1500°C.

## Acknowledgement

This project has received funding from the Key Digital Technologies (KDT) under Grant Agreement No 101007237. The KDT receives support from the European Union's Horizon 2020 research and innovation programme and Germany, France, Italy, Sweden, Austria, Czech Republic, Spain. Part of this work, performed on the Platform for NanoCharacterisation (PFNC) of CEA, was supported by the "Recherche Technologique de Base" Program of the French Ministry of Research.

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