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A Novel Contactless SiC Wafer Planarization Processing after Mechanical Slicing by Dynamic Thermal Annealing Processes

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Abstract. In conventional machining of SiC wafers, material loss and sub-surface damage (SSD) of both the front and back surfaces are major issues. In this study, we focused on Dynamic AGE-ing® (DA), which is a sublimation-controlled process, and applied it to the total wafering process without any mechanical contact of both the front and back surfaces to explore the possibilities to reach the CMP-equivalent quality. DA process enables material lossless planarization of SiC wafers by applying a temperature gradient to achieve simultaneous etching and growth at the same rate on one and the other surfaces, respectively. To drive the planarization function for a multi-wire saw finished as-sliced wafer, as an example, a high-temperature regime above 2000 ºC under an Ar background pressure higher than 1 kPa to suppress etching and growth rates was employed as the first step in the DA treatment. In this step, an effective annealing function arises where sublimation and recrystallization occur simultaneously through a sub-surface region on both sides of the wafer. Due to the active interchange of the surface and subsurface layer, a self-organizing planarization effect occurs on a macroscopic scale on both surfaces with the removal of SSD. The conventional DA processes were employed for the following microscopic flatness control. As a result, the roughness of the 6-inch as-sliced wafer was reduced to 0.7 nm on the Si-face and 2.0 nm on the C-face while maintaining the wafer thickness. This is the first promising result exhibiting the potential of thermal contactless treatment for next-generation wafer manufacturing by improving quality and cost.

Introduction

SiC wafers sliced from boules are typically planarized by conventional machining processes with mechanical contact, such as lapping/grinding, mechanical polishing (MP), and chemical mechanical polishing (CMP). These multi-step machining processes produce SiC wafers with flat surfaces that are applicable to the CVD process (Ra: ≤ 0.1 nm). However, it is known that sub-surface damage (SSD), which deteriorates the epitaxial growth layer, remains near the surface of the wafer [1-5]. Additionally, the material loss of about 100 μm that occurs when fabricating a single CMP-finished wafer through these machining processes is a significant issue due to the high material cost of SiC. To produce commercially viable SiC wafers with a thickness of 350 μm, the boule must be sliced into wafers of 450 μm thickness. If the material loss during the machining processes could be completely eliminated, it would be possible to slice at a thickness of 350 μm. This realization is expected to improve the yield of SiC wafers by more than 20 %. Developing a new process that simultaneously achieves the three goals of as-sliced SiC wafer planarization, SSD removal, and material lossless will lead to a major breakthrough. As a potential method that could solve these as-sliced SiC wafer planarization issues, we focused on the Dynamic AGE-ing® (DA) method, a contactless thermal sublimation process.

DA is a sublimation etching/growth technique for the Si- or C-face of single crystal SiC wafer placed in a quasi-closed polycrystalline SiC container using a temperature gradient between the

container and the wafer as the driving force. The C/Si ratio of the quasi-closed environment, which depends on the existence of the Si supply component, is autonomously maintained constant over a wide temperature range. So far, we have focused on one side (Si-face) of MP- and CMP-finished SiC wafers, using DA-etching for surface planarization (Ra: ≤ 0.2 nm) and removal of residual SSD [6-9]. These DA processes were performed in the temperature range of 1500 - 1900 °C and under ultra-high vacuum (10^{-5} - 10^{-7} Pa) environmental conditions. However, as-sliced wafers with extremely rough Si-face (Ra: ≥ 40 nm) must be planarized to CMP-equivalent levels (Ra: ≤ 0.1 nm) without material loss and SSD. In addition, a mirror surface is required on the C-face to prevent leaks during vacuum chucking or other negative effects during device fabrication. With conventional DA process conditions, such dramatic planarization is difficult to achieve. Thus, we propose a new annealing process that applies the DA process in order to solve this problem.

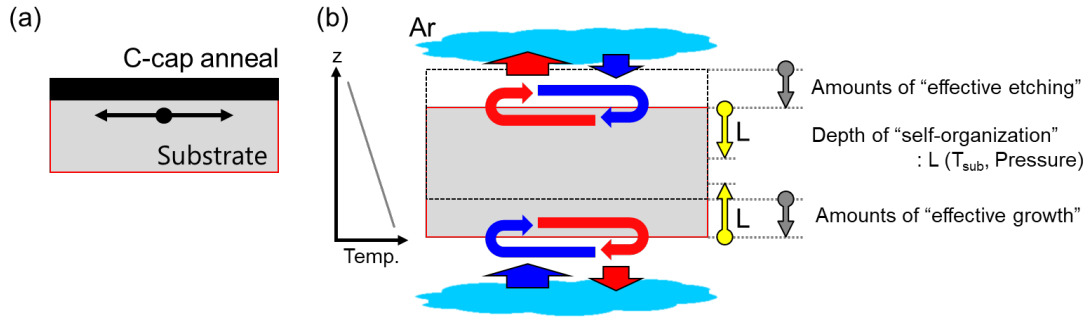

Fig. 1. Schematic diagrams of (a) carbon-cap anneal (closed-end), which is a conventional static anneal, and (b) a novel Dynamical anneal effect (open-ends), which is a new concept that allows simultaneous control of both sides.

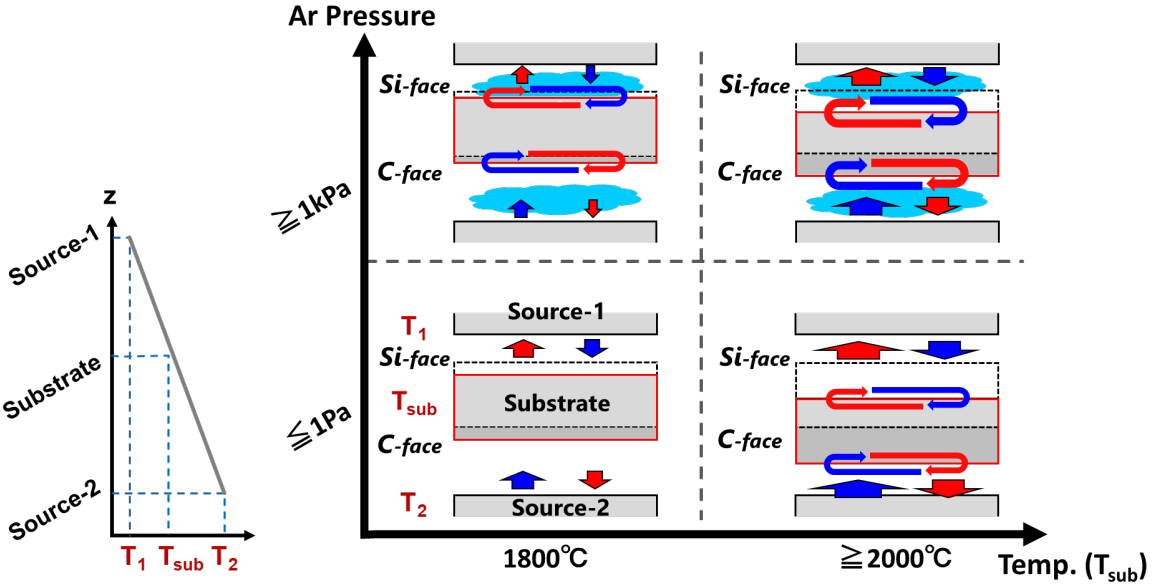

Fig. 2. Schematic diagram indicating the temperature and pressure dependence of the Dynamical anneal effect.

A typical annealing technique for SiC is carbon cap annealing, which is performed after ion implantation, as shown in Fig. 1 (a). This technique attaches a carbon cap to the surface (closed-end) to suppress surface roughening and carbonization. In contrast, in the DA process, both surfaces (Si- and C-face) are not covered (open-ends) because the SiC wafer is held in the hollow. As shown in Fig. 1 (b), consideration of both sides in the DA process leads to two functions. The first is the lossless effect, in which one side is etched by a temperature gradient while the other side grows almost at the same rate. The second function is the self-organization effect that occurs on both the etching and

growth faces. The effect results from the simultaneous occurrence of intense sublimation and recrystallization reactions. The lossless effect is enhanced at slower growth and etching rates. The removal of SSD and surface planarization due to the self-organization effect is greater as the sublimation and recrystallization reactions are more intense (Fig. 2). This self-organization effect is also enhanced in near-thermal equilibrium process conditions, where both the growth and etching rates are small. We defined the "Dynamical anneal effect" as combining these effects. This effect is expected to be maximized under high-temperature and high-pressure conditions. Therefore, the DA process, which is performed at a high temperature of 2000 ℃ or higher and a pressure of 1 kPa or higher, is referred to as DA-annealing. DA-annealing is a DA process performed under conditions that maximize the "Dynamic annealing effect". In this study, we observed the evolution of the roughness of as-sliced SiC wafers before and after DA-annealing in order to develop a planarization process without the material loss and the SSD. We also investigated the extent to which as-sliced wafers can be planarized by combining DA-annealing with the conventional DA processes.

Experiments

A 6-inch 4H-SiC (0001) wafer 4º off-cut toward <11-20> direction sliced by a multi-wire saw (MWS) with loose abrasive was used as the sample. During the DA process, the wafer was placed in a hollow within a polycrystalline SiC container. DA-annealing conditions were used for 1 h at a high temperature of more than 2000 ℃ and a pressure of more than 1 kPa. As conditions for DA-etching, we used a SiC-Si phase equilibrium environment (PE) with Si supply components and a SiC-C PE without components at 1800 ℃ for 1 h in an ultra-high vacuum (10^{-5} - 10^{-7} Pa). Visual inspection was used to confirm macroscopic flatness, and low energy electron channeling contrast imaging (LE-ECCI) by SEM was used to confirm microscopic flatness [10, 11]. The cross-sectional profile and roughness Ra were measured by AFM (10 μm x 10 μm) to evaluate the microscopic surface flatness. The surface morphology and the roughness Sa were also confirmed by laser microscopy (200 μm × 200 μm) to evaluate the macroscopic surface flatness. The total thickness of the SiC wafer was measured with an electronic caliper. The electron back-scattered diffraction (EBSD) method by SEM was used to observe SSD.

Results

Fig. 3 shows laser microscope images of the Si- and C-face of the as-sliced SiC substrate. The Sa values for Si- and C-face, indicating the surface roughness in the macroscopic range, were 166 ± 22 nm and 270 ± 22 nm, respectively. We investigated the temperature and pressure dependence of surface morphology and wafer thickness variation by DA processes using these as-sliced wafers. Figs. 4 (a) and (b) show the Si- and C-face measurement results, respectively. As shown in Figs. 4 (i) and (i'), when the DA process was performed at low-temperature and low-pressure (1800 ℃, 10^{-5} - 10^{-7} Pa), the macroscopic roughness Sa of the Si- and C-face were 70 and 745 nm, respectively. Under these conditions, which are commonly used for DA processes, while the Sa on the Si-face improved by about half, it increased by a factor of three on the C-face. The total thickness

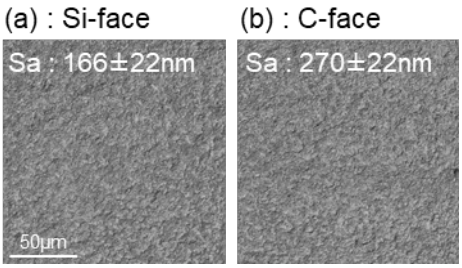

Fig. 3. Laser microscope images of the Si- and C-face of the SiC wafer sliced by MWS (loose abrasive).

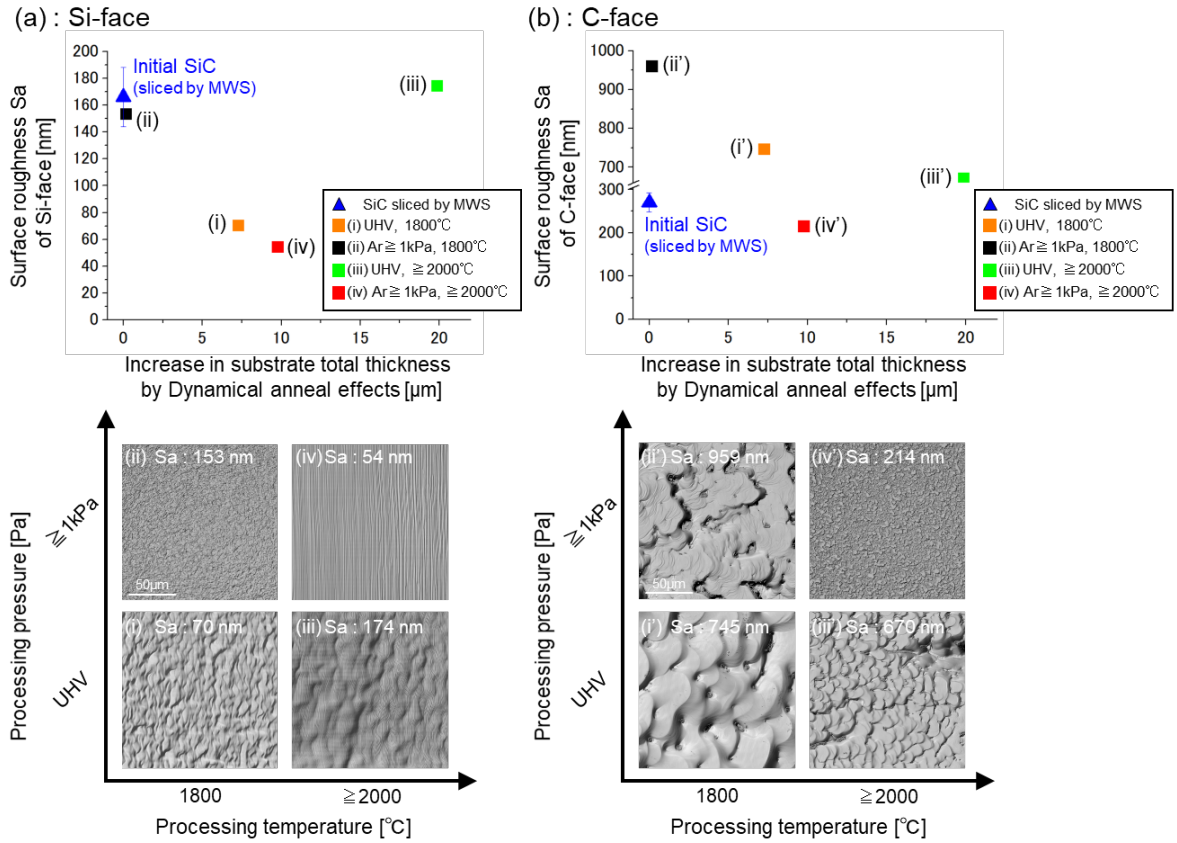

Fig. 4. Sa values on the (a) Si-, and (b) C-face and the total thickness variation of each substrate sliced by MWS (loose abrasive) due to the Dynamical anneal effect under four conditions of different temperature and pressure. Laser microscope images (i)-(iv), and (i')-(iv') representing the surface morphology after DA process under each condition.

of the substrate increased by 7.3 μm. As shown in Figs. 4 (ii) and (ii'), when the DA process was performed at low-temperature and high-pressure (1800 °C, Ar ≥ 1 kPa), the macroscopic roughness Sa of the Si- and C-face were 153 nm and 959 nm, respectively, and the thickness increase was 0.2 μm. Since the DA process in a high-pressure environment prevents the transport of molecules in the gas phase between the source and the substrate, it is expected to be material lossless and self-organization for a longer duration. As expected, the substrate thickness remained almost identical to the DA process, and material lossless was achieved. However, the Sa on the Si-face showed little improvement, and the value on the C-face increased by approximately 3.6 times. The DA process at low-temperature and high-pressure is insufficient for planarization on both sides. As shown in Figs. 4 (iii) and (iii'), when the DA process was performed at high-temperature and low-pressure (≥ 2000 °C, 10^{-5} - 10^{-7} Pa), the macroscopic roughness Sa of the Si- and C-face increased to 174 nm and 670 nm, respectively, and the thickness increase was 19.9 μm. The Sa on the Si-face improved little, while it increased by a factor of about 2.5 on the C-face. The high-temperature environment was expected to improve the planarity because of the intense sublimation and recrystallization reactions on both the etching/growth surfaces. However, due to excessively fast etching/growth rates, sufficient planarity could not be obtained. The DA process at high-temperature and high-pressure is desirable to control etching/growth rates. As shown in Figs. 4 (iv) and (iv'), when the DA process was performed at high-temperature and high-pressure (≥ 2000 °C, Ar ≥ 1 kPa), the macroscopic roughness Sa of the Si- and C-face decreased to 54 and 214 nm, respectively. It was decreased by about 100 nm on the Si-face and 60 nm on the C-face. As can be seen from the laser microscope image, a straight step-terrace structure was formed on the Si-face. This condition is the only one that can reduce roughness on the C-face, even where effective growth occurs. The total thickness of the substrate increased to 9.8 μm. Compared to the high-temperature and low-pressure conditions, the increase in total thickness could be reduced to about half. In summary, it was found that the largest Dynamical anneal effects are

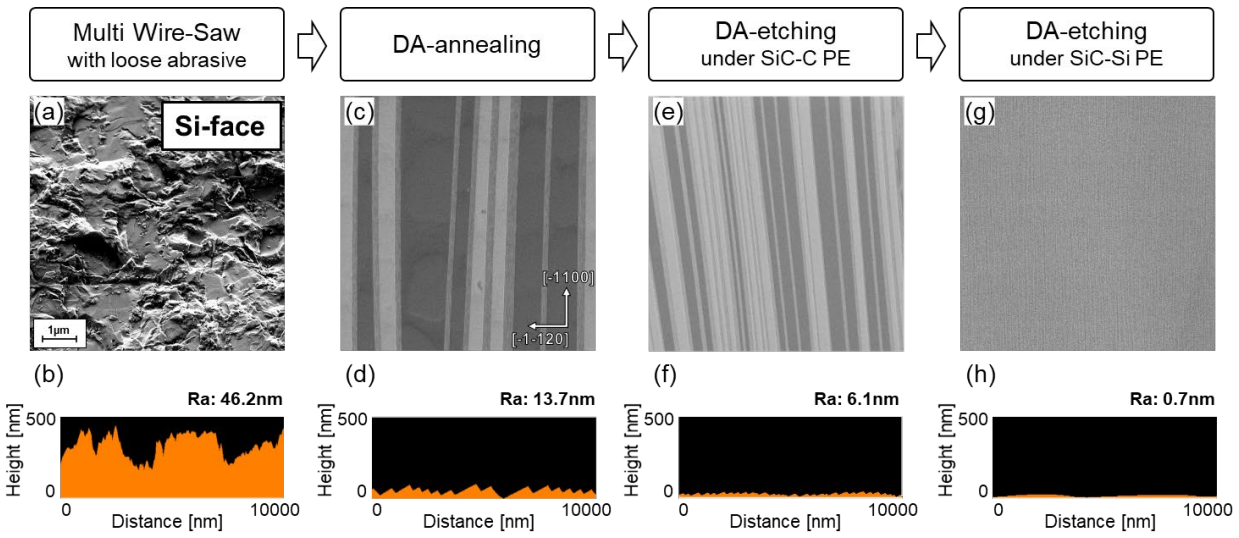

Fig. 5. SEM images of the Si-face (a), (c), (e), and (g) at each stage of the three-step DA process on the substrate sliced by MWS with loose abrasive and the cross-sectional height profiles (b), (d), (f), and (h) measured by AFM (10 μm × 10 μm).

obtained in high-temperature and high-pressure environments and that macroscopic planarization without material lossless is possible.

These results show that the DA process can achieve macroscopic planarization of as-sliced SiC wafers under high-temperature and high-pressure conditions. Therefore, we attempted to combine this DA-annealing with conventional DA-etching to achieve a CMP-free process. The procedure consisted of three steps. First, DA-annealing was performed on an as-sliced SiC wafer to obtain macroscopic planarity. DA-etching (1800 °C, 10^{-5} - 10^{-7} Pa) was then performed on SiC-C PE to improve the planarity further. Subsequently, DA-etching (1800 °C, 10^{-5} - 10^{-7} Pa) was performed on SiC-Si PE. The surface morphology of the wafer after each process was observed by SEM and AFM (10 μm × 10 μm) to investigate the planarity in the microscopic range. SEM image and cross-sectional profile of the Si-face of the initial as-sliced SiC wafer, as shown in Figs. 5 (a) and (b) indicated a very rough surface with Ra = 46.2 nm. The step-terrace structure, which reflects the crystal structure of SiC, could not be observed on the surface. DA-annealing on the wafer resulted in a linear morphology perpendicular to <11-20>, as shown in Figs. 5 (c) and (d). This indicated that a step-terrace structure was formed on the Si-face. The terrace width of the structure is about 1 μm, and the microscopic roughness Ra is significantly reduced to 13.7 nm. Furthermore, DA-etching on SiC-C PE shortened the terrace width of the step to about 300 nm, as shown in Figs. 5 (e) and (f). The microscopic roughness Ra was 6.1 nm, which is half that of the wafer after DA-annealing. Subsequently, when DA-etching was performed on SiC-Si PE, the terrace width of that step was decreased to about 14 nm, as shown in Figs. 5(g) and (h). Finally, the microscopic roughness Ra of the Si-face was significantly reduced to about 0.7 nm. It should be noted that there is a slight undulation in the surface profile obtained. Since it may be attributed to the increase in the Ra, the surface morphology of the Si-face should be improved. The SEM image and the cross-sectional height profile of the

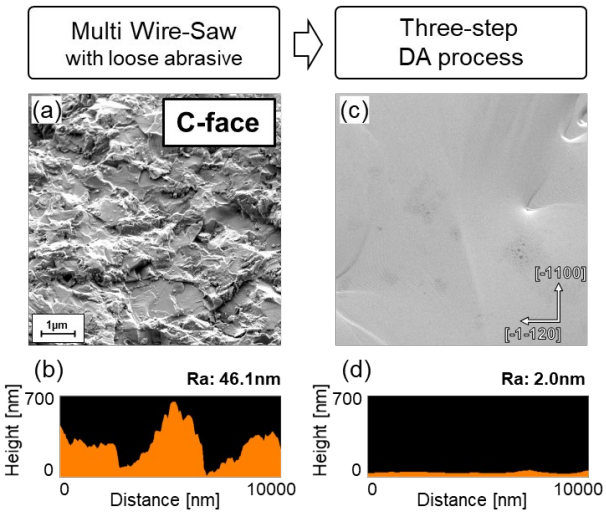

Fig. 6. (a), (c) SEM images and (b), (d) cross-sectional height profiles measured by AFM (10 μm × 10 μm) of the C-face of the sliced wafer before and after the three-step DA process, respectively.

C-face of an initial as-sliced SiC wafer are shown in Figs. 6 (a) and (b). The microscopic roughness Ra is 46.1 nm, indicating that the surface profile is quite rough, as well as the Si-face. DA-annealing and two types of DA-etching resulted in the formation of a step-terrace structure on the C-face, which is meandered. The microscopic roughness Ra was reduced to 2.0 nm, about 5 % of the initial Ra, indicating that the flatness was clearly increased.

Then, photographs of the Si-face of the as-sliced SiC wafer and the different wafer sliced from the same boule after the three-step DA process are shown in Figs. 7 (a) and (b). The wafer had low transparency and became a mirror surface by the DA process. After the DA process, the wafer container became visible through the wafer, indicating improved transparency. It should be noted that the wafer slightly remained with macro undulations that had formed during the slicing process. Photographs of the C-face of those wafers are shown in Figs. 7 (c) and (d). The transparency of the C-face of the as-sliced SiC wafer is also low. The DA process slightly increased its transparency. The DA process has a macro planarization function for both the Si- and C-face of as-sliced SiC wafers.

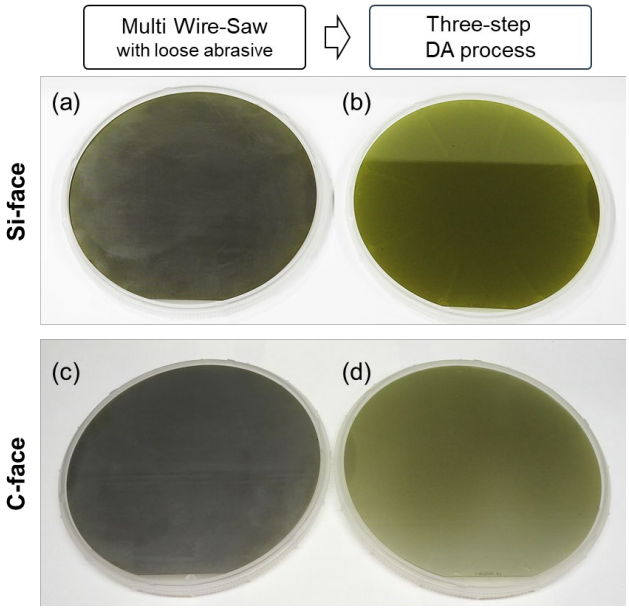

Fig. 7. Photographs of (a), (b) Si- and (c), (d) C-face wafers sliced by MWS (loose abrasive) and the three-step DA process, respectively. These are different wafers sliced from the same boule.

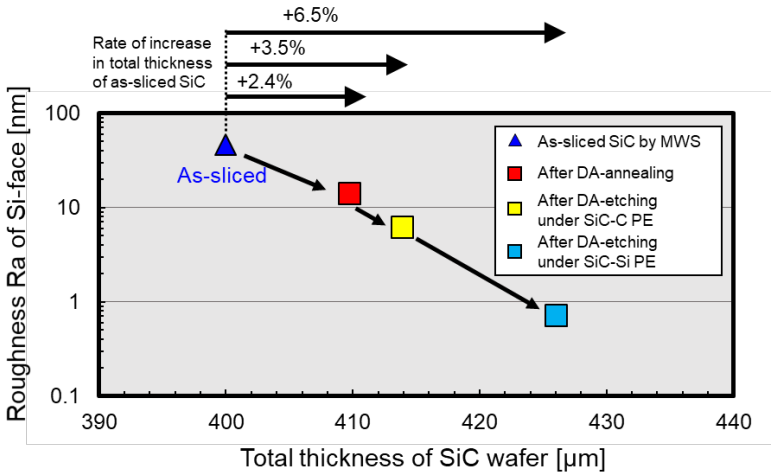

Fig. 8. a values acquired by AFM (10 μm × 10 μm) of Si-face and total thickness at each stage of the three-step DA process on the wafer sliced by MWS with loose abrasive.

The roughness Ra in the microscopic range of the Si-face and the total thickness of the substrate were measured at the three stages of the DA process, and the results are shown in Fig. 8. The initial thickness of the as-sliced SiC wafer used as a sample was 400.0 μm and its Ra was 46.2 nm. After DA-annealing, the thickness of the wafer increased to 409.8 nm. Furthermore, the thickness increased to 414.0 μm by DA-etching under SiC-C PE. Finally, DA-etching under SiC-Si PE increased its thickness to 426.1 μm and reduced Ra to 0.7nm. This result indicated that there was no material loss at all in the three-step DA sublimation process but rather an increase in wafer thickness. The increased thickness is because the chemical potential of a polycrystalline SiC container as source material is larger than that of monocrystalline SiC. The amount of source gas supplied from the polycrystalline SiC to the monocrystalline SiC is larger than that of sublimation from the wafer. In other words, the thickness of the wafer increases. As a result, the DA process can reduce the thickness required for a

single as-sliced SiC wafer. It suggests that it is possible to slice a larger number of SiC wafers from a boule of limited height.

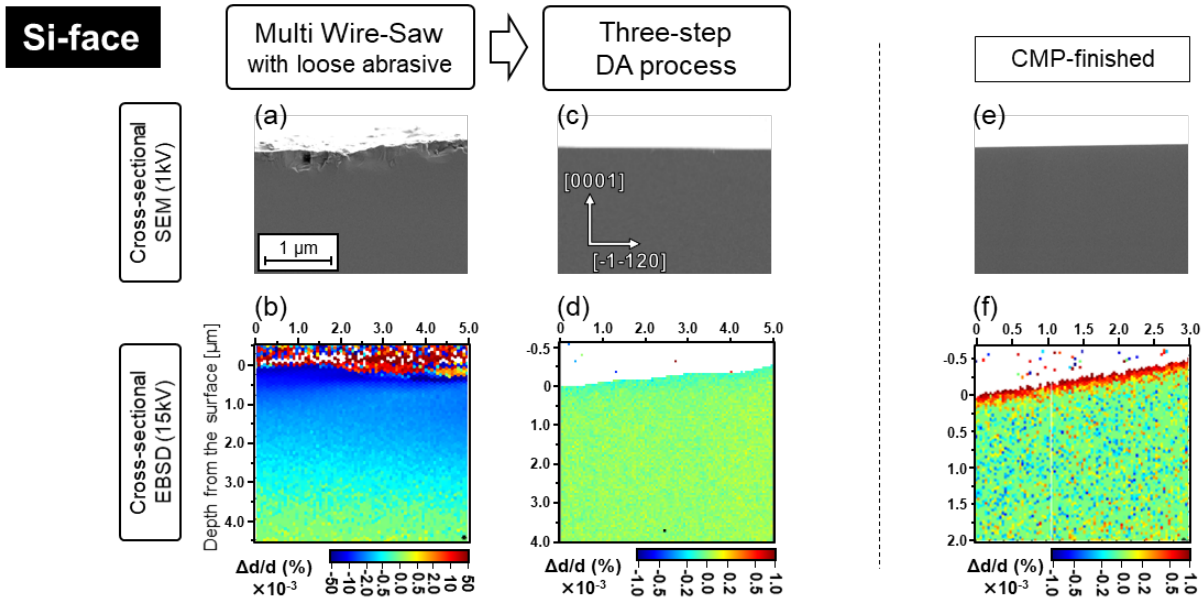

Fig. 9. Cross-sectional SEM images and Cross-sectional EBSD uniaxial strain mapping images measured at 15 kV acceleration voltage near the Si-face of (a), (b) the SiC substrate sliced by MWS with loose abrasive, (c), (d) the sliced substrate after the three-step DA process, and (e), (f) the CMP-finished SiC, respectively.

Finally, cross-sectional SEM and EBSD were measured to examine the magnitude and distribution of SSD near the Si-face of the wafer after the three-step DA process. Figs. 9 (a), (c), and (e) show cross-sectional SEM images of initial as-sliced SiC, as-sliced SiC after the process, and CMP-finished SiC. The irregularities of several hundred nm can be observed on the Si-face of the as-sliced SiC due to the slicing process. The morphology was not observed from the cross-sectional SEM image after the DA process, and the flatness was comparable to that of CMP-finished SiC obtained by the conventional machining process. Cross-sectional EBSD normal strain mapping images of these substrates using EBSD (acceleration voltage of 15 kV) are shown in Figs. 9 (b), (d), and (f). The lattice strain Δd/d (d: lattice constant) is shown in color scale. SSDs were introduced into the as-sliced SiC deeper than about 3.0 μm from the Si-face. It was much deeper than the depth of the irregularities that can be seen in the cross-sectional SEM image. Compared to CMP-finished SiC, fewer SSDs can be seen on the Si-face of the wafer after the DA process. It is also considered that DA-annealing removes the SSD of the C-face as well as the Si-face. The DA sublimation process, which does not involve physical contact, indicated that removing the SSD introduced during slicing is possible and ensures sufficient planarity without introducing a new SSD.

Summary

This study demonstrates that the macro and micro flatness of 4H-SiC wafers can be significantly improved by DA-annealing, a DA process in a high-temperature (≥ 2000 °C) and high-pressure (≥ 1 kPa) environment. DA-annealing on SiC wafers sliced from boules resulted in a significant reduction in surface roughness on both the Si- and C-face and an increase rather than a decrease in overall wafer thickness. This reduced the macroscopic roughness Sa acquired by laser microscopy from 166 nm to 54 nm on the Si-face and from 270 nm to 214 nm on the C-face. Further planarity improvement was achieved in the subsequent DA-etching process in the SiC-C and SiC-Si PE. As a result, with respect to the microscopic roughness Ra obtained by AFM, the Si-face decreased from 46.2 nm on the as-sliced wafer to 0.7 nm, and the C-face decreased from 46.1 nm to 2.0 nm. Cross-sectional EBSD analysis also confirmed that the distribution of SSD near the Si-face of the wafer was reduced to below the measurement limit, and the quality of the wafer was improved. The results of these studies suggest that non-contact DA processes, including DA-annealing, can be combined with

conventional mechanical processes to effectively improve the surface morphology and crystal quality of SiC wafers. It indicated the potential of applying this novel non-contact style thermal planarization technique for rough SiC wafers to the mechanical process. It should be noted that the slight undulation of the Si-face and the roughness of the C-face that occurs on the wafer during this process need to be improved. Our future work is to solve the problems of this research such as undulation of Si-face and roughness of the C-face.

Acknowledgments

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