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Study on Homoepitaxy Performance of Engineered 150 mm and 200 mm SiC Substrates in a Multi-Wafer Batch Reactor

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Abstract. Engineered SiC wafers with a thin 4H-SiC layer bonded on a polycrystalline carrier substrate for the application as substrate in epitaxy are investigated. Epitaxial layers grown on such substrates in 150 mm and 200 mm diameter are compared to those on state-of-the-art conventional substrates from different vendors. The performance of the engineered wafers is judged by doping and thickness uniformities as well as the number and statistics of killer defects in the epitaxial layer.

Introduction

The fast growth of the silicon carbide (SiC) power device market is relying on a sufficient supply of high quality SiC substrate wafers to achieve low epi defect numbers [1]. A reduction of monocrystalline SiC material usage for substrates is highly desirable to reduce device and material costs and secure a steady supply chain. One strategy, among others, is to use a very thin 4H-SiC layer bonded onto a mechanical carrier. These so-called engineered substrates are regarded as sufficient for epitaxy and device production.

In addition to reduced SiC crystal consumption, the device performance can be improved further thanks to lower conduction and switching losses [2] in the device using ultra high conductivity receiver substrates. SOITEC's SmartCut™ process [3] uses such a below 1 µm thin monocrystalline SiC layer, which is transferred to a polycrystalline SiC carrier substrate [4] and bonded utilizing a conductive bonding.

This study extends a benchmark performed on early samples [5] and looks more into the feasibility for high volume manufacturing using a full cassette to cassette (C2C) epitaxy line. Sets of current generation 150 mm and 200 mm SOITEC engineered substrates will be compared with industry standard bulk wafers from multiple vendors.

Experimental

In this benchmark study we are aiming to compare SOITECs SmartSiC™ engineered SiC substrates in 150 mm and 200 mm diameter as well as SOITEC Advanced SiC Engineered Substrates in 150 mm (abbreviated to "Soitec Advanced" in the graphs) to comparable monocrystalline substrates from four industry standard suppliers. These reference wafers were supplied partially by the TRANSFORM project partner STMicroelectronics, and partially bought from three external vendors:

- 150 mm: prime grade from vendor A and vendor B
- 200 mm: prime grade from vendor A and vendor C

From SOITEC we received different generations of their engineered substrates to be included:

- 150 mm: SmartSiC™ and Advanced SiC Engineered Substrates
- 200 mm: SmartSiC™

The epitaxy was performed in AIXTRON G10-SiC reactors in 9x150 mm and 6x200 mm configurations respectively. This allows a direct comparison between different substrates in the same process run under the same conditions and epitaxy process parameters. Two runs per substrate diameter were performed with the different substrate types distributed over both runs per diameter. Like this a total number of 18 wafers of the 150 mm size and 12 wafers of the 200 mm size were included in this study.

Table 1. Overview of substrate vendors and number of substrates included in this study

Vendor/type	**150 mm**	**200 mm**
SOITEC SmartSiC	4x	3x
SOITEC Advanced	4x	---
STMicroelectronics	4x	3x
Vendor A	3x	3x
Vendor B	3x	---
Vendor C	---	3x

On both substrate diameters, a 1µm thick buffer with a 1.0E18 cm^{-3} doping level was grown, followed by a 15 µm thick drift layer. This was doped at 1.0E16 cm^{-3} and 1.8E16 cm^{-3} on 150 mm and 200 mm respectively.
After epitaxy, all wafers were then characterized regarding epilayer thickness and doping concentrations by FTIR spectrometry and mercury probe capacitance-voltage (C-V) measurements, respectively. All wafers were characterized with ultraviolet photo luminescence (UVPL) imaging and surface inspection with a Lasertec SICA88 system to obtain the defect statistics. For all characterization methods an edge exclusion of 5 mm was applied.
The defect scans on the SmartSiC™ wafers were performed with slightly changed settings compared to the conventional substrates. This was done to adopt the defect recognition to the different surface morphology of the epilayer on the engineered substrates [5]. Main changes were a reduced brightness of the differential interference contrast channel and shifted thresholds for the adaption and optimization of the defect recognition algorithm. Due to this, there is no reliable detection of small surface defects like micropits and bumps on epilayers on SmartSiC™ substrates.

Wafer behavior in process

The AIXTRON G10-SiC reactor type used in this study is equipped with a full cassette-to-cassette automated wafer handling and loading system. All wafers were loaded and unloaded using the automated system at elevated temperatures. No problems occurred during these procedures and the engineered substrates can be handled using the automated system.

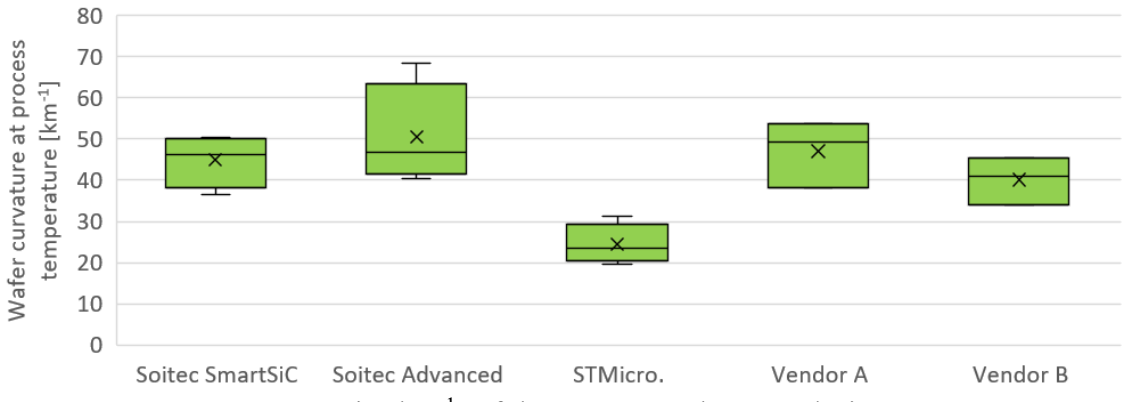

Fig. 1. Curvature in [km^{-1}] of the 150 mm substrates during process.

The AIXTRON systems also allow to measure the wafer curvature during the epitaxy at full process temperature. This allows to judge the substrates for internal strain and the potential risk of breakages or wafer slipping due to excessive curvature.
All 150 mm wafer exhibited a curvature between 20 km^{-1} and 70 km^{-1} under epitaxy process conditions (see Figure 1). On the 200 mm substrates we observed curvatures in a window of +/- 45 km^{-1} around the average for all the monocrystalline wafers, with the SOITEC SmartSiC™ substrates showing less curvature at roughly 90 km^{-1} lower than the average of standard wafers under the same conditions. All wafers stayed in the expected range of curvature during process and no slippage was detected.

Epilayer characterization on 150 mm substrates

Doping and Thickness: For this comparison between standard substrates and engineered wafers we are not only looking at defect performance and predicted device yield but also at the doping and thickness uniformity. As seen in Figure 2 and Figure 3, which show two substrates processed in the same epitaxy run, the performance in the doping uniformity is very good and comparable between conventional and engineered substrates on 150 mm.

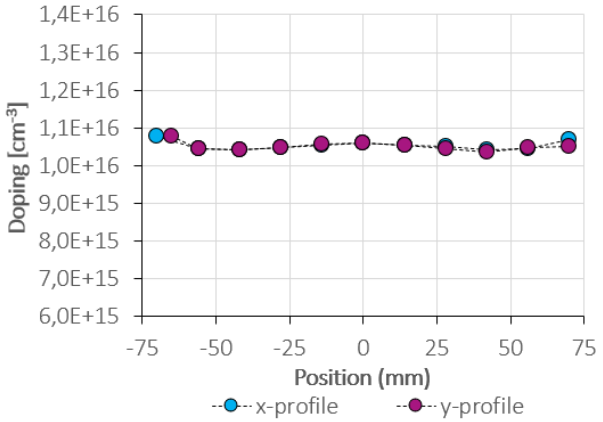

Fig. 2. Doping uniformity on a 150 mm conventional reference wafer from STMicroelectronics. At a mean doping of 1.05E16 cm^{-3} the uniformity is 1.05 % sigma/mean.

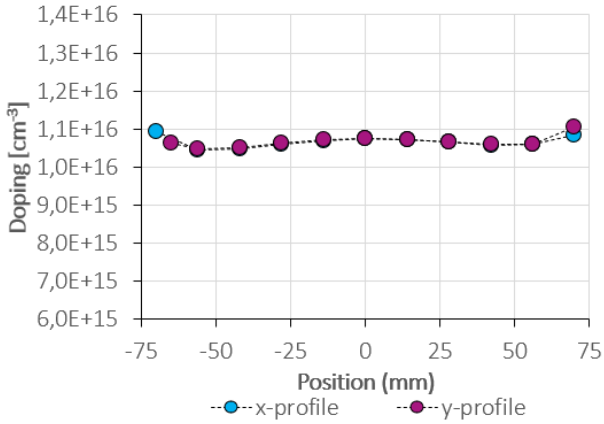

Fig. 3. Doping uniformity on an engineered 150 mm SmartSiC™ wafer from Soitec. At a mean doping of 1.07E16 cm^{-3} the uniformity is 1.34 % sigma/mean.

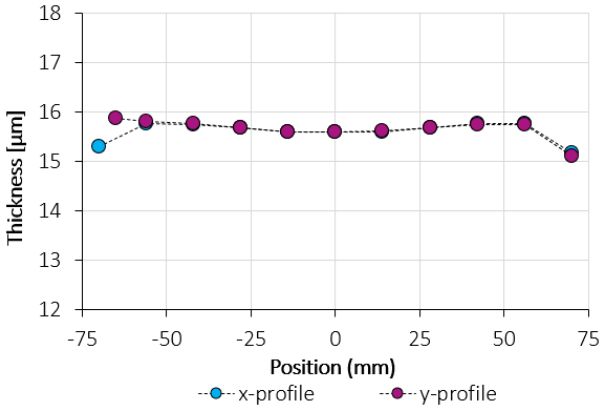

Fig. 4. Thickness uniformity on a 150 mm conventional reference wafer from STMicroelectronics. At a mean thickness of 15.64 µm the uniformity is 1.27 % sigma/mean.

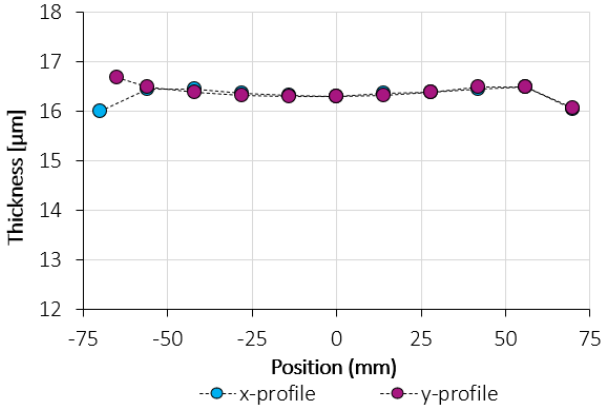

Fig. 5. Thickness uniformity on an engineered 150 mm SmartSiC™ wafer from Soitec. At a mean thickness of 16.36 µm the uniformity is 0.96 % sigma/mean.

The same comparability is evident on the thickness measurements. In Figure 4 and Figure 5 are two thickness profiles from a standard substrate and a SOITEC SmartSiC™ substrate. While the uniformities are comparable in the range of the measurement error, we can see a slight artefact in the average thickness measured on the engineered substrate, as the FTIR systems makes its fit to the bonded interface. Due to this the epitaxial layer appears thicker by 0.6 µm, which equals the bonded single crystalline layer. This must be accounted for in tuning the epitaxial process.

Defects: In Figure 6 you can see a boxplot of the killer defect density. Counted here are polytype inclusions, stacking faults, PL stacking faults, propagated stacking faults and downfalls. One can see that the SmartSiC™ substrates perform on par with the monocrystalline substrates when looking at the total killer defect density.
The substrates from STMicroelectronics and from vendor A had one outlier wafer each with a higher killer defect density. Excluding those outliers, vendor A would perform the best in this factor.

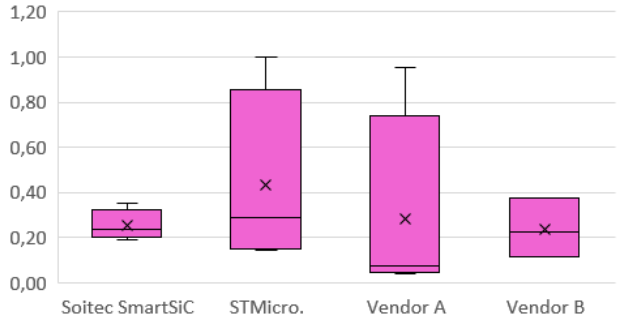

Fig. 6. Normalized killer defect density on 150 mm with the worst wafer in the study set to unity. Counted are polytype inclusions, stacking faults, PL stacking faults, propagated stacking faults and downfalls.

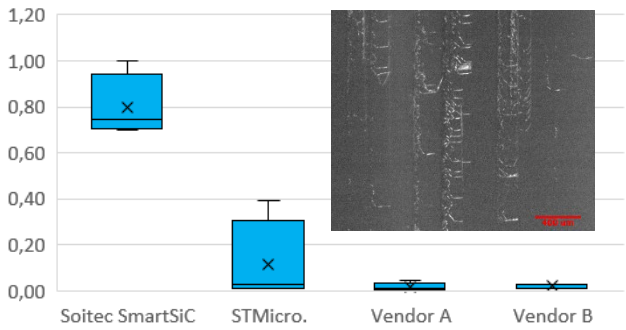

Fig. 7. Normalized BPD density on 150 mm with the worst wafer in the study set to unity. The insert shows BPDs within bar shaped stacking faults on SmartSiC™.

The density of basal plane dislocations (BPDs) appears to be very high in the epilayers on SmartSiC™ substrates (Figure *7*). This could be assigned to a faulty defect recognition and dislocation features connected mainly to bar shaped (propagated) stacking faults.

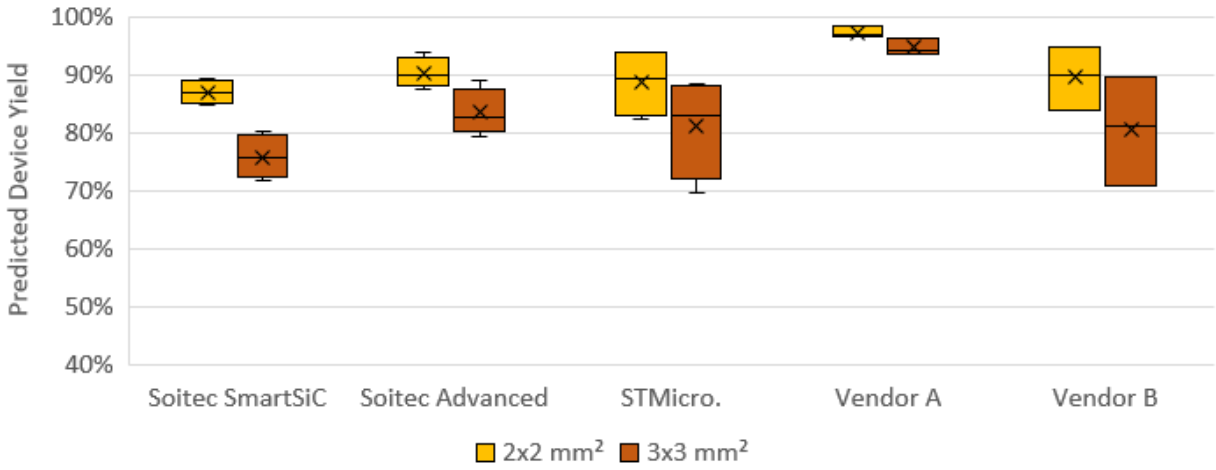

Fig. 8. Projected device yield for 2x2 mm² and 3x3 mm² on epilayers on the tested 150 mm substrates of different vendors.

The SOITEC Advanced SiC Engineered Substrates were not included in the statistics for the killer defects. This decision was made as these are early prototypes that still show some bonding failures leading to localized polycrystalline growth in the epi process. These poly regions cannot be analyzed with the automated Lasertec system as there is a high number of false recognitions. But as these poly regions only make up a small part of the wafer, we can still look at the projected yield, as only a few devices would be affected.

Despite these small areas with polycrystalline growth the SOITEC Advanced SiC Engineered Substrates give a higher predicted yield both on 2x2 mm² and 3x3 mm² grids compared to the SmartSiC™ substrates (see Figure *8*). STMicroelectronics substrates and wafers from vendor B have a wider spread, but in general perform on a similar level to the SOITEC SmartSiC™ engineered substrates. Vendor A is superior though when it comes to predicted device yield and the consistency of the results.

Epilayer Characterization on 200 mm Substrates

Doping and Thickness: As seen in Figure 9 and Figure 10, which show two 200 mm substrates processed in the same epitaxy run, the performance in the doping uniformity is very good and comparable between conventional and engineered substrates.

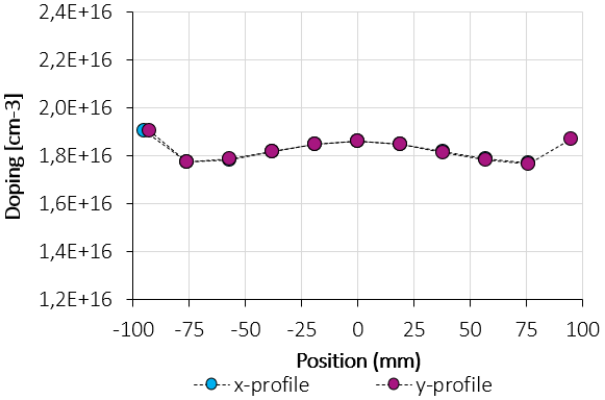

Fig. 9. Doping uniformity on a 200 mm conventional reference wafer from STMicroelectronics. At a mean doping of 1.82E16 cm^{-3} the uniformity is 2.36 % sigma/mean.

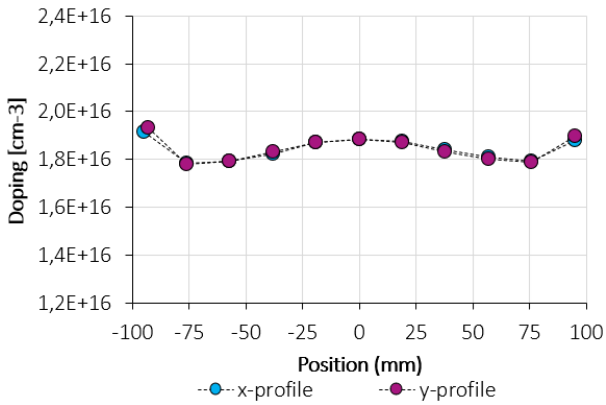

Fig. 10. Doping uniformity on an engineered 200 mm SmartSiC™ wafer from Soitec. At a mean doping of 1.84E16 cm^{-3} the uniformity is 2.48 % sigma/mean.

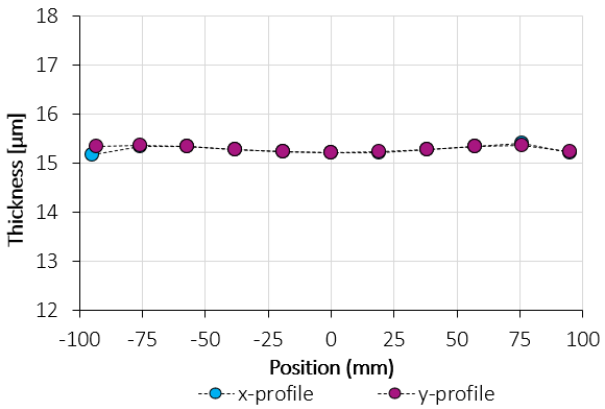

Fig. 11. Thickness uniformity on a 200 mm conventional reference wafer from STMicroelectronics. At a mean thickness of 15.29 µm the uniformity is 0.42 % sigma/mean.

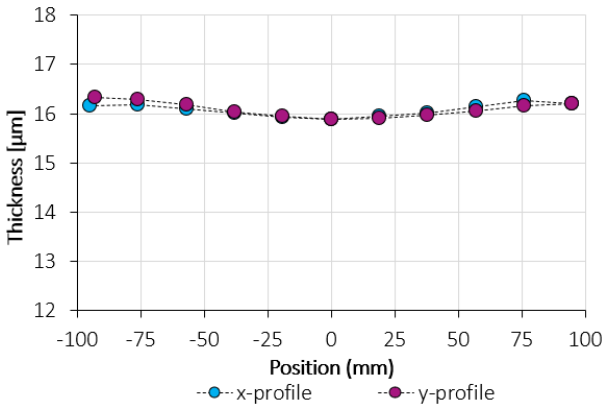

Fig. 12. Thickness uniformity on an engineered 200 mm SmartSiC™ wafer from Soitec. At a mean thickness of 16.09 µm the uniformity is 0.81 % sigma/mean.

In the thickness measurements the same offset applies as for the 150 mm substrates. In Figure 11 and Figure 12 are two thickness profiles from a standard substrate and a SOITEC SmartSiC™ substrate. While the uniformities are comparable in the range of the measurement error, we can see a deviation in the average thickness measured on the engineered substrate. This makes the epitaxial layer appear thicker by 0.8 µm due to the included bonded single crystalline layer. This must be accounted for in tuning in the epitaxial process.

Defects: In Figure 13 you can see a boxplot of the killer defect density. Counted here are polytype inclusions, stacking faults, PL stacking faults, propagated stacking faults and downfalls. One can see that the 200 mm SmartSiC™ substrates perform on par with the monocrystalline substrates from STMicroelectronics and vendor C when looking at the total killer defect density. Vendor A shows a lower killer defect density in the epilayer.

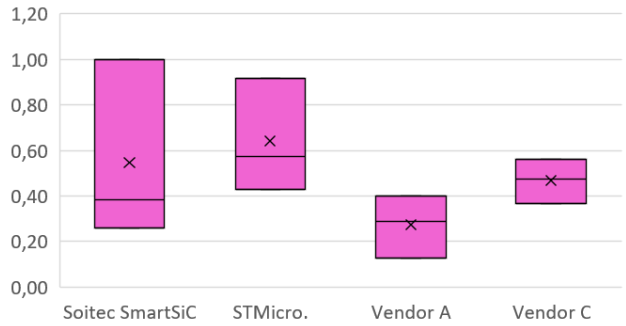

Fig. 13. Normalized killer defect density on 200 mm with the worst wafer in the study set to unity. Counted are polytype inclusions, stacking faults, PL stacking faults, propagated stacking faults and downfalls.

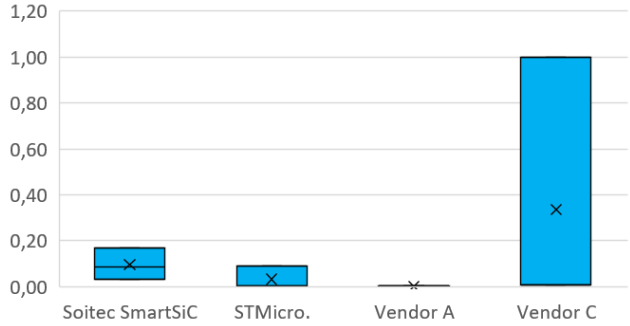

Fig. 14. Normalized BPD density on 200 mm with the worst wafer in the study set to unity.

Most of the standard monocrystalline substrates perform well in respect to BPDs (Figure 14), except for one significant outlier wafer on vendor C. Epilayers on the 200 mm SmartSiC™ substrates exhibit a slightly higher count of BPDs than the average.

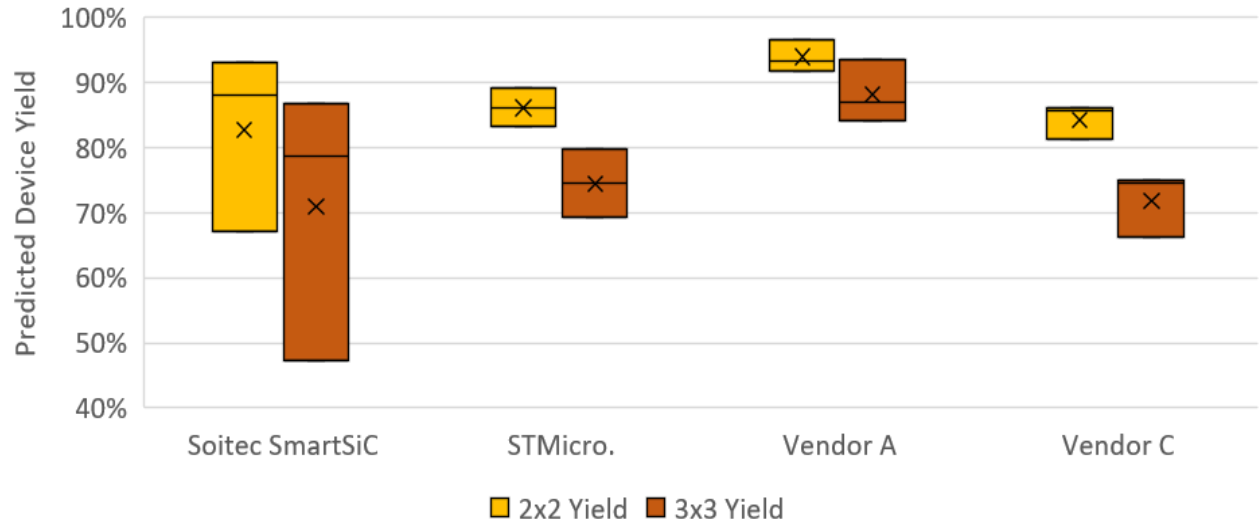

Fig. 15. Projected device yield for 2x2 mm² and 3x3 mm² on epilayers on the tested 200 mm substrates of different vendors.

While having a larger spread of yield – likely due to the early prototype status of the used substrates – the 200 mm SmartSiC™ showed an average yield comparable to STMicroelectronics and vendor C conventional substrates (Figure 15). Like the performance on 150 mm, we can also see the best predicted yield on 200 mm substrates from vendor A.

Vendor Fingerprints in Defects

The following graphs (Figure 16 to Figure 25) show a relationship of some relevant defects between three substrate types (SmartSiC™, STMicroelectronics and vendor A) in 150 mm and 200 mm sizes. One can see that the different manufacturers have a certain "fingerprint" in the distribution of defects. SOITEC's Advanced SiC Engineered Substrates, vendor B and vendor C are not included in this section as they were not available in both substrate diameters.

Stacking Faults and Polytype Inclusions: SOITEC and vendor A show a lower number than STMicroelectronics

PL Stacking Faults, Propagated Stacking Faults and BPDs: SOITEC has the highest density, followed by STMicroelectronics and with vendor A the best

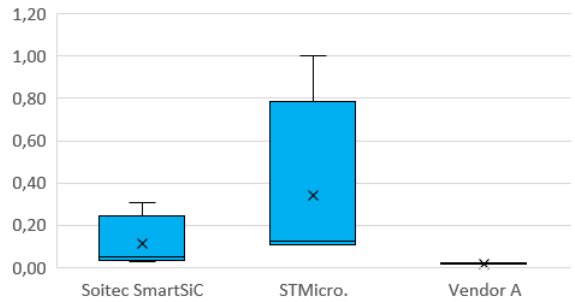

Fig. 16. Normalized Stacking Fault density on 150 mm substrates from different vendors with the worst wafer set to unity.

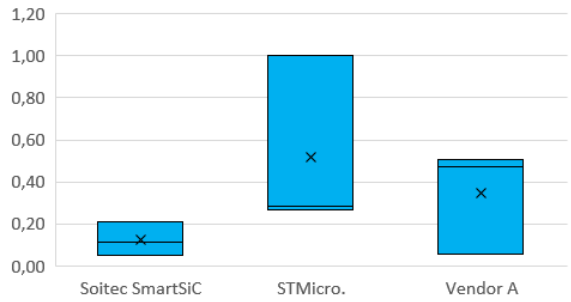

Fig. 17. Normalized Stacking Fault density on 200 mm substrates from different vendors with the worst wafer set to unity.

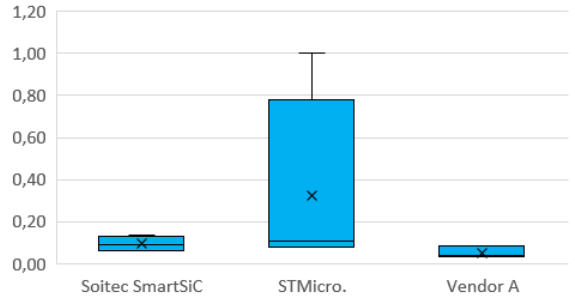

Fig. 18. Normalized Polytype Inclusion density on 150 mm substrates from different vendors with the worst wafer set to unity.

Fig. 19. Normalized Polytype Inclusion density on 200 mm substrates from different vendors with the worst wafer set to unity.

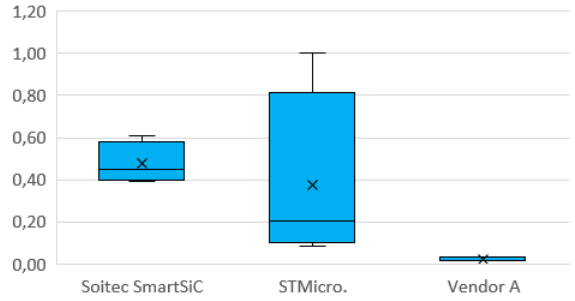

Fig. 20. Normalized PL Stacking Fault density on 150 mm substrates from different vendors with the worst wafer set to unity.

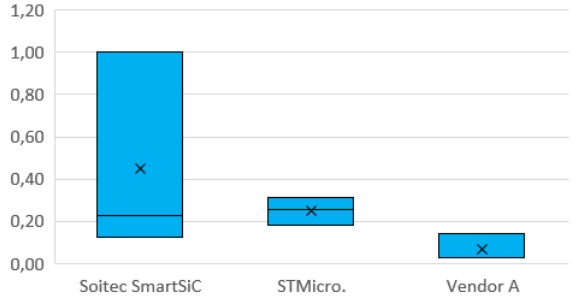

Fig. 220. Normalized PL Stacking Fault density on 200 mm substrates from different vendors with the worst wafer set to unity.

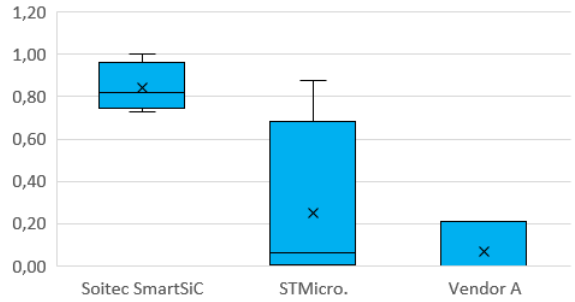

Fig. 22. Normalized Propagated (Bar Shaped) Stacking Fault density on 150 mm substrates from different vendors with the worst wafer set to unity.

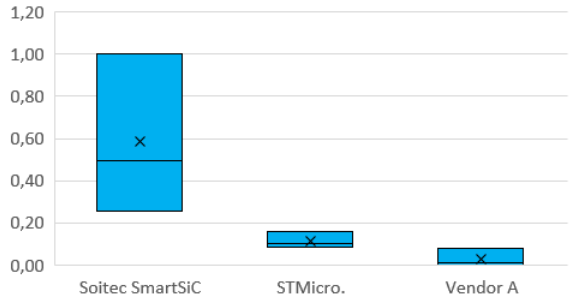

Fig. 23. Normalized Propagated (Bar Shaped) Stacking Fault density on 200 mm substrates from different vendors with the worst wafer set to unity.

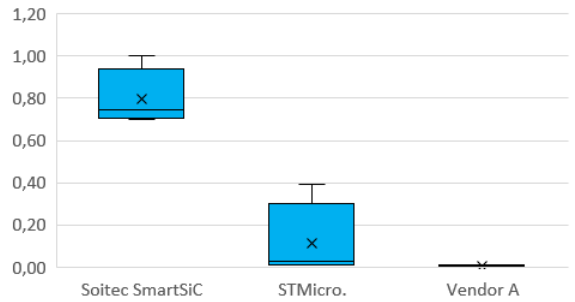

Fig. 24. Normalized BPD density on 150 mm substrates from different vendors with the worst wafer set to unity.

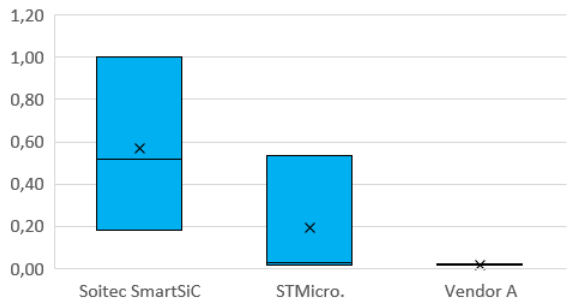

Fig. 21. Normalized BPD density on 200 mm substrates from different vendors with the worst wafer set to unity.

Summary

Across both substrate diameters we have observed a very similar performance of the SOITEC engineered substrates compared to conventional substrates from different industry vendors. Doping performance in average level and uniformity is not affected by the substrate type. Thickness uniformity is also not affected while we see an offset in the average layer thickness caused by the bonded layer, which gets included in the fit of the FTIR data. Epitaxy defects cause a certain yield loss. Here SmartSiC™ substrates perform on par with STMicroelectronics and vendors B and C. Vendor A typically delivers the best defect performance in this comparison. The fact that ratios of defects between different suppliers seem very similar between 150 mm and 200 mm indicates that the defect performance is mainly given by the crystal and surface quality and not dominated by outliers and random effects.

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