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A Study of Epitaxial Growth on 4H-SiC Substrates Treated by Plasma Polish Dry Etch (PPDE) Process

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Abstract. We studied the impact of plasma polish dry etch (PPDE) on SiC substrates and its effect on epilayers grown on PPDE treated substrates. PPDE treatment on chemo mechanical polished (CMP) surface shows no significant degradation in surface roughness even with 3μm removal. On the other hand, when a mechanical polished (MP) surface was treated by PPDE, surface roughness was improved, demonstrating that PPDE can smooth a rough surface post MP process. Selective etching of threading screw dislocations (TSD) was evident from pit formation on the substrate surface. These pits may generate extended structural defects (e.g. triangular defects) during the epilayer growth depending on the sizes of the pits. No evidence was found that PPDE selectively etched BPD in the substrate and, hence, no improvement in BPD conversion was seen after epilayer growth. Ideally, PPDE treated surface pits needed to be minimized at TSD sites and mild etching at BPD sites is preferable and subject to future optimization.

Introduction

Silicon carbide is an important material for high voltage applications due to its various exceptional electrical and mechanical properties. To achieve reliable high voltage devices, however, defect-free epitaxy is essential. On the other hand, to achieve epitaxy with low defect counts, it is essential to optimize substrate surface preparation prior to epilayer growth. During the wafer processing, e.g. grinding, polishing etc., the substrate is damaged by scratches. This damaged surface is planarized by chemical mechanical polishing (CMP) to achieve a smooth scratch-free surface. Even though the surface is very smooth after CMP (roughness <0.1nm RMS), it is expected that some subsurface damage [1] is still present. Conventionally, hydrogen etching is used prior to the epilayer growth to create atomic steps on the surface. However, etching may not remove adequate material to eliminate subsurface damage due to its low removal rate in conventional epitaxial process.

Subsurface damage has been discussed earlier [2, 3]. Efforts have been made to mitigate subsurface damage by so called "Dynamic Aging", where the substrate is treated at a high temperature [3], have been shown to be beneficial for the reduction of basal plane defects (BPDs) and stacking fault (SF) defects in epitaxy. As an alternative to chemo-mechanical polishing, plasma polish dry etch (PPDE) is currently gaining attention [4] with the potential benefit of removal of subsurface damage. Plasma etching has well known applications in semiconductor industries, especially as a part of lithographic steps during device fabrication [5, 6]. High speed plasma etching on SiC has also been demonstrated [7]. However, detailed study of plasma etching on SiC substrates in terms of defects and their impact on epitaxial growth is not well known. In this research, we explore the effect of plasma polish dry etching (PPDE) on 4H-SiC substrates (4° off cut) and study its effect on epitaxial growth.

Experimental

SiC wafers (150mm diameter) were selected from multiple boules to eliminate any effect due to boule-to-boule variations. We divided these wafers into three groups as: mechanical polished wafers or MP, CMP, CMP+PPDE, MP+PPDE and hereby use these abbreviations in this manuscript. Here, plasma polish dry etching (PPDE) was performed using a PlasmaPro 100 Cobra tool from Oxford Instruments [4]. Plasma etch process atomic force microscopy (AFM) was used to measure surface roughness of these wafers prior to and after plasma etching. Finally, epitaxy was grown on these wafers using a commercial epi reactor with fixed growth conditions (thickness target 11µm and doping target 8e15cm^{-3}). The shape of these wafers was measured using a Tropel Ultrasort and defects were characterized by a SiCA88 tool.

Results

We studied shape, roughness, and surface of the plasma etched wafers. From the total thickness of the wafer, we found that ~3um of SiC was removed from the surface by the plasma etching process [Fig. 1 a]. We observed a positive shift in the wafer bow after the plasma treatment [Fig. 1b]. This indicates that PPDE imparting additional stress to the Si face of the wafers. This may be due to a small-scale increase in surface roughness after PPDE. Further study is needed to understand this bow change after PPDE. On the other hand, bow of the epi wafer did not increase further after epilayer growth but, contrarily, the bow reduced. Epilayer bow for PPDE treated wafer was found to be comparable to the epilayer grown on non PPDE treated substrates. It is likely that the residual stress induced by PPDE was removed during epitaxial growth process in a high temperature and H_2 ambient.

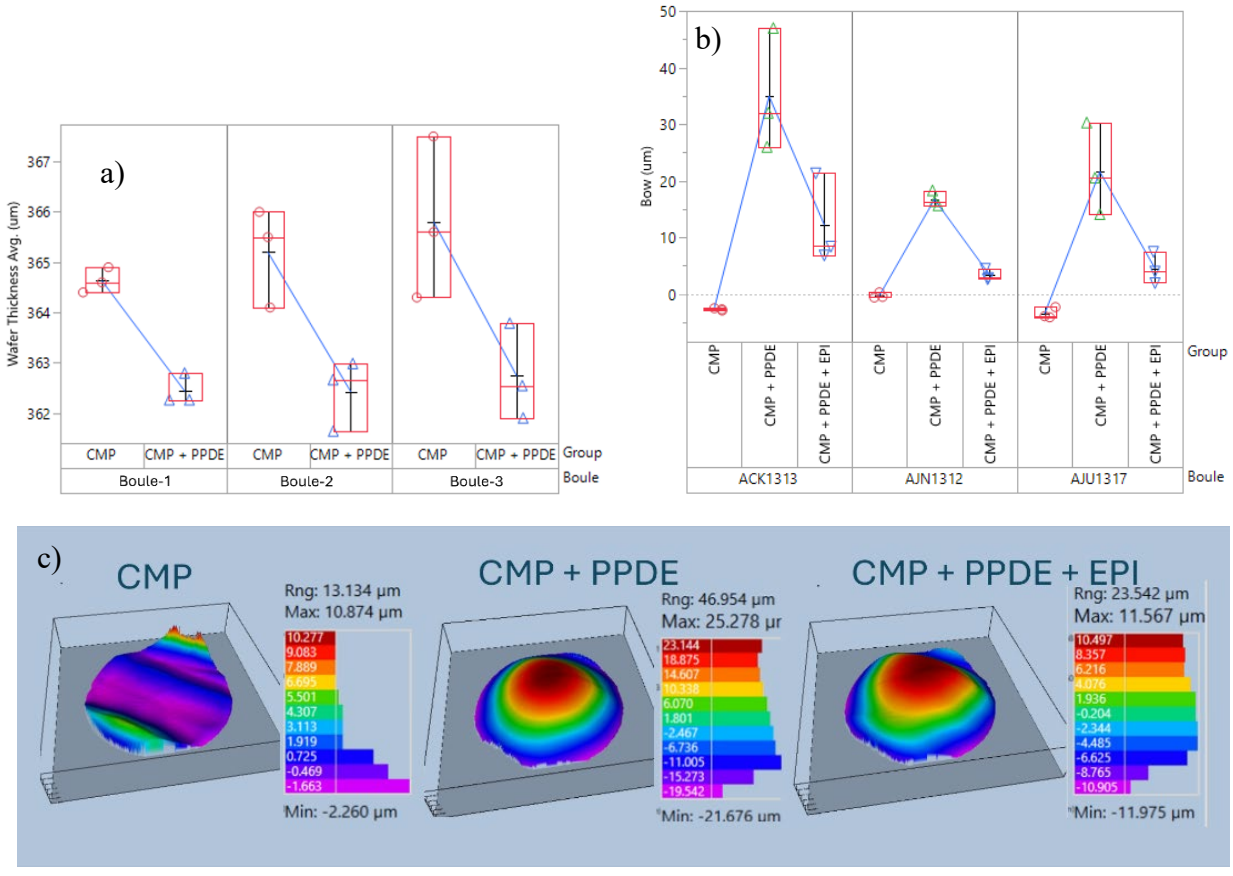

Fig. 1. a) Substrate thickness measurement shows ~3 µm removal after plasma dry etch. b) The substrate bow increases up to ~26 um after the plasma dry etching process but reduced after the epi run. c) Comparative images of the bow of the substrates for CMP, CMP + PPDE and CMP+ PPDE + EPI wafers.

When comparing roughness for CMP and CMP+PPDE substrates, we did not see a significant difference between the treatment techniques (Fig. 2). This indicates that the PPDE process does not add damage to the CMP surface. On the other hand, we found that when PPDE was performed on MP wafers, there was improvement in roughness of the surface. This indicates that PPDE has a potential to replace CMP polish for surface smoothing after MP. Post epitaxial surface roughness on epilayers grown on PPDE treated wafers were also found to be comparable to the non PPDE treated wafers (Fig. 2).

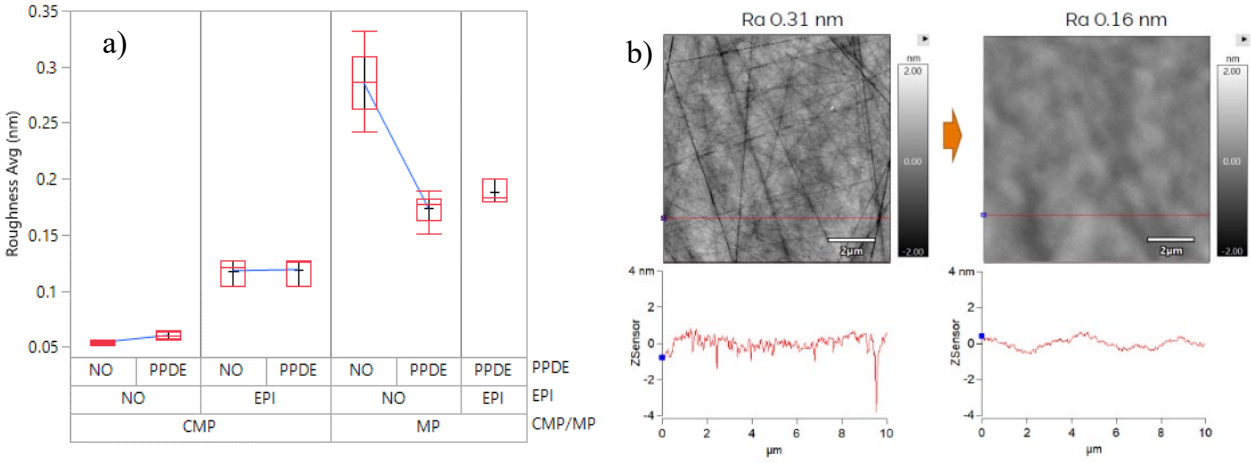

Fig. 2. AFM study demonstrates that roughess of the substrate treated by PPDE closely matches to the roughness of the CMP surface, showing plasma etch does not degrade the surface significantly. On the other hand, roughness of the surface was reduced significantly by plasma etching of a mechanically polished (MP + PPDE) surface. Post epi surface roughness of PPDE treated surfaces was also comparable to surface roughness of epilayers grown on non PPDE treated surfaces. b) AFM image on the MP substrate (left) and after treated by PPDE (right) showing surface smothing.

We studied defects on the PPDE treated substrates and their effect on consequently grown epilayers. We observed an increase in surface pits on the PPDE treated surface (Fig. 3). In the PL image we see TSDs as black dots (confirmed by KOH etch). Typically, TSDs are seen only in PL images as black dots (Fig 3a) in CMP treated surface and they are not seen in surface image (Fig 3b). Similar black dots are seen in PL image after PPDE (Fig. 3c), however, unlike CMP surface, pits are seen at the same location (Fig. 3d). We found that not all TSDs are converted into pits after PPDE. We believe whether PPDE creates etch-pits or not will depend on the sizes of the dislocation and upon plasma etch conditions. Further detailed study is required to understand when certain types of TSDs generate pits after PPDE and the effect of plasma etch conditions, which will be a topic of our future research.

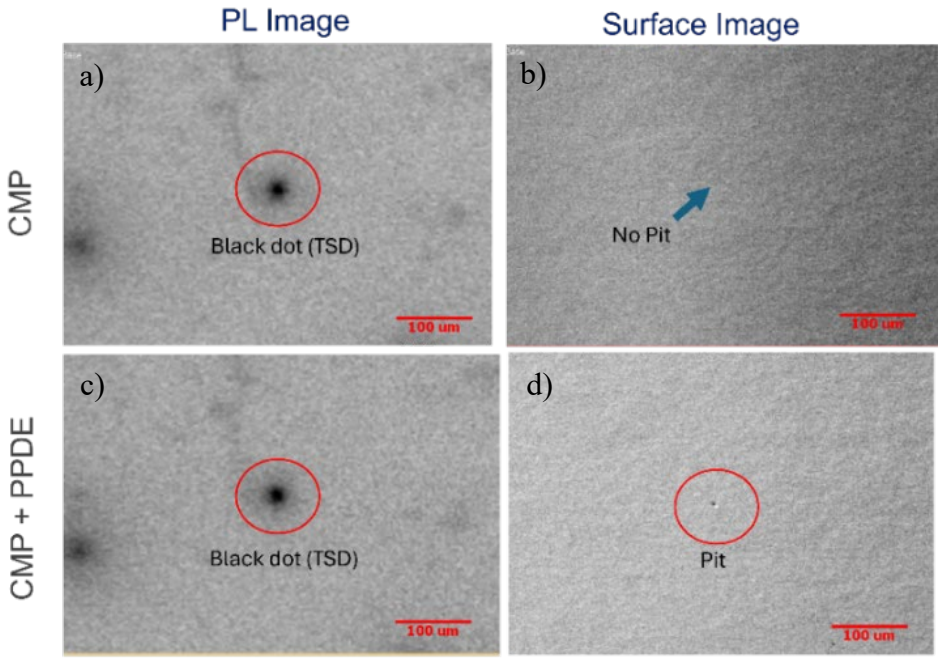

Fig. 3. a) Black dot is seen in the PL image on the substrate prior to epilayer but b) no pit is seen as the surface was planarized by CMP. c) black still exist in the PL image after PPDE treatment. d) PPDE generates a pit at the black dot location seen in the surface image.

We found that most of these pits translated into the epilayer as pits. Some, however, acted as a source of triangular defects and related stacking faults in the epilayer (Fig. 4, 5). Hence, it is essential to reduce TSD related pit formation on the substrate by PPDE by optimization of the plasma process. On the other hand, mild etch pit creation at BPD sites may be beneficial so that the conversion of BPDs to TED is enhanced in a similar fashion as BPD reduction by KOH etching [8]. However, no evidence is yet found to demonstrate that PPDE selectively etches BPDs on the surface and reduces BPDs in epilayer grown on PPDE treated substrate based on our results (Fig. 6). Further study is required to optimize the PPDE process so that it selectively etches BPDs (with minimal TSD etch pits) and enhances BPD conversion for low BPDs in the epilayers.

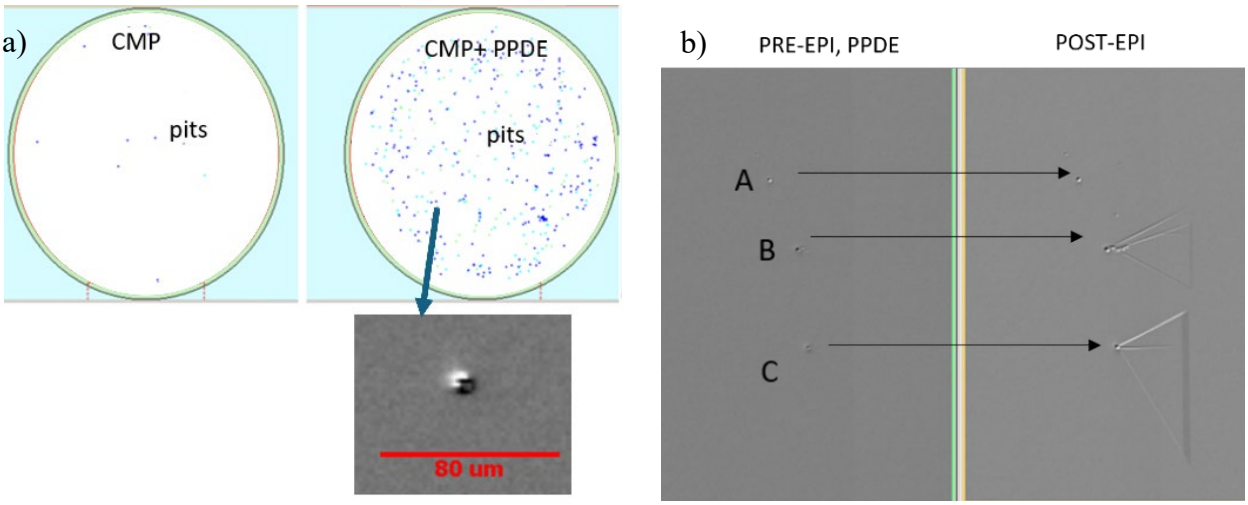

Fig. 4. a) The number of pits increased in the substrates after the plasma treatment. b) The majority of these pits were propagated into epi as pits (A), while a minority of them generated triangular defects and stacking faults (B, C).

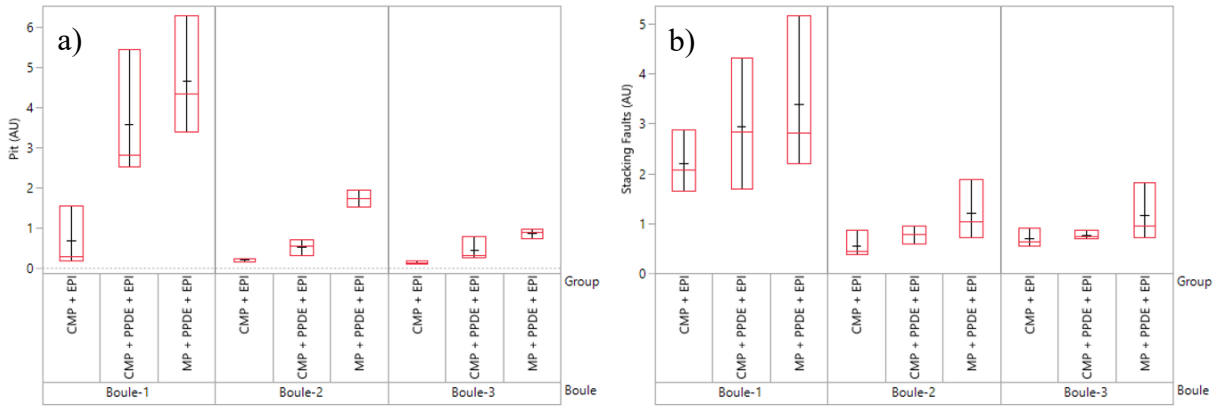

Fig. 5. a) Increase in pits for PPDE treated substrates and b) consequent increase of Stacking faults for PPDE treated surface

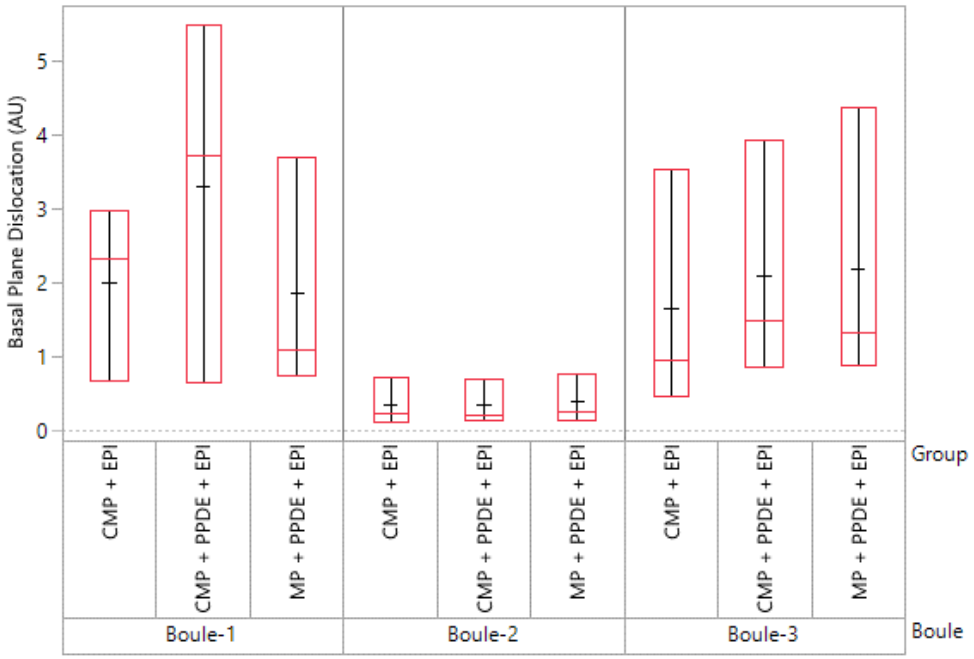

Fig. 6. Basal plane dislocation (BPD) count at different surface conditions is shown. It shows that post PPDE has no clear effect on BPD conversion or reduction.

Conclusion

The effects of plasma polished dry etch (PPDE) on 4H-SiC substrates were studied. We found that surface roughness did not signmificantly worsen for PPDE treated substrate on CMP wafers. PPDE improves surface roughness by smoothing the mechanically polished surface. PPDE selectively etches TSDs in the substrates creating etch pits. These etch pits either propagate into the epilayer as a pit or may work as a source of extended defects (e.g. triangular defects, stacking faults). Our initial goal of the research was to demonstrate that PPDE reduced BPDs by etching BPD sites on the surface similarly as BPD pit creation by KOH etching. However, no clear evidence in BPD reduction was found from our experiments. Since PPDE demonstrates selective etching of TSDs, it has the potential to selectively etch BPD sites as well but further study is required. TSD etch pits need to be minimized by optimizing the process to prevent structural defect formation in the epilayer. These items will be covered in future research.

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