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Thick Semi-Insulating 4H-SiC Layer Exfoliation for Non-Epitaxial Engineered Substrates

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Abstract. The growing demand for 4H-SiC substrates in power device fabrication has encouraged the development of engineered substrates to reduce costs and facilitate wafer re-usability for effective material utilization. This work presents a novel approach for manufacturing SiC power devices is to exfoliate the required drift layer thickness from ultra-high-quality Semi Insulating (SI) 4H-SiC material, bond it to a conductive SiC substrate and thus obtain the non-epitaxial engineered substrate. Energy-filtered Ion Implantation (EFII) technology enables custom doping profiles, precise control of doping concentration, and potentially robust material properties compared to as-grown epitaxial layers in the bonded layer. Key steps to exfoliate a 4µm thick SiC layer from semi-insulating substrates and bond it to low-cost, highly conductive mono-crystalline SiC are demonstrated. This paper mainly focuses on the physical characterization of demonstrated samples.

Introduction

To meet the growing demand for 4H-SiC as a next-generation wide band-gap semiconductor and accelerate power device production, novel substrates are needed to reduce production time and manufacturing costs without compromising device characteristics. Currently, epi-ready substrates [1, 2] rely on traditional epitaxial growth methods to grow the voltage-sustaining layer, a crucial step in the fabrication of power devices [3]. SiC-epitaxy is a complex process and requires regular maintenance to achieve uniform doping profiles and material quality in mass production. An alternate solution is to use the novel non-epitaxial engineered substrates introduced in our previous work [4] to fabricate SiC power devices without the need for epitaxy using on-axis SI 4H-SiC. There are several advantages of having the voltage sustaining layer oriented on-axis, <0001>. 1. Trench MOSFETs do not need the 4° tilted trench etch to maximise the channel mobility on c-plane {0001} [5, 6]. 2. There exist a possible choice of Si-face or C-face for application specific power device. 3. There is also a possibility to achieve Hu profile [7] for achieving minimum ohmic-resistance and highest breakdown voltage. These profiles can be tailor made by utilizing the choice of doping technology described further.

The proposed non-epitaxial engineered substrate could be a promising alternative to current epi-ready substrates if the donor material, doping technology and wafer bonding methods are carefully selected. First, vanadium-free, high-quality semi-insulating (SI) 4H-SiC is chosen as the donor material for the voltage-sustaining layer to avoid unwanted trap levels in the band structure. This material has been used in power devices for JFET operations [8]. Second, Energy Filtered Ion Implantation (EFII) is used to implant box profiles in this layer [9, 10], replacing conventional drift zone doping done via epitaxy. For layer exfoliation of donor wafers, ion slicing with proton implantation [11, 12] is the suitable method among many methods [13–18], as it allows precise control of layer thickness and achieves surface roughness close to a few nanometers after exfoliation. Lastly, wafer bonding needs to provide a seamless bond with minimal electrical resistance, using a

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low-temperature process to preserve the proton concentration for exfoliation. Oxide-free hydrophobic direct bonding [19] with surface activation at room temperature must be chosen over more common hydrophilic bonding [20]. The process flow is illustrated in the Fig. 1

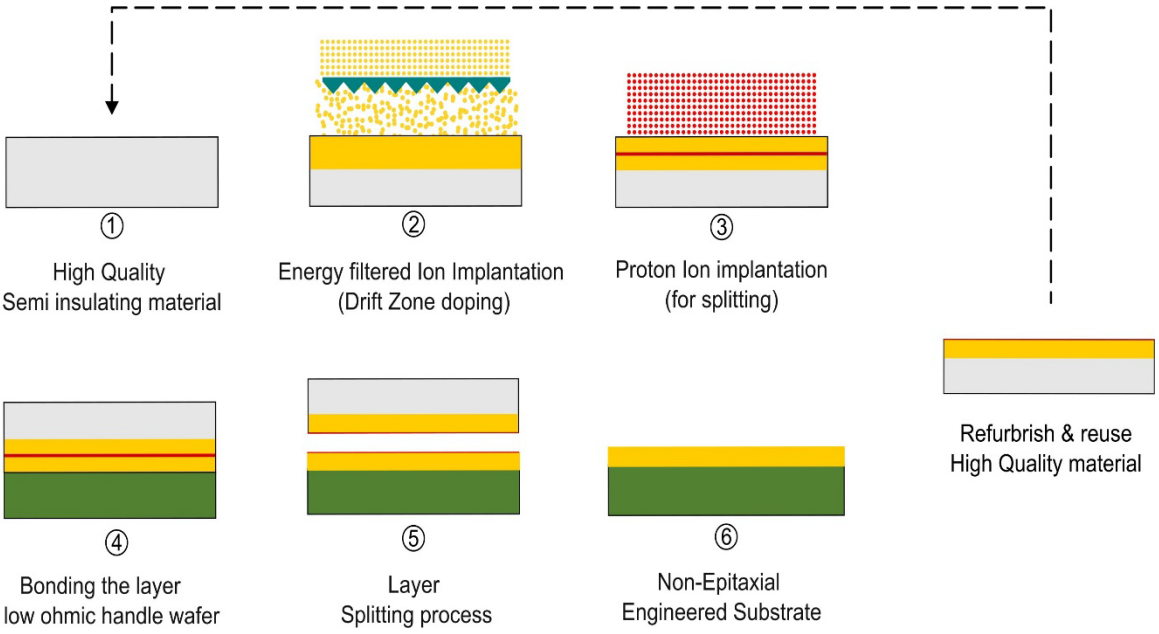

Fig. 1. Illustration of the novel non-epitaxial engineered substrate technology for 4H-SiC power device fabrication. This high quality donor wafer can be used multiple times.

Previous attempts to exfoliate and bond thick SiC layers have failed. This paper details the necessary process steps required to obtain non-epitaxial engineered substrates demonstrated on a chip scale of 20x20mm area. The physical effects of proton implantation on the SiC chips like surface bow, surface roughness, exfoliated layer thickness and bond interface investigations are done. This approach eliminates the need for epitaxy in conventional SiC power device fabrication and is scalable to 200mm SiC technology.

Experimental Approach

Two 6-inch, commercially available on-axis (SI) 4H-SiC wafers were chosen from our previous study [4], these wafers had the lowest density of BPD per volume and the surface roughness of <0.5nm RMS on Si-face was critical for bonding applications. A wafer was implanted with a 5E15cm-3 box profile on the Si-face up to a depth of 8.35µm with Nitrogen using EFII technology and activation annealed at 1700°C for 30 minutes. The implanted wafer served as a doped SI material for the study and the other as an undoped SI material. These samples were prepared to demonstrate that the exfoliation process is suitable for both types of material. Furthermore, wafers were cut into 20x20mm chips to study the critical proton dose requirement and suitable heat treatment parameters to exfoliate the layer from the surface of the chip using ion slicing technique.

For this study, proton energy of 500 KeV was used which has a projected range of 4µm, that implies 4µm thick layers can be exfoliated from the chip. Based on previous work, to exfoliate the thin layer in the SiC [21–26] at lower proton energies, peak concentration was estimated to be in the range of 3E21-6E21 cm-3 for successful layer exfoliation. GEANT4 simulations were performed to obtain the corresponding maximum concentration for proton implants in the range of 1E17-2E17 cm-2 dose as shown in Fig. 2. The chips were then categorized according to material type, labeled and implanted with proton dose as per the Table. 1.

All these chips were implanted with 500 KeV proton with maximum available tilt angle of 7° at the implanter to avoid channelling on the Si-face. After proton implants, one set of chips were subjected to blister tests to find the optimum exfoliation parameters for heat treatment while the other set were chosen for layer transfer with bonding experiments. Tube furnace with Ar ambient was utilized for both blister tests and bonding tests. The heat treatment parameters, including the critical temperature,

Table 1. 500 KeV proton implantation doses and corresponding peak concentrations obtained using GEANT4 simulation in 4H-SiC substrates.

Label	Implanted Dose [cm^{-2}]	Effective Peak Concentration [cm^{-3}]
S	1.00E17	3E21
M	1.35E17	4E21
L	1.68E17	5E21
U	2.00E17	6E21

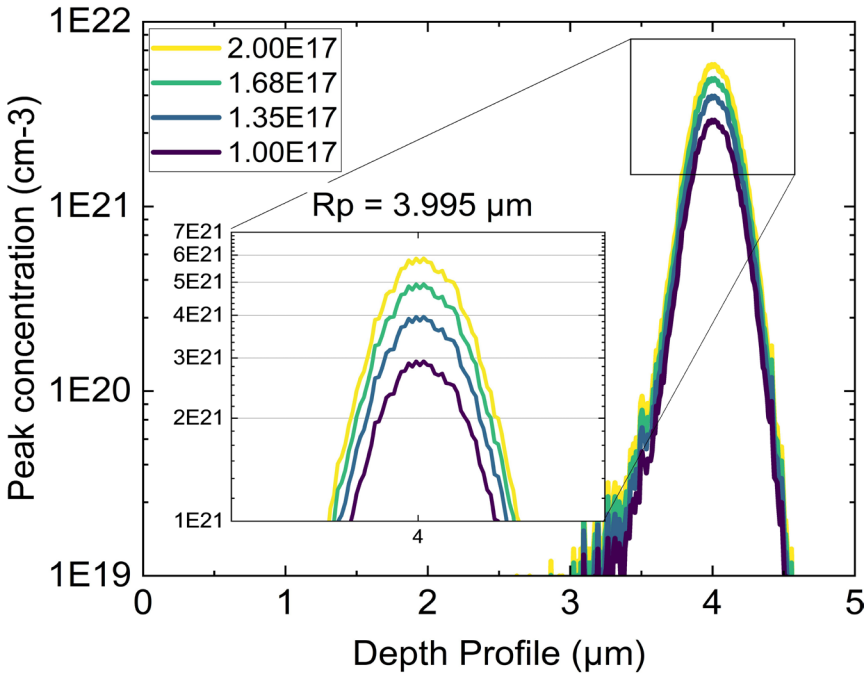

Fig. 2. GEANT4 simulation of ion stopping and range to obtain effective peak concentration for implant doses of proton at 500 KeV energy into 4H-SiC material.

optimal hold times and ramp rate to promote Ostwald ripening process was studied [22]. These tests are critical to find the parameters that promote blister formation, which is crucial for the exfoliation process.

Blister test: Chips selected for blister tests underwent heat treatment at two different hold temperatures at 836°C (T1) and 872°C (T2) with the maximum possible ramp (6°K/min) temperature of the used furnace. T1 was chosen as the minimum activation temperature for blister formation from the arrhenius plot from previous work [25] and higher temperature T2 to enable higher activation rates for blistering. A duration of 30 and 60 minute as hold time at T1 and T2 was tested individually to obtain adequate time for ripening process. The physical aspects of the chip after high proton dose implants were

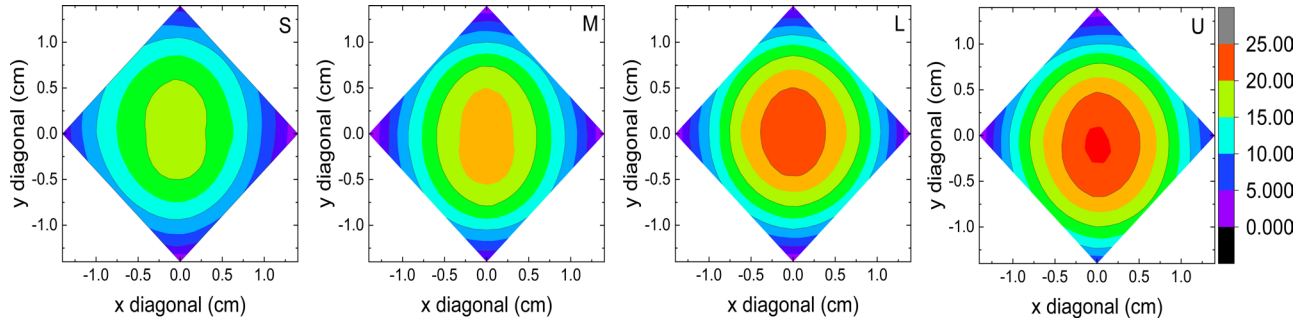

Fig. 3. The physical effect of high dose proton implantation on 20x20mm chips, where bow of 25µm is observed on the highest dose of 2E17 cm-2. Note the measurement points are on the diagonals and the surface is interpolated contour plot from interferrometric measurements.

studied. Convex bow is observed on the implanted chip surface as illustrated in Fig. 3. Similar convex wafer surface can be expected on 6-inch full wafers too with higher magnitude in accordance with previous studies [27]. The blister test results, layer thickness and surface roughness measurement are discussed in the results section.

Bonding experiments: The successful process parameters obtained from the blister tests were used for the bonding experiments. Four bond chip pairs as described in Table. 2 were stuck to a 6-inch Si wafer for handling purpose with kapton tape. The bond equipment MWB-06/08-AX [28] was used for room temperature bonding under ultra high vacuum with in-situ Surface Activation Bonding (SAB) using Ar in Fast Atomic Beam (FAB) gun [29, 30]. An attempt to bond exfoliated SiC to Si chip was also done with Silicon Sputtered Bonding (SSB). Further, bonded layer thickness, surface roughness and cross-section of bond interface with FIB were studied and compared with the blister test results.

Results and Discussion

Blister tests: With regards to the proton dose requirement for both doped and undoped material, a dose of 1.68E17 cm-2 is suitable for exfoliating 4µm thick layers efficiently. Treating the chips at 836°C which is 3°C higher than the minimum theoretical activation temperature [25], can be used to compensate temperature tolerance errors in the furnaces. Blisters were noticeable for 30 minutes hold time. 60 minutes hold time at T1 did not have any notable difference. Temperature T2 or longer hold times could improve bond strength and diffuse residual hydrogen at the bond interface as noted from earlier studies [31]. The N-doped SI SiC layer showed less curling than undoped SI, indicating lower internal stress compared to bulk substrates. This may be due to the 1700°C activation anneal after N implantation with EFII. The test results are summarized in Fig. 4.

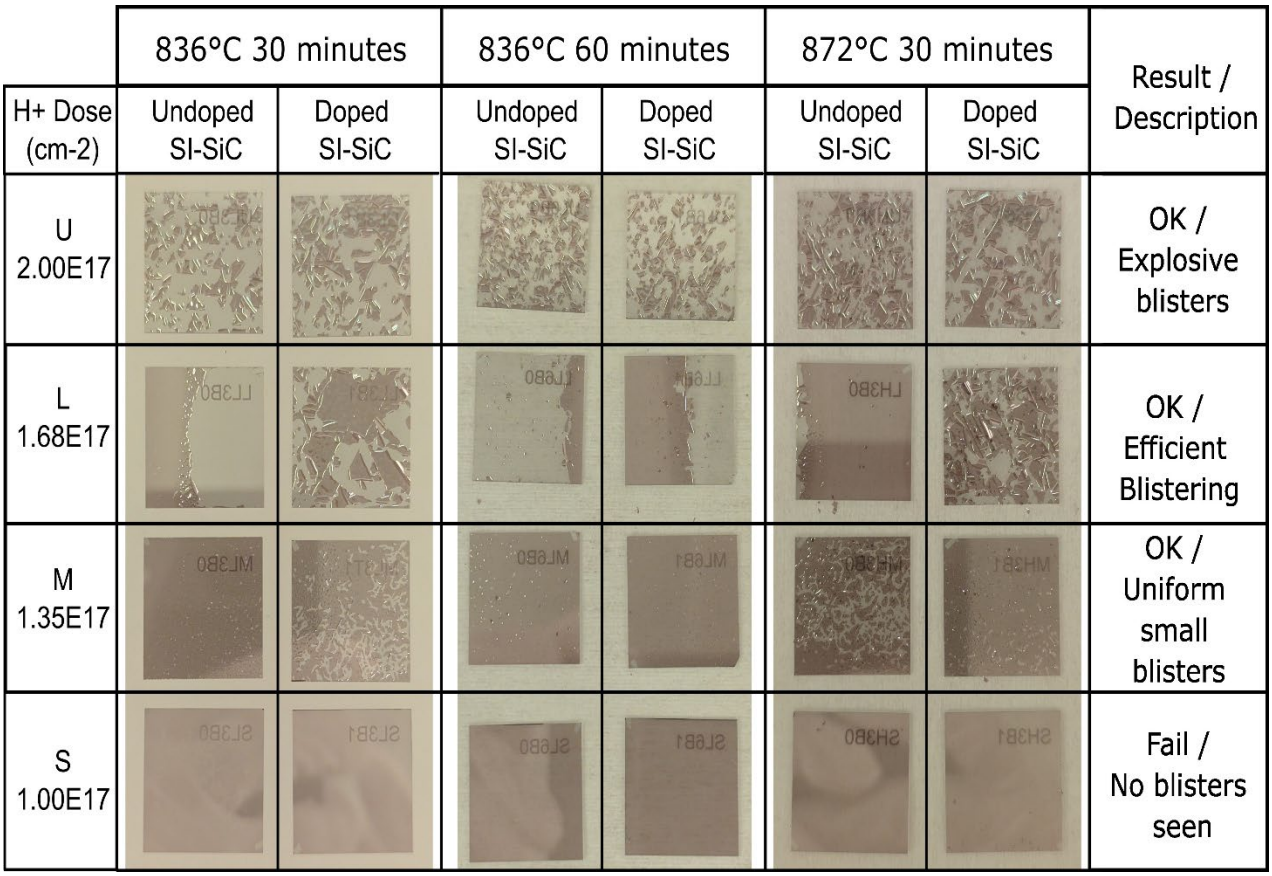

Fig. 4. Results of blister test at different blister parameters like proton dose, heat treatment temperature and ripening time on undoped SI 4H-SiC and doped SI 4H-SiC chips. The minimum dose requirement for a thick 4µm layer blistering is 1.35E17 cm-2. Darker layers are exfoliated SiC and lighter regions are bare substrate underneath.(some dark regions in S row are reflection on the chips)

Fig. 5 shows consistent results for exfoliated SiC layer thickness and surface roughness across multiple samples. However, some samples did not exfoliate uniformly throughout the chip area, likely due to the channeling effect during proton implantation, causing lower peak concentration at the projected range. A 7° tilt is insufficient to avoid channeling in on-axis SiC. An optimal anti-channeling angle for on-axis [0001] in 4H-SiC must be used during proton implantation to ensure uniform exfoliation [32, 33].

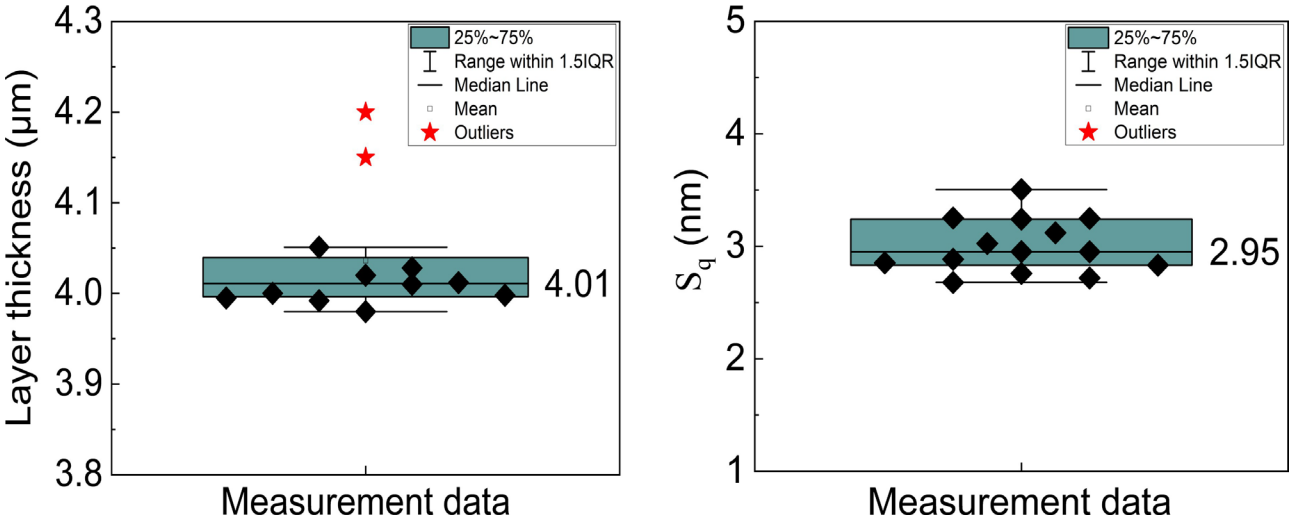

Fig. 5. The blister test measurements promises repeatability of the ion slicing process. *left* shows the median layer thickness of 4.01 µm obtained corresponding to the simulated 4 µm, for 500KeV proton implants in SiC. *right* shows the area surface roughness (Sq) of a 80x80 µm area is also consistent at a median of 2.95 nm.

Table 2. The bond pairs involved, undoped and nitrogen-doped SI 4H-SiC (exfoliation layer) from the donor chips, bonded to N-type SiC and Si as acceptor chip. Bonding results, immediately after bonding and post-exfoliation at 836°C for 60 minutes, are tabulated.

Bond Pair	Donor chip material	Proton dose	Acceptor Chip	FAB type	Pressure welding	Result (as bonded)	Result (after splitting)
1	Undoped SI SiC	M	N-type SiC	SAB	10 MPa	Failed	-NA-
2	Undoped SI SiC	L	N-type SiC	SAB		Success	Success
3	Doped SI SiC	L	N-type SiC	SAB		Success	Success
4	Doped SI SiC	L	N-Type Si	SAB		Success	Failed

Bonding experiments: The bonding experiments results are summarized in the Table. 2 and bond pair 2 image is illustrated in Fig.6a. Due to kapton particle contamination during surface activation step, bond pair 1 failed. Whilst other chips with surface activation bonding were successful. Even the SiC and Si chips were bonded. But during the heating procedure to exfoliate the layers, SiC-Si bond failed due to CTE mismatch. The bond pair 2 and 3 were successful and the exfoliated layer showed robust bond strength even at 872°C for 30 minutes. The layer thickness of 3.92µm was measured with interferrometer as shown in the profile plots of Fig. 6b. The surface roughness (Sq) of the exfoliated surface were measured to be ~3 nm and surface morphology from SEM image is shown in Fig. 6c. Further, plasma assisted polishing [34, 35] provides smooth surface for power device fabrication.

The FIB cross-section measurements on bond pair 3 shown in Fig. 7 also reveals 4µm layer bonded seamlessly to the N-type SiC substrate with interface thickness of <20 nm pre-reactivation anneal. This is a necessary step after bonding to re-activate the dopants after proton implants [36]. The measured value in FIB cross-section Fig. 7b is slightly higher than the interferrometric measurements due to measurement artifact in the tool. These thickness measurements on bonded layers are in accordance with the layer thickness measured after blistering tests. The reduction of 80nm is expected due to the surface cleaning process and the surface activation step before bonding the chips. These results also reveal that the critical peak concentration of hydrogen in 4H-SiC needs to be >3E21 cm-3 for blistering and >4E21 cm-3 for optimum exfoliation of layers. Due to furnace malfunction during 1700°C reactivation annealing, bonded SiC chips were completely oxidized and destroyed. Hence,

bond characterization of the bond interface after high temperature anneal was not performed. Our future work includes scaled up demonstration of this technology on a full 6-inch wafer with further electrical characteristics of the novel non-epitaxial substrates.

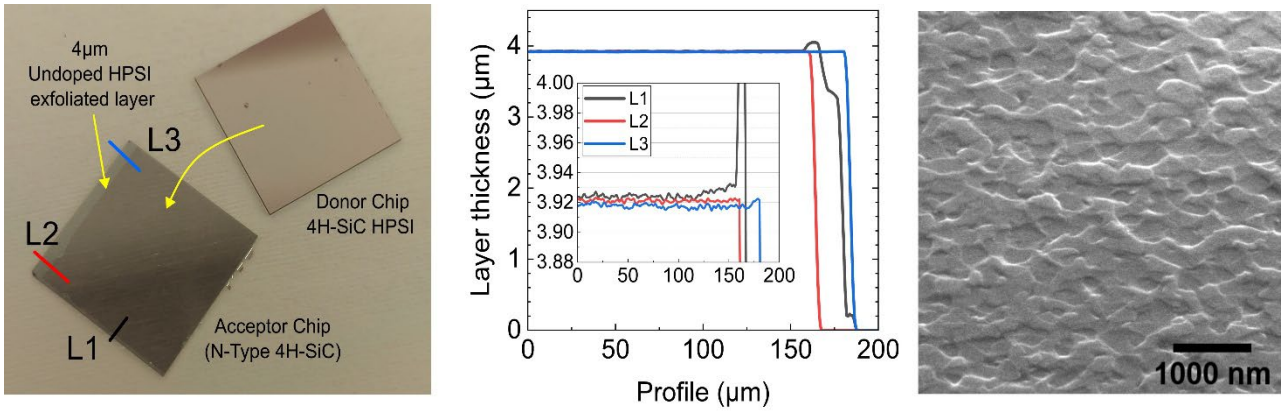

Fig. 6. (a) A 20x20 mm chip was successfully bonded and exfoliated from a donor SI 4H-SiC onto an N-type 4H-SiC substrate. (b) Profile plots of L1, L2, and L3 show a uniform 3.92 µm layer thickness across the chip surface. (c) SEM image of the 5x5 µm exfoliated area reveals a rough surface topology, requiring polishing.

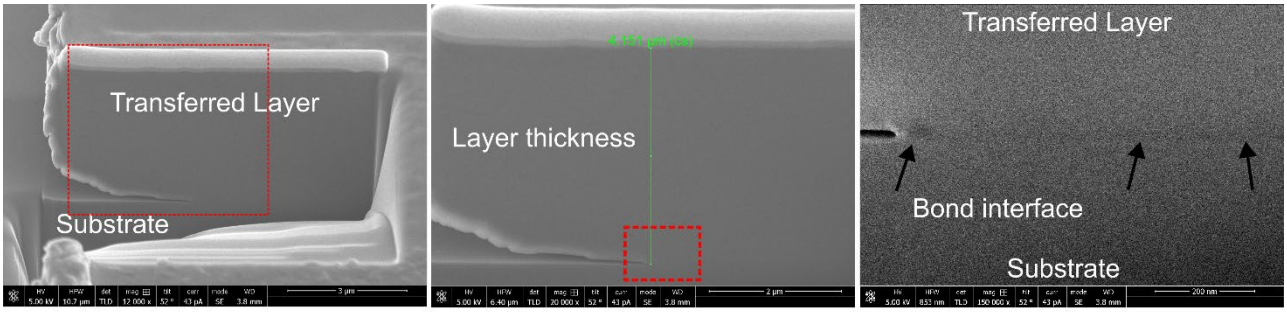

Fig. 7. FIB cross-section images results indicating the seamless bond interface after exfoliating the layer. Regions marked in red are zoomed in successive images. (a) at the edge of the bonded layer. (b) measured layer thickness. (c) Seamless bond interface (enhanced contrast for visibility)

Summary

For the first time, exfoliating a thick 4µm semi insulating 4H-SiC layer and successfully bonding it to a SiC substrate is demonstrated over an area of 20x20mm. This study showcases that for 4µm thick layer exfoliation, peak proton concentration >4E21 cm-3 must be reached at 500 KeV energy followed by the heat treatment greater than 836°C for 30 minutes to sufficiently exfoliate thick layers. Bonding SiC-SiC material is also made possible by using in-situ surface activation bonding at ultra high vacuum under room temperature. However, particle contamination plays an important role in bonding step, hence least particle contamination must be maintained for void free bonding. This technology offers optimal accesibility for exfoliating non-epitaxial layers of thickness upto 15µm for power device fabrication corresponding to the voltage class of 2 KV.

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