Materials Science Forum
ISSN: 1662-9752, Vol. 1156, pp 65-74
doi:10.4028/p-7vQ6Zj
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Submitted: 2024-09-18
Revised: 2025-02-26
Accepted: 2025-02-28
Online: 2025-09-04

SmartSiC™ 150 & 200mm Engineered Substrate: Enabling SiC Power Devices with Improved Performances and Reliability

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Keywords: SiC MOSFETs, specific on resistance, SiC layer transfer, SmartCut™, SmartSiC™, Low resistivity, Bipolar degradation, Power Cycling.

Abstract. The Smart Cut™ technology enables the int egration of high-quality SiC layer transfers, thereby optimizing device yield. It employs low resistivity handle wafers (below 5 mOhm.cm) to minimize conduction and switching losses for both 150mm and 200mm wafers. Material characterization indicates potential R_{DSon} reductions of up to 15% or 30% for advanced 1200V SiC MOSFETs and JFETs. A 24% R_{DSon} improvement for 650V SiC MOSFETs has been demonstrated, with potential reductions of up to 30% for next-generations 1200V SiC MOSFETs. Proton irradiation which is inherent to the Smart Cut™ technology induces an increased ruggedness with regards to bipolar degradation. Additionally, the polycrystalline SiC used as the main material for the die has shown to double power cycling lifetime in silver sintering die attachment An increase of 20K of the maximum junction temperature could be applied without compromising the reliability of the die attach , allowing for a further current increase of up to 10%.

Introduction

Power electronics based on Silicon Carbide (SiC) technology is now considered as a crucial key technology for the electrification of mobility and the efficient use of renewable energies. With the increasing demand of the market, power semiconductor companies are under pressure to rapidly scale up their production capacity. Although there has been notable improvement in the quality and supply of 4H-SiC material, achieving low defect density and reliable wafers for high yields and increased device performances remains a challenge. In response to this, we have introduced a groundbreaking SiC engineered substrate. In this paper, we will demonstrate how SiC engineered substrate is bringing not only performance benefits but also reliability improvements.

Fabrication of SiC Engineered Substrates

The Smart Cut™ technology (see Fig 1) enables the integration of high quality SiC layer transfer for device yield optimization, combined with a low resistivity handle wafer (<5mOhm.cm) to improve device conduction and/or switching losses [1-4] both for 150mm and 200mm wafers diameter (see Fig 2). The SmartSiC™ engineered substrate is composed of a thin (between 350 and 800nm) high-quality 4H-SiC layer bonded (conductive bonding) on top of a 350µm thick polycrystalline SiC handle wafer.

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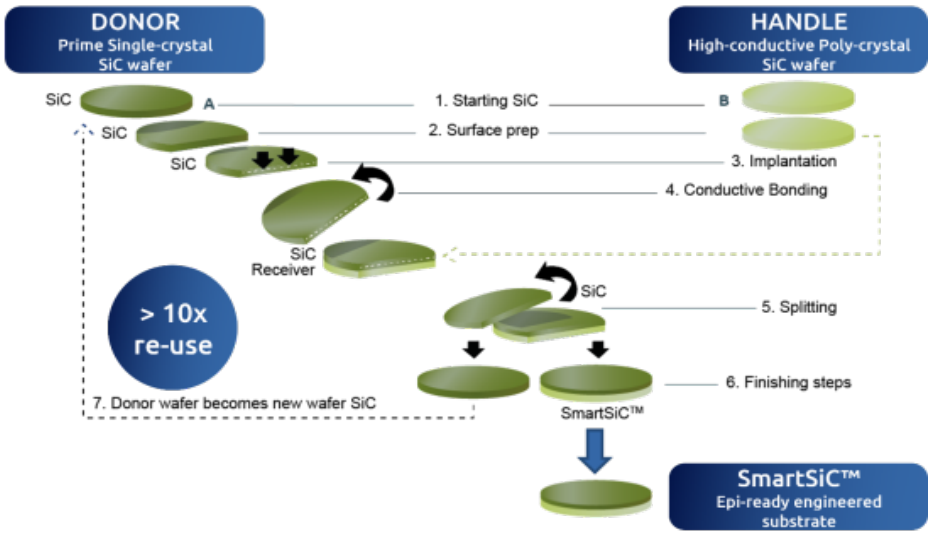

Fig. 1. Smart Cut™ technology adapted to silicon carbide.

Fig. 2. 150mm & 200mm SmartSiC™ substrate ready for SiC drift epitaxy

The initial single crystal donor wafers can be re-used multiple times, leading to efficient usage of the SiC boule materials. Conventional wafering technology can extract a maximum of 50 wafers per boule, whereas our technology enables the preparation of up to 500 wafers out of the same boule. Compared to standard single crystal 4H-SiC material with a conductivity around 20mΩ.cm, resistivities well below 5mΩ.cm are achieved (see Fig. 3) for polycrystalline SiC (pSiC) handle wafer. By means of a high material doping, the electrical resistivity of the pSiC substrate is reduced by a factor of at least 4, up to 10, compared to conventional single crystal SiC (mSiC) wafers. Less than 5 mOhm.cm electrical resistivity is guaranteed, with typical value in the range of 1 to 2 mOhm.cm. Through the application of CVD technology, the performance remains consistent across wafers for substrate diameters of both 150mm and 200mm. This consistency can be replicated using various material sources, a crucial factor for industrial applications, as illustrated in figure 3.

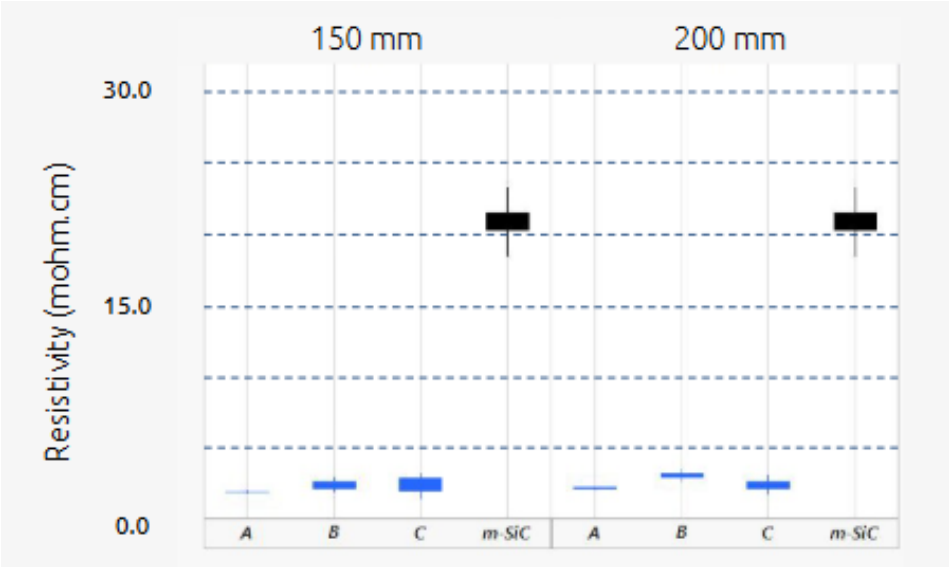

Fig. 3. Electrical resistivity distribution of polycrystalline SiC (pSiC from A, B, C sources) compared to single crystal SiC substrate (mSiC).

Material characterization of SiC engineered substrates for electron transport

Such a high electrical conductivity is confirmed from room temperature (25°C) to maximum device operating temperature (175°C) as stated on Table 1 which compares electrical resistivity on single crystal SiC, pSiC & SiC engineered substrate wafer bonding interface over the whole temperature range [5].

Table 1. Electrical resistivity for each SmartSiC™ layer, from 25°C to 175°C

Temperature	25°C	175°C
4H-SiC bulk [mOhm.cm]	15 – 25	15 – 25
Bonding Interface [mOhm.cm²]	0.003 – 0.006	0.002 – 0.006
Handle pSiC bulk [mOhm.cm]	1.5 – 2.2	1.7 – 2.5

The polycrystalline SiC substrate has a nitrogen dopant concentration higher than the standard level of 4H-SiC. Due to this high N concentration (higher than 10^{20} at/cm^3 [7]), it is thought that, merely by depositing metal, ohmic contact is obtained by means of a tunneling current, since the barrier between the metal and the semiconductor is thin. The contact resistance is hence lowered and we anticipate a level below 10µOhm.cm². Dedicated characterizations are being pursued. As a result, SiC engineered substrates enable a simplified device fabrication process by eliminating the need for ohmic contact annealing, while still maintaining low backside contact resistance**.** Furthermore, as discussed later in this paper, the assembly power cycling (PC_{sec}) reliability [3] remains uncompromised**.**

Device performance results

Given the materials improved properties highlighted in the previous section, we will show in the following section how this enhanced substrate conductivity impacts the SiC power device performances. As a first step we prepared SiC diodes. In a second step we collaborated with ST Microelectronics to evaluate the performance benefit on a large current state of the art SiC MOSFET.

The fabrication of 0.09mm² 1200V JBS diodes and MPS diodes (with areas of 2.5x2.5mm: see figure 4) has been performed in collaboration with Fraunhofer IISB. For 1200V JBS diodes, we have performed wafer level 300x300µm dies forward and reverse characteristics. No critical change in the reverse characteristics was observed [8].

For 1200V MPS diodes, we have reported wafer level dies forward characteristics. Voltage drop lowering at the rated current of 9A for 2.5x2.5mm (see Fig.4) MPS diodes, is around 12%. A first extraction of the dynamic on resistance of the forward regime (2 to 10A) of the MPS diodes leads to a benefit (linked to SiC engineered substrate transition) around 0.9mOhm.cm². This is even beyond the expected gain linked to the improved material resistivity: around 0.77 mOhm.cm². This further gain is supposed to be linked to the lower contact resistance of the back side contact coming from the high level of doping in the pSiC as explained in the previous paragraph.

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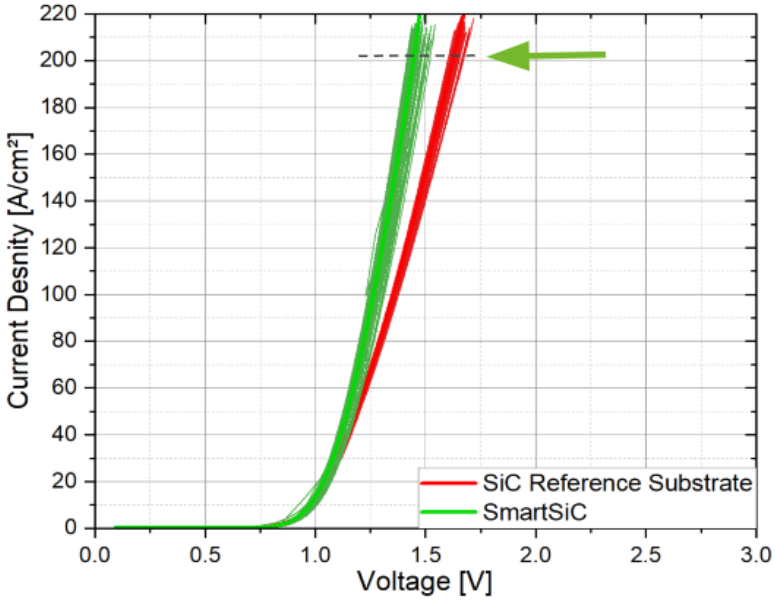

Fig. 4. Forward resistance of Standard SiC and SmartSiC™ for 2.5x2.5mm 10A rated MPS diodes.

In parallel, 650V SiC planar MOSFETs 13mOhm / 650V Gen2 planar SiC MOSFETs were manufactured on both types of substrates (SiC engineered substrates and standard single-crystal 4H-SiC wafers, n-type) and processed simultaneously as a single batch by STMicroelectronics as part of the EU funded program Transform [9]. We have demonstrated a benefit of 24% of R_{DSon} (see Fig. 5). This result was obtained without compromising the leakages (see Fig. 6). Such a strong reduction of R_{DSon} is close to what can be expected during the transition from a given device generation to the next one.

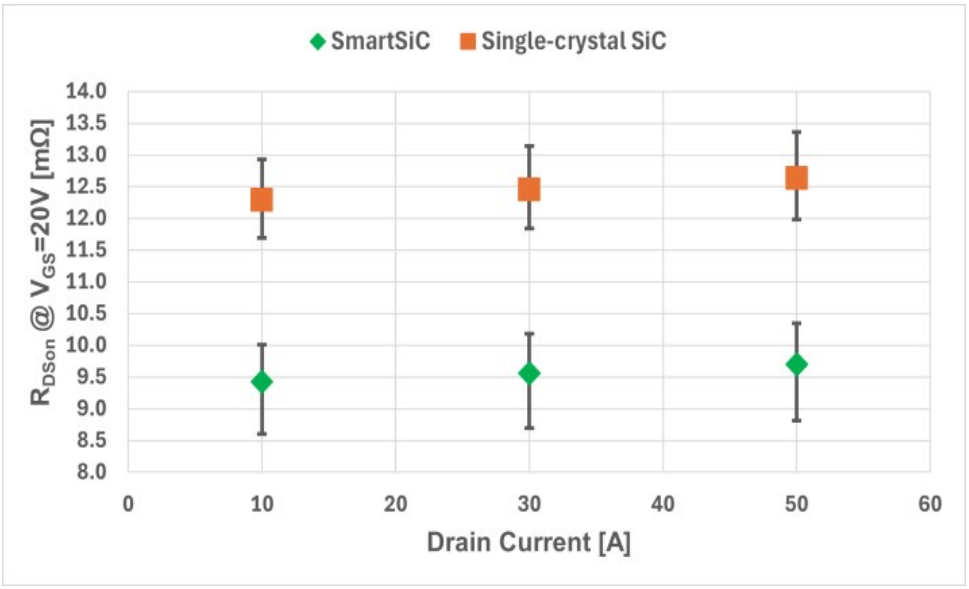

Fig. 5. Ron comparison for a 13mOhm / 650V Gen2 SiC MOSFET manufactured with 4H-SiC and SmartSiC™ [3]

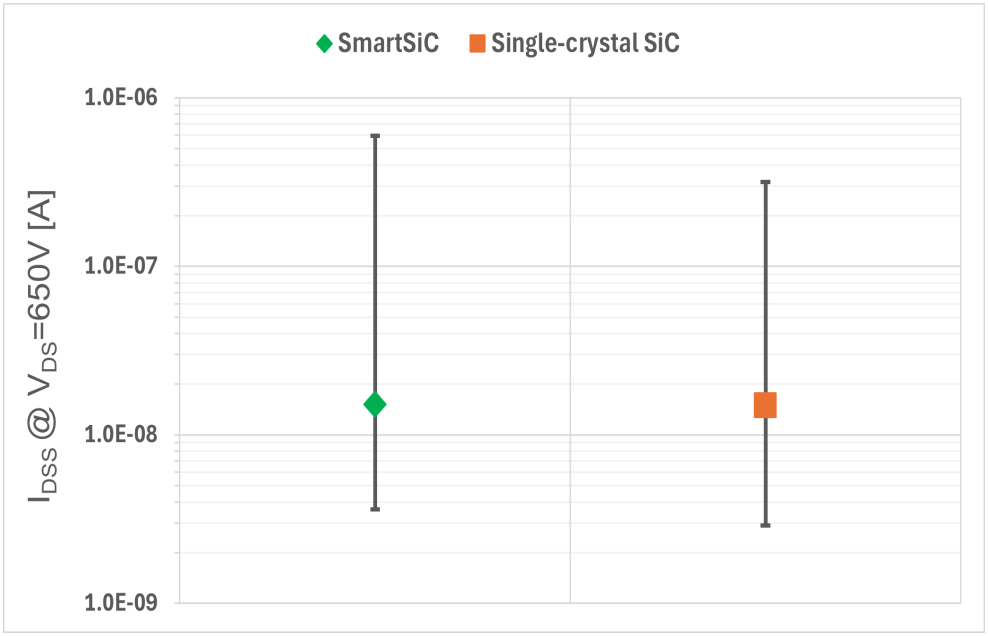

Fig.6. I_{DSS} comparison for a 13mOhm / 650V Gen2 SiC MOSFET manufactured in single-crystal SiC and SmartSiC™ substrates [3].

We recently evidenced that the switching losses of SiC MOSFETs prepared with SiC engineered substrates are drastically improved in terms of Q_{rr} at high temperature (175°C) [10].

Perspectives for SiC MOSFETs Performance

The above presented results are showing evidences that SiC engineered substrate enables an increase of the current density at the device level thanks to both the polycrystalline SiC material's low resistivity and the lowered back side contact resistance. Compared to standard single crystal SiC substrate with a material electrical resistivity around 20mOhm.cm, the polycrystalline SiC material can reach material resistivity as low as 2mOhm.cm. In parallel, thanks to the high doping level of polycrystalline SiC, the contact resistance is lowered around 10-50 µOhm.cm². Let's see now how this will impact the upcoming SiC power devices developments.

SiC MOSFET R_{DSon}. A specific resistance has been improved by all device suppliers through specific engineering of the active layers (channel, contacts, cell pitch,...) and advanced thinning of the substrate down to 100µm. While there is still room for improvement for the active layers (reduced pitch through super junction design, dense cell pitch through trench design,...), the mechanical thinning of the SiC substrate will soon reach its limit especially in the context of the transition to 200mm diameter SiC semiconductor substrates. This will increase drastically the contribution of the substrate to the device specific resistance (see Fig.7). As device R_{DSon}.A specific resistance is lowered the relative contribution of the 4H-SiC substrate (considering a 100µm thickness) is drastically increasing.

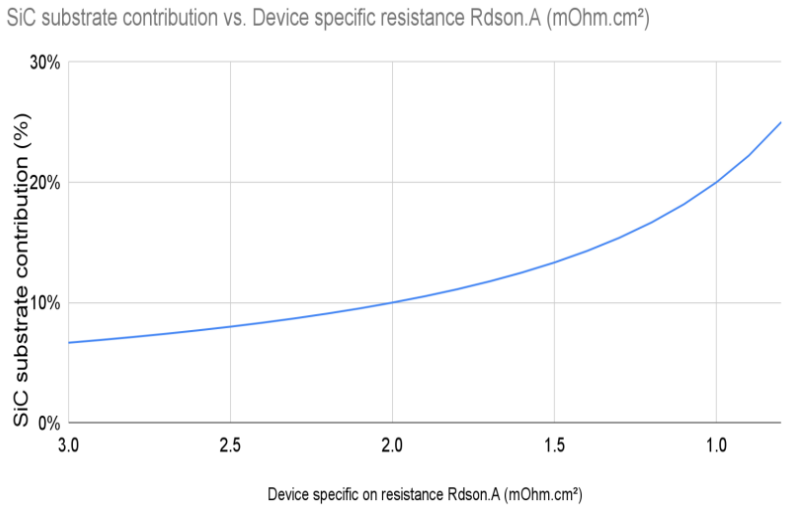

Fig. 7. SiC substrate contribution to MOSFETs specific on resistance.

Now switching to SiC engineered substrate, the benefit on the electrical parameters as compared to 4H-SiC standard material can be calculated as a function of device specific resistance (R_{DSon}.A) at room temperature and die thickness. We clearly see that for R_{DSon}.A improvement up to 15% for state of the art 1200V SiC MOSFETs and up to 18% for next generation 1200V SiC MOSFETs, can be envisioned (see Fig.8). Considering ultimate SiC MOSFET or state of the art JFET, improvement up to 30% is anticipated.

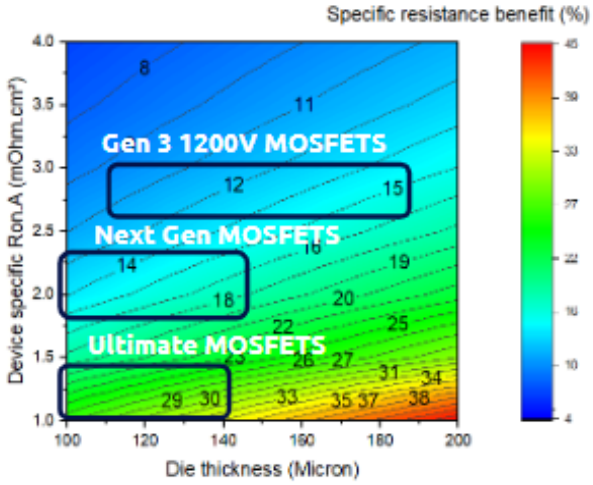

Fig. 8. R_{DSon}.A benefit enabled by SmartSiC™ integration for 1200V SiC MOSFET.

SiC power device ruggedness; bipolar degradation benefits of SiC engineered substrate

Beyond the performance improvements discussed in the previous section, the SiC engineered substrate also helps tackle one of the key challenges in SiC power devices: bipolar degradation**.**
Basal plane dislocations (BPDs) in 4H-SiC substrates have emerged as crucial defects in SiC wafers during the past decades. Bipolar degradation in 4H-SiC PN diodes and SiC MOSFETs (through the bipolar body diode) has become a significant concern affecting device ruggedness. This phenomenon occurs when BPDs are transformed into single Shockley stacking faults (1SSFs) which expand, leading to an increased device R_{DSon}. Two major strategies have been developed to address this issue: first reduce BPD density and minority carrier lifetime through the design of a proper SiC buffer layer, second use an external Schottky diode which can be monolithically integrated [11].

As a first assessment of SiC engineered substrates we have decided to use a newly developed E-V-C technique developed by ITES, Co. (Japan) that enables us to stress the material (through UV illumination) without processing and characterizing a real device.
Bipolar degradation of post epitaxy SiC substrates without diode processing was carried out on reference and engineered SiC substrates. This involves initiating bipolar degradation driven by SSF through UV illumination, followed by a focused examination of photoluminescence using a selective band-pass filter (BPF) at approximately 420 nm [12, 13]. Different UV intensities with a wavelength of 355 nm were used (38, 75 and 150W/cm²).
As the UV illumination power increases, SSFs develop faster in the case of single crystal SiC compared to SiC engineered substrates (ratio of linear regression of SSF area over illumination between the 2 wafer designs) [14]. Fig. 9 provides a comparison of observation fields using the 420nm band-pass filter (BPF).

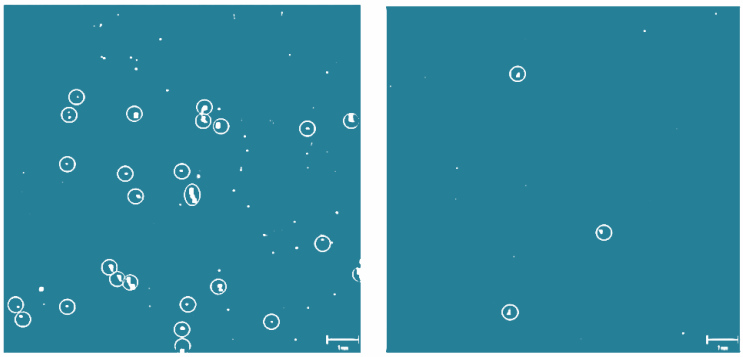

Fig.9. Typical 10x10mm observation fields post UV illumination of bipolar degradation severity between single crystal SiC +10µm epi (left) vs. SiC engineered substrate +epi (right)

We have demonstrated that both the number of Shockley stacking faults (SSF), the indicator that bipolar degradation takes place, and their typical size are lower in the case of SiC engineered substrate prepared through Smart Cut™, compared to the results obtained in standard SiC wafers (see fig.5). In parallel, Kato et al. [15] have demonstrated that the movement of partial dislocations can be suppressed by proton implantation. Proton implantation is inherent to the Smart Cut™ technology. Device assessment is now under evaluation on our side, and electrical stress tests are being carried out.

Power module reliability of SiC engineered substrate based dies

Now looking at the power module integration, the thermo mechanical properties of this new material are driving the reliability of the complete stack. With SiC engineered substrate, we introduce a new semiconductor design embedding a bonded interface and a new material structure for the backside (non annealed back side ohmic contact). Main focus of this study was to assess the compatibility of this new semiconductor substrate with reliability standards, especially at the power module level. When looking at AQG324 [15] (qualification of power electronics modules for use in motor vehicle components) for power module qualification, we focused on the power cycle test (PCT) which assesses the reliability of both front and back side die assembly and connections, and assess any potential weakness at the bonded interface (see Fig.10). By limiting the t_{on} (on-time of the load current) to a value of $t_{on} < 5s$, the test exerts targeted stress on the chip – near interconnections (die-attach and top side) and any other structure within the chip itself – thus studying the potential impact of SiC engineer substrate materials properties in a conventional module setup.

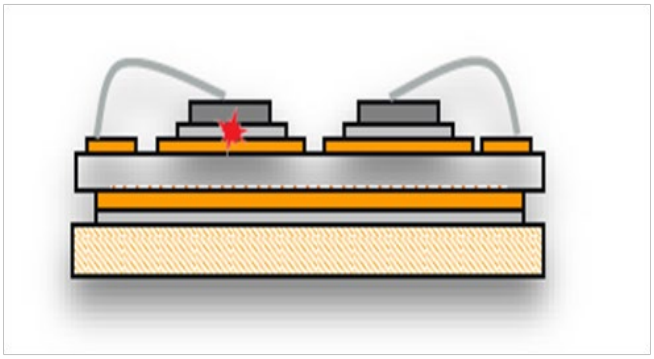

Fig. 10. Schematics of conventional setup of power modules used for the AQG324 PC_{sec} test [15] and the expected location of failures close to the chip marked red (from ECPE training by A. Schletz)

We designed a specific test vehicle [2] with a Schottky contact built on the top side of the substrate. Current is injected in the devices under test (DUT) through this Schottky contact. A conventional Ti/Ni/Ti/Ag metallization stack on the backside has been prepared after thinning down to 250µm and NiAl ohmic contact formation annealed by laser. These Schottky contacts act as semiconductor junctions used for heating and temperature sensing within the power cycling test. Substrates were diced into individual chips of 5mm x 10mm. DUTs are mounted onto conventional DCB-substrates by silver-sintering with jetted sinter-paste. The top-side contact is connected through Al bond wires (see Fig.11).
The active power cycling tests were performed to compare the lifetime of the SiC engineered substrate compared to standard SiC reference using a well-validated setup [16]. The DUTs were mounted to a water-cooled Aluminum heatsink with coolant temperature of 40°C. The backsides (opposite to the sintered chip) of each individual DCB-substrate were direct-cooled by water-glycol coolant. Calibration of a typical device voltage drop at a given low current (30mA, to avoid self heating) at various temperatures allows for direct measurement of junction temperature of the device under test.

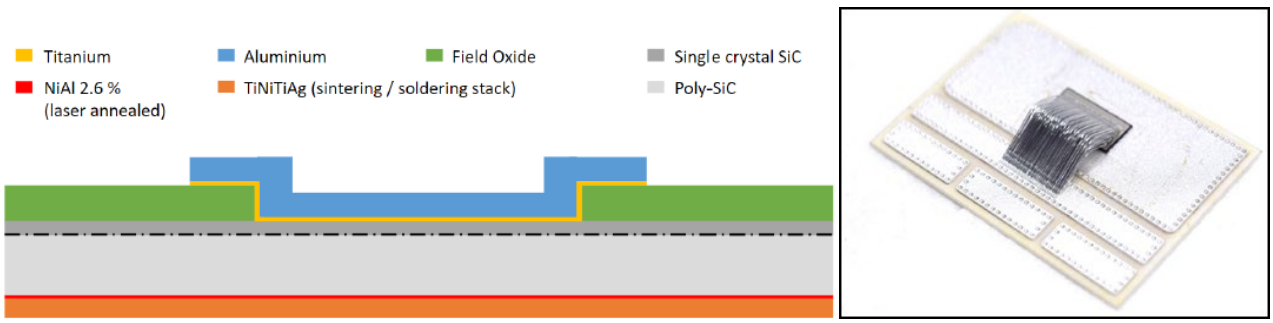

Fig. 11. (Left) Schematics of Schottky-Contact on SiC devices used for reliability testing, (Right) Silver-sintered sample on DCB with silver surface with top-side contact by 125um Aluminum bond wires

The active power cycling tests were performed to compare the lifetime of the SiC engineered substrate compared to standard SiC reference using a well-validated setup. The Power Cycling (PC) test is designed to characterize the lifetime of the semiconductor itself using short cycles (PC_{sec}) with 3 seconds heating (t_{on}) and 6 seconds cooling (t_{off}) with a temperature swing ΔT targeting 120 K and 80K.

PC_{sec} has been validated up to 350k cycles and 1600k cycles respectively for 120K and 80K of temperature swing, at least for 29 samples prepared from 2 different SiC engineered substrates with silver sintering assembly. On the other side standard SiC samples had reduced lifetime.

A uniform Delta T set point was guaranteed through the adaptation of the current load to the dynamic resistance of the DUTs (reference SiC or SiC engineered substrate): 10% higher current load for DUTs prepared with SmartSiC™.
The lifetime data (see Fig.12) exhibit an exponential term as expected from the CIPS 2008 [17] as a major driving term. Looking the other way around, it means that for a given use case having its targeted lifetime, temperature swing could be increased, meaning a higher dissipated power and then an increased current. As shown on figure 12, an increase of 20K of the maximum junction temperature could be applied without compromising the reliability of the silver sintering die attachment.

$$P_{max} = R_{on}.I^2_{max} = (T_{j,max} - T_{case})/R_{TH} \quad \text{(Eq.1)}$$

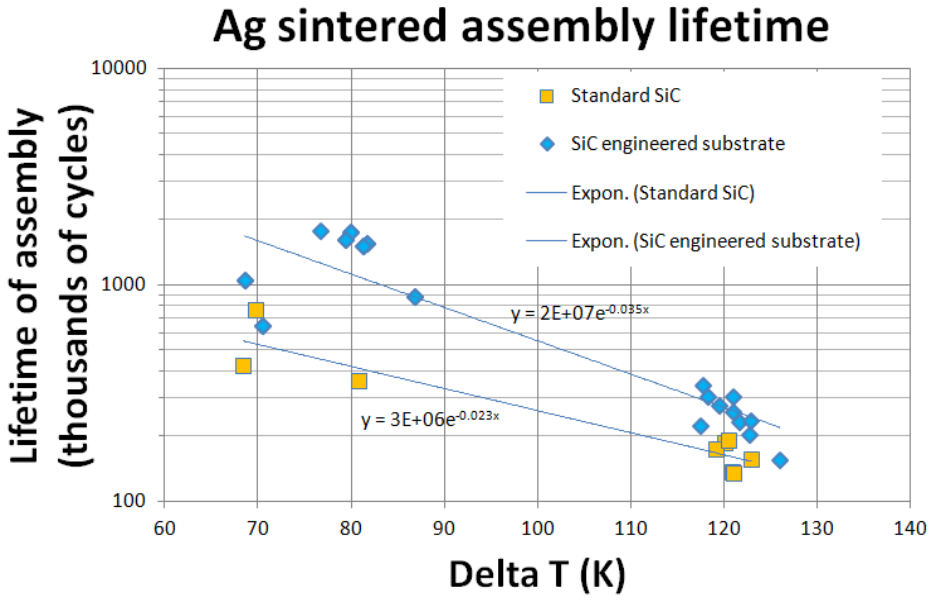

Fig. 12. Comparison of SiC standard and engineered substrates lifetime assembly for both silver sintering.

Polycrystalline SiC used as a receiver for SiC engineered substrates is driving the thermo mechanical properties of the final SiC MOSFET die and will play a crucial role on the die assembly reliability. Our main hypothesis is that elastics and/or thermoplastics properties of the polycrystalline SiC material are modifying the lifetime model (modification of the Young modulus and/or Morrow model parameters [18]). An alternative hypothesis is that either the grain size and orientation distribution of the polycrystalline SiC is modified [19] close to the interface, or polycrystalline SiC is experiencing subcritical crack growth [20]. Both mechanisms could improve lifetime. Coefficient of thermal expansion (CTE), flexural strength and Young's modulus of polycrystalline SiC material are currently performed and modeling is being performed.

Conclusion

SmartSiC™ engineered substrates demonstrate a significant enhancement of performance and reliability. The low resistivity polycrystalline SiC (as low as 2 mΩ·cm vs. 20 mΩ·cm for 4H-SiC) enables higher current densities with a demonstrated improvement of SiC MOSFETs specific on resistance by more than 20%. Proton implantation, intrinsic to the Smart Cut™ process, effectively suppresses Shockley stacking fault (SSF) expansion. Wafer reusability further enhances sustainability. SmartSiC™ is paving the way for next-generation SiC devices with superior efficiency and reliability.

Acknowledgements.

This work is supported by the H2020 - ECSEL JU programme of the European Union under the grant of the TRANSFORM project 'Trusted European SiC Value Chain for a greener Economy' (ECSEL JU Grant No. 101007237).

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