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# Development of a Novel Warpage Control Method for Epi-Ready 4H-SiC Wafers by Depositing Homoepitaxial Layers on both Si- and C-Faces

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**Keywords:** Sublimation etching, Epitaxial growth, Dynamic AGE-ing®, Sub-surface damage, Thermal stress, Bow

**Abstract.** We have demonstrated a novel process that precisely controls the wafer bow, a key parameter of overall warpage, of 4H-SiC wafers to any desired value by integrating a thermal sublimation process, Dynamic AGE-ing® (DA), immediately prior to the CVD epitaxial process. This method achieves atomic-level flatness of the CMP-finished surface independent of the growth and etching amounts, while concurrently eliminating sub-surface damage (SSD). When DA is applied to simultaneously etch the Si-face and grow the C-face, the wafer bow decreases linearly with increasing C-face growth. In wafers with poorer mechanical processing quality, an increase in bow is observed for C-face growth below 120 nm, likely due to the relaxation of SSD on that side. The process also removes SSD from the Si-face, ensuring that both sides are sufficiently cleared of damage. Furthermore, for wafers with an initially negative bow, simultaneous Si-face growth and C-face etching using DA produces a linear increase in bow. By applying these processes, we successfully adjusted the bow to –0.4 μm on an 8-inch wafer that initially measured –12.0 μm. These results indicate that, regardless of the initial bow severity, precise control of the wafer bow can be achieved without adversely affecting subsequent CVD epitaxy processes by appropriately managing the growth layer thicknesses on both faces using DA.

## Introduction

In device manufacturing, active control of wafer bow, curvature component of the wafer warpage, is essential for improving yield. This is because the significant Bow hinders uniform resist deposition in the lithography process and causes vacuum chuck failure in the device fabrication process. [1].

Wafer bow arises when the stress states on the front and back surfaces differ. Such stress differences originate from residual effects introduced during ingot growth, the Twyman effect resulting from variations in mechanical processing quality, and uneven film deposition (Fig. 1) [2]. Residual stress in ingots is generated by thermal gradients, cooling rates, and impurity distributions during growth [3]. For example, if the C-face experiences higher temperatures during the ingot growth, defect formation to relieve thermal stress can lead to tensile stress and a positive bow bias.

If the backside surface of the wafer has a rougher processing state than the frontside, the wafer shape will have a concave shape due to the strong compressive stress originate from sub-surface damage (SSD). This effect is referred to as the Twyman effect [2, 4]. During the device fabrication process of the wafers, epitaxial growth is performed on the Si-face, and it is essential to sufficiently remove sub-surface damage (SSD) introduced by machining to prevent defects. Therefore, the mechanical processing accuracy of the Si-face tends to be emphasized more than that of the C-face.

It is important to note that the bow of "bare" wafers is determined by both internal stress and the polishing state. This variability may differ not only between manufacturers but even from wafer to wafer, complicating bow control. Furthermore, especially with the push toward large diameter such as 8-inch processing, can further increase the challenge of maintaining uniform bow.

Deposition of thin films also influences wafer bow through intrinsic film stress. According to Stoney's formula, the bow depends on both the substrate and the epitaxial growth layer thicknesses [5]. For instance, growing a lower N-doped homoepitaxial layer can induce tensile stress, increasing the bow to form a convex shape [6]. High-temperature processes like CVD epitaxy and post-implant annealing disturb the stress balance on the wafer surfaces. Because mechanical strain is concentrated at the surface, even incremental etching (on the order of less than 100 nm, the limit of $H_2$ etching) can significantly alter the strain distribution and thus the bow.

Our innovative method actively controls wafer bow by relieving stress on both surfaces simultaneously. We have developed Dynamic AGE-ing® (DA), a thermal sublimation etching and epitaxial growth technique that anneals SiC wafers in a quasi-closed space, enabling simultaneous etching on one side and growth on the other (Fig. 2). A key feature of DA is that it allows independent control of surface roughness regardless of the etching depth of over 10 µm [7]. By removing strain from the Si-face via etching and relaxing strain on the C-face through homoepitaxial growth, SSD could be relieved, thereby minimizing its effect on wafer bow. Consequently, by optimizing the thicknesses of the epitaxial layers on both sides, the wafer bow can be tuned to any desired value (Fig. 3).

To quantitatively assess mechanical processing quality, we have also developed a laser light scattering (LLS) method [8]. By irradiating the wafer at oblique angles, the LLS intensity distribution correlates with the depth of sub-surface damage (SSD) and the processing quality, enabling a comprehensive evaluation of the balance in mechanical processing across different vendors.

In this study, we demonstrate stress relaxation on both wafer surfaces using the DA process and focus on controlling the wafer bow. We further correlate the mechanical processing quality evaluated via LLS on both the Si-face and C-face with the resulting wafer bow.

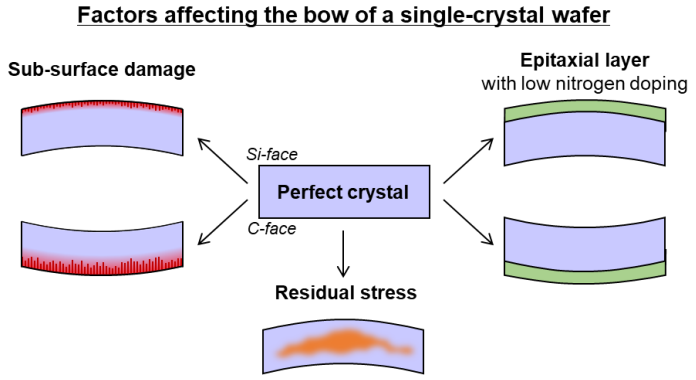


**Fig. 1.** Factors causing stress and warpage in single-crystal wafer.

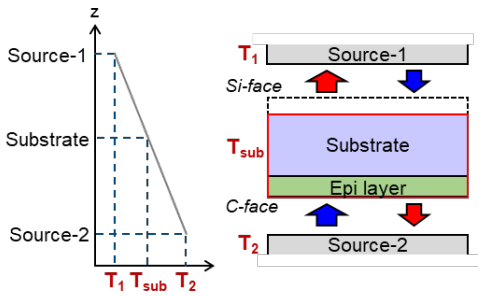


**Fig. 2.** Schematic of simultaneous control of both sides of a SiC wafer using the Dynamic AGE-ing® (DA).

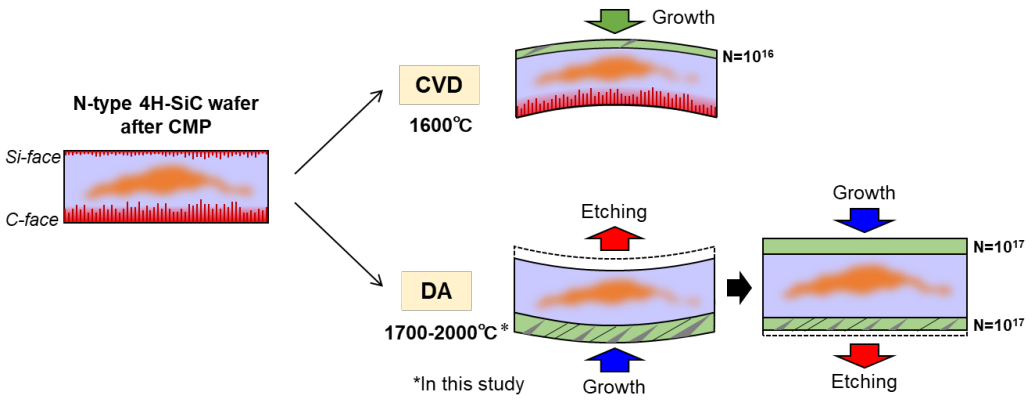


**Fig. 3.** Differences between CVD epitaxy and DA process and their impact on wafer bow.

## Experiments

The samples were 4° off-cut towards [11-20] direction and epi-ready polished on the (0001) Si-face wafers purchased from several vendors. The wafer sizes were 6- and 8-inch, and the details of sample information used for the DA process are summarized in Table 1.

The samples were measured for LLS intensity. The incident laser was *s*-polarized to the wafer and wavelength of 355 nm. The obtained LLS intensity values were calibrated by the amplification factor. The same samples were also measured by laser interferometry using the NIDEK Slanting Incidence Interference Method Flatness Tester. This equipment measures the sample in a vertical position. The mode values of the LLS intensities for the Si- and C-faces were then determined. Photoluminescence imaging (PLI-200) was also used to observe defects across the entire surface.

DA process was used for sublimation etching and sublimation epitaxial growth. The DA etching was performed on the Si-face at a temperature of 1700 - 1950 °C for 10 - 120 minutes, with an etching depth of approximately 80 nm to 16 μm set for the Si-face. During the etching of the surface, an epitaxial growth layer was simultaneously grown on the back surface. Sublimation epitaxial growth was then used to attach an epitaxial growth layer (carrier concentration: 1.0 to 3.0 × $10^{17}$ $cm^{-3}$) of about 3 μm to 20 μm to the Si-face. After each experiment, the bow of the wafer was measured.

**Table 1.** Details of sample information used in the DA process.

| | Wafer Ⅰ | Wafer Ⅱ | Wafer Ⅲ | Wafer Ⅳ | Wafer Ⅴ | Wafer Ⅵ |
|---|---|---|---|---|---|---|
| **Vendor** | A | D | A | A | B | D |
| **Grade** | Production | Production | Research | Research | Production | Research |
| **Diameter** [mm] | 150.1 | 150.0±0.2 | 150.1 | 150.1 | 149.9 | 200.0±0.2 |
| **Thickness** [μm] | 370 | 367 | 375 | 365 | 348 | 497 |
| **Resitivity** [Ω·cm] | $1.7\times10^{-2}$ | $1.9\times10^{-2}$ | $1.7\times10^{-2}$ | $1.7\times10^{-2}$ | $1.7\times10^{-2}$ | $2.0\times10^{-2}$ |
| ***C-face* LLS intensity** [mV] | $3.5\times10^{-1}$ | $2.3\times10^{-1}$ | $1.0\times10^{1}$ | $8.4\times10^{0}$ | $7.3\times10^{1}$ | N/A |
| ***Si-face* LLS intensity** [mV] | $2.1\times10^{-2}$ | $2.2\times10^{-4}$ | $1.4\times10^{-2}$ | $2.0\times10^{-2}$ | $1.2\times10^{-2}$ | $1.7\times10^{-2}$ |

## Results and Discussions

To investigate vendor strategies for controlling wafer warpage, the process quality balance of both sides of a 6-inch wafer from each vendor was quantified and related to the bow. Fig. 4 shows a graph relating the bow to the mode value of the LLS intensity for both Si- and C-faces of wafers from several vendors; colors represent vendors, with circles and crosses for Si- and C-face, respectively.

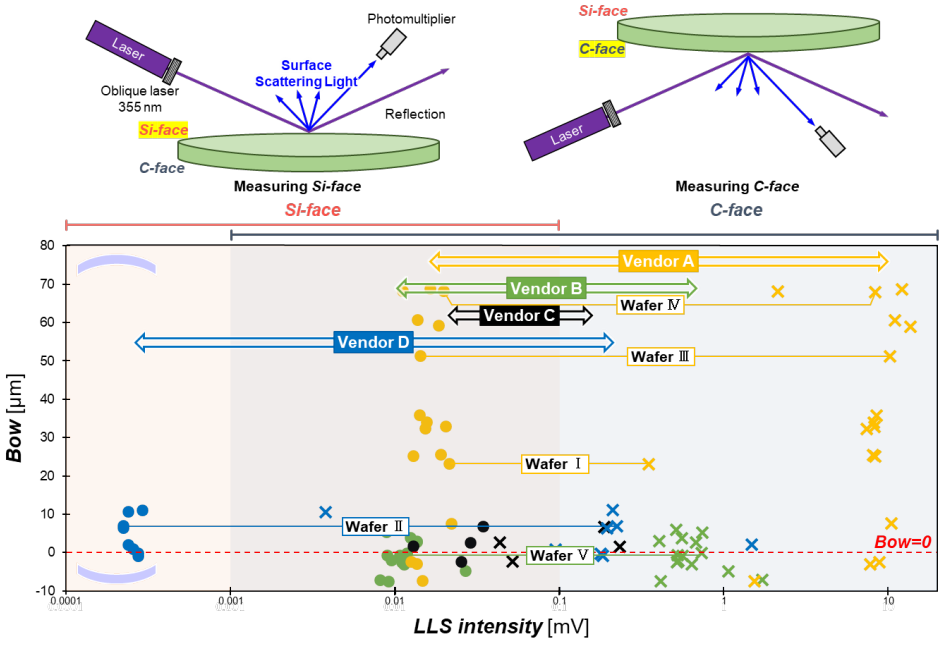


**Fig. 4.** Laser light scattering (LLS) intensity mode value - bow value graph for the Si-face and C-face of 43 φ6-inch 4H-SiC wafers from vendors A to D.

For the 6-inch wafers used in the DA process, the values for the Si- and C-faces are connected by lines. From the graph, it can be observed that wafers from the same vendor have similar scattering intensities on both the Si- and C-faces. It also shows that the bow is biased in the positive direction, which is due to residual stresses introduced during bulk growth. The SSD and rough surface on the C-face tend to reduce the bow, while the residual stress within the wafer increases it. In other words, wafers with an initially high positive bow caused by residual stress are controlled by adjusting the mechanical processing quality of the C-face. This suggests that, different vendors have different strategies for controlling wafer warpage and may utilize the Twyman effect.

Fig. 5 shows the evolution of wafer bow for two wafers processed by DA-growth on the C-face and DA-etching on the Si-face over 2–2.5 hours. Both Wafer I and Wafer II exhibit a linear bow change with increasing epitaxial thickness as predicted by Stoney's formula—except for the initial DA process on Wafer I. In that first process, Wafer I shows a non-linear bow change when DA-growth and DA-etching are applied simultaneously. Since the SSD on the Si-face is negligible (LLS intensity ~0.021 mV), this non-linearity is attributed to defect formation at the C-face interface due to high SSD. Photoluminescence images support this, revealing an epitaxial defect density of 54/cm² on Wafer I versus 0/cm² on Wafer II. These results suggest that early defect formation relieves stress from C-face SSD and that DA epitaxial growth both mitigates SSD and calibrates stress variations from doping differences. Additionally, the reversal of bow from positive to negative in Wafer II indicates that the initial bow can be adjusted to specifications, potentially reducing yield losses. In a related experiment with Wafer III, where 80 nm of the Si-face was etched and 120 nm of the C-face grown, the bow peaked at 120 nm before decreasing linearly, further confirming that changes in SSD distribution during thermal processing drive bow behavior via early defect formation.

If the cause of the exceptional bow changes observed at the beginning of DA-growth on the C-face of wafer I is defect formation at the interface between the substrate and the epitaxial growth layer, it should impact the initial stage of epitaxial growth on the C-face. To investigate the effect of SSD concentrated on the surfaces of both sides of the wafer on the bow during thermal sublimation etching and epitaxial growth, the DA process was used to simultaneously etch the Si-face by 80 nm and grow the epitaxial layer on the C-face by 120 nm. The results of the bow changes are shown in Fig. 5. Wafer III. The bow value reached a maximum at 120 nm of epitaxial growth on the C-face and then decreased linearly. This result indicates that the bow is significantly affected by changes in the SSD distribution on both sides of the wafer during the thermal sublimation etching of the Si-face and the epitaxial growth on the C-face. This suggests that the stress caused by the SSD on the C-face is released through defect formation, which occurs at the very beginning when the interface with the growth layer is formed.

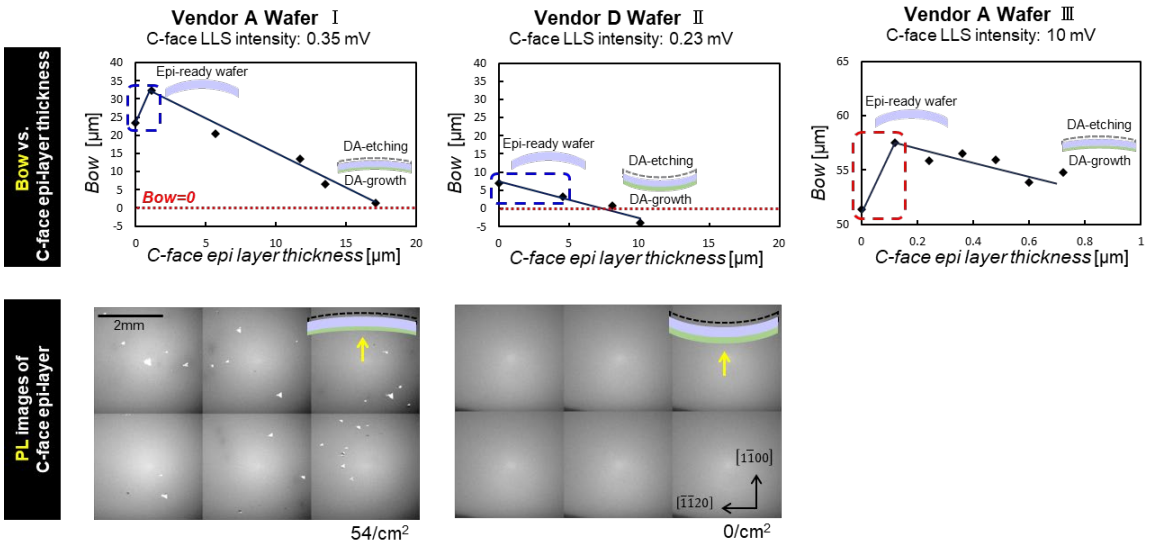


**Fig. 5**. Measurement results of the bow values during the DA process for wafers I - III. PL images of the epi-layer formed on the C-face of wafer I and II.

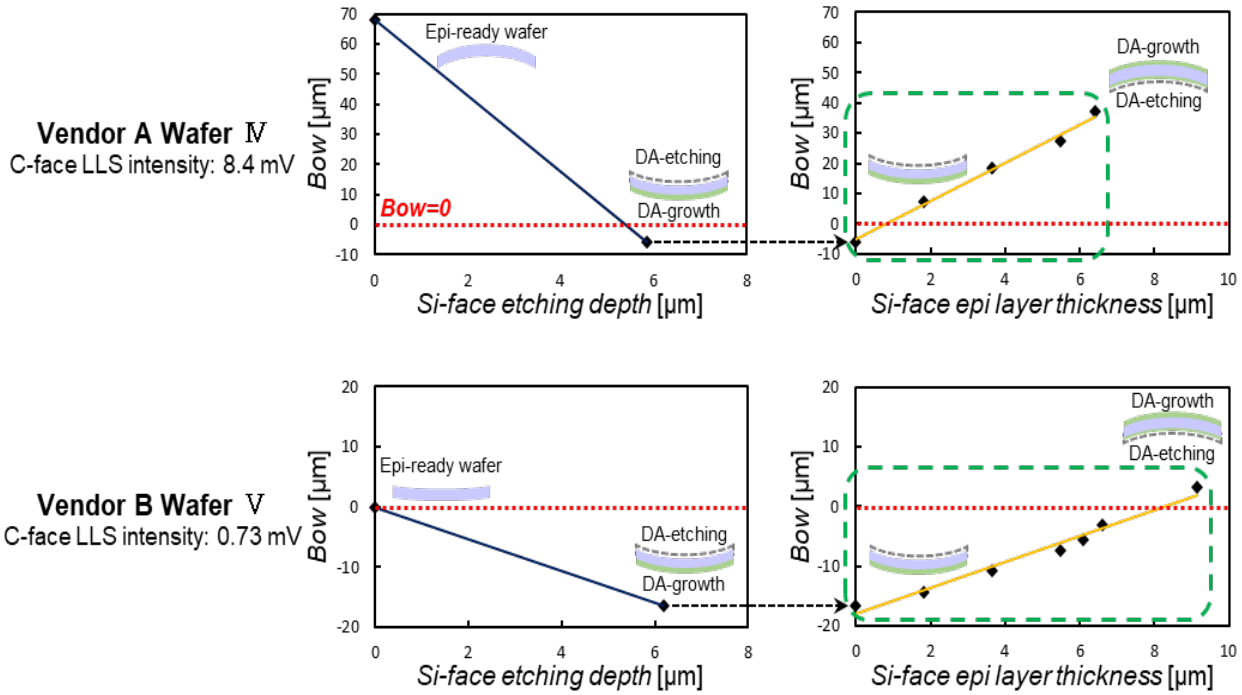


**Fig. 6.** Measurement results of bow change when etching the Si-face and growing the C-face using DA for wafers IV and V and then growing the Si-face and etching the C-face.

Fig. 6. shows the change in wafer bow when wafers from vendors A and B are processed by performing DA-growth on the C-face while DA-etching the Si-face for 2 hours using the DA process. This is followed by DA-growth on the Si-face and DA-etching of the C-face for a total of 40 to 80 minutes over multiple sessions. The graph shows that, when wafers from vendors A and B are processed by DA-growth on the Si-face and DA-etching of the C-face, the bow increases linearly with the epitaxial layer thickness on the Si-face for both wafers (circled by the blue dotted line), despite differences in C-face process quality.

Fig. 7 shows bow control using the DA process on an 8-inch wafer from Vendor D. The initial bow was -11.96 μm. After Si-face etching and C-face growth using DA, the bow decreased to -25.91 μm, but after Si-face growth and C-face etching, it recovered to -0.37 μm. Fig. 8 shows a smooth surface obtained from the LLS mapping after DA-etching of the Si-face [9]. It has also been reported that DA is a method capable of controlling surface roughness, regardless of etching depth and the amount of epitaxial growth [7]. This process allows for the mitigation of device-killer defects on the wafer and consistent control of the bow.

As wafer diameters increase, large warpage is becoming a serious issue. In this study, the demonstrated control of warpage using the DA process for 8-inch large-diameter wafers can significantly contribute to cost savings for large-diameter 4H-SiC wafers and improve wafer yield.

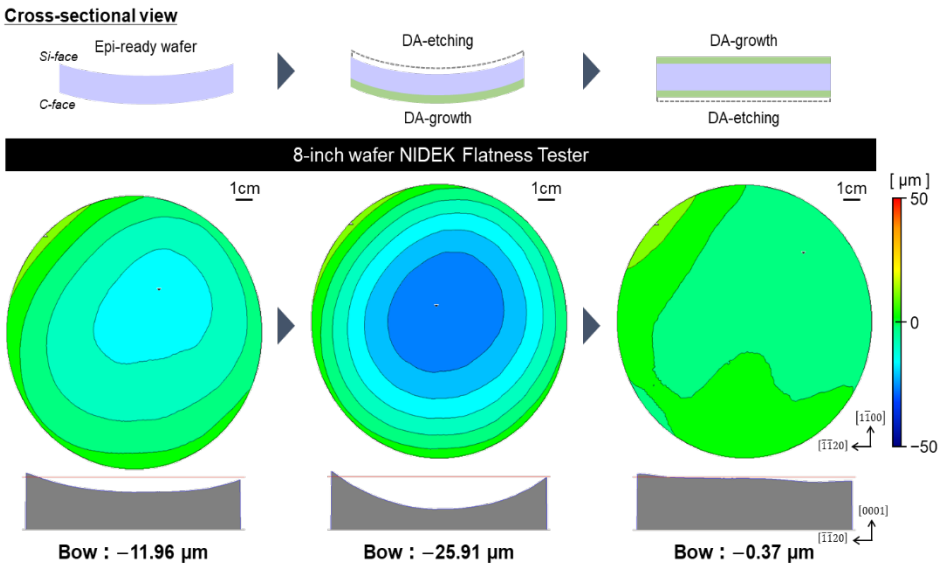


**Fig. 7.** Bow control results for wafer VI using the DA process.

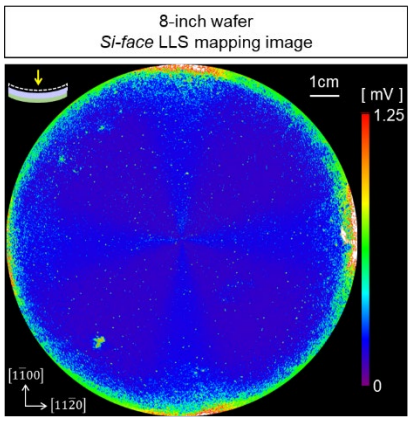


**Fig. 8.** LLS images of the Si-face of wafer VI after DA-etching.

## Summary

This study demonstrates a novel process to control the wafer bow, i.e., the key aspect of overall warpage, of 4H-SiC wafers to any desired value by incorporating Dynamic AGE-ing® (DA) between polishing and CVD epitaxy. Measurements on 43 φ6" epi-ready polished wafers from vendors A, B, C, and D revealed a consistent positive bow bias. Laser light scattering (LLS) evaluations showed that all vendors processed the C-face more roughly than the Si-face, suggesting that residual stress from ingot fabrication induces positive bowing and that vendors may intentionally roughen the C-face (via the Twyman effect) to counteract this stress.

Using the DA process for simultaneous Si-face etching and C-face growth, the wafer bow decreased linearly with increasing C-face growth, while surface roughness was independently controlled. This indicates that wafers with a positive bow can be adjusted to zero or even negative values. Notably, only one wafer with a rough C-face exhibited an increased bow at 120 nm C-face growth, likely due to defect formation mitigating SSD. Additionally, 8-inch wafer bow was controlled from -11.96 μm to -0.37 μm in this mechanism.

Importantly, these results not only confirm that the bow can be tuned to 0 nm but also suggest a new process strategy for high-thickness (≥100μm) epitaxy: pre-adjusting the wafer bow to a negative value prior to epitaxial growth. This approach could help to optimize film deposition and improve overall process yields without adversely affecting subsequent CVD epitaxy.

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**References**

[1] N. Piluso, S. Rinaldi, S. Lorenti, A. Bassi, A. Severino, S. Coffa, An Approach to Predict 4H-SiC Wafer Bending after Back Side Thinning by Substrate Resistivity Analysis, Materials science forum 1004 (2020) 57-62.

[2] F. Guo, C. Shao, X. Chen, X. Xie, X. Yang, X. Hu, X. Xu, Shape modulation due to sub-surface damage difference on N-type 4H–SiC wafer during lapping and polishing, Mater. Sci. Semicond. Process 152 (2022) 107124.

[3] B. Gao, K. Kakimoto, Three-Dimensional Modeling of Basal Plane Dislocations in 4H-SiC Single Crystals Grown by the Physical Vapor Transport Method, Cryst. Growth Des. 14 (2014) 1272-1278.

[4] F. Twyman, Prism and lens making, 2nd ed., Hilger & Watts, London, 1952.

[5] G.G. Stoney, The tensions of metallic films deposited by electrolysis, Proc. R. Soc. Land. A82 (1909) 172-175.

[6] B. Kallinger, P. Berwian, J. Friedrich, G. Muller, A. Weber, E. Volz, G. Trachta, E. Spiecker, B. Thomas, Doping induced lattice misfit in 4H–SiC homoepitaxy, J. Cryst. Growth, 349 (2012) 43-49.

[7] D. Dojima, K. Tayake, K. Shigematsu, K. Toda, T. Kaneko, Macro Step Bunching/Debunching Engineering on 4° off 4H-SiC (0001) to Control the BPD-TED Conversion Ratio by Dynamic AGE-ing®, Defect and diffusion forum, 434 (2024) 165-172.

[8] D. Dojima, K. Shigematsu, K. Tayake, K. Toda, T. Kaneko, Non-Destructive Quantification of In-Plane Depth Distribution of Sub-Surface Damage on 4H-SiC Wafers Using Laser Light Scattering, Defect and diffusion forum 434 (2024) 157-163.

[9] D. Dojima, D. Dansako, M. Maki, K. Toda, T. Kaneko, 4H-SiC Full Wafer Mapping Image of CMP-Finished Sub-Surface Damage by Laser Light Scattering, Defect and diffusion forum 343 (2023) 43-50.