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Active Planarization Method from Rough Surface of 4º-off 4H-SiC (0001) Controlled by Step Bunching and Debunching Mechanism Using Dynamic AGE-ing®

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Abstract. In this study, we developed two planarization mechanisms, macroscopic and microscopic, controlled by adjusting the C/Si ratio during Dynamic AGE-ing® (DA) sublimation etching. Using these mechanisms, we planarized rough 4H-SiC wafers without the use of chemical mechanical polishing (CMP). Macro planarization forms macro step bunching (MSB) using high C/Si ratio DA etching, straightens the steps using step tension, and removes scratch marks caused by mechanical processing. Microscopic planarization involves debunching these MSBs using low C/Si ratio DA etching. It was observed that debunching progressed more quickly on wafers before CMP finishing due to the higher density of MSBs with ramified structures, which serve as starting points for debunching. The rate at which the MSB is shortened by step debunching increases with rising temperature, reaching about 20 μm/min at 1800 °C. By utilizing these mechanisms, we achieved high-quality planarization (initial Ra = 0.6 nm) to Ra = 0.18 nm for φ6-inch 4H-SiC wafers that had not undergone CMP. Furthermore, by performing DA sublimation growth on this planarized wafer, we achieved an in-grown stacking fault (IGSF) density of 0.09 cm^{-2} and a basal plane dislocation (BPD) to threading edge dislocation (TED) conversion ratio of 99.95 %.

Introduction

In the manufacturing of 4H-SiC wafers, mechanical processing is expensive and introduces SSD due to abrasive contact during processing from SiC boules to wafers [1]. SSD leads to BPD propagation and IGSF formation during epitaxial growth, which impair device reliability [2, 3]. To remove SSD and achieve a surface roughness of Ra ≤ 0.2 nm, a stepwise process involving slicing, grinding/lapping, and CMP is commonly employed. In the later stages of the machining process, the higher the precision required, and thus the higher the cost. In addition, it has been reported that SSD is not completely removed even after CMP. Therefore, developing a process that can replace the later stages of the machining process with Ra ≤ 0.2 nm and remove SSD is a significant breakthrough.

Alternatives to CMP, such as plasma etching, efficiently remove damaged layers by preferentially etching weakly damaged areas [4, 5]. However, this results in surfaces with Ra = 0.7 nm and large undulations, which can promote BPD propagation and IGSF formation in the epitaxial layer. Thermal etching, utilizing sublimation at high temperatures, is another non-contact method considered for replacing mechanical polishing.

To control surface morphology using thermal processes, understanding the step terrace structure of 4H-SiC surfaces is essential. 4H-SiC wafers are cut with a 4° off-cut in the [11-20] direction from the (0001) plane to induce step-flow growth, forming step terrace structures. The minimum step height after thermal processing is 0.5 nm (half-unit cell height), but steps with a full unit cell height of 1 nm are more stable. MSBs with many steps bunched together increase surface roughness. Hydrogen etching, a common thermal etching method in CVD process, increases MSB with etching

depth [6]. Once formed, MSBs are stable and difficult to debunch. Therefore, replacing the machining process with a thermal process while ensuring sufficient flatness is challenging.

We previously reported for the first time that MSBs can be debunched into steps of about 1 nm in height by thermal sublimation etching on 4H-SiC on-axis and 4° off-axis substrates under controlled C/Si ratio and high temperature environment. The sublimation process called Dynamic AGE-ing® (DA) enables precise control of surface morphology, achieving both flat and MSB-formed surfaces, regardless of etching depth and grown layer thickness at temperatures between 1500-2000 ℃ [7]. The DA sublimation etching and growth of single crystal SiC wafer is performed in a quasi-closed polycrystalline SiC container, driven by a slight temperature gradient. It can etch more than 10 μm of material while maintaining surface flatness, effectively planarizing rough wafer surfaces. Thus, SSD introduced by machining process can be removed, and the surface can be planarized simultaneously.

By varying temperature, pressure, and C/Si ratio in DA, different surface morphologies can be achieved, enabling macroscopic and microscopic planarization. Macroscopic planarization occurs at high temperatures above 2000 ℃ and high pressures above 1 kPa or under SiC-C phase-equilibrium environment (PE) with high C/Si ratio, forming large step bunching with heights of several tens to hundreds of nanometers. As these large steps sweep across the surface, they effectively planarize rough surfaces by slicing, glinding, and DP [8]. Microscopic planarization performed under SiC-Si PE with low C/Si ratio can debunch MSBs of several 10 nm to 1 nm. We have reported that using the DA process with SiC-Si PE, CMP-finished and MSB-formed surfaces with Ra = 1-5 nm can be reduced to Ra ≤ 0.2 nm. We have also reported that 4H-SiC wafers after mechanical slicing with Ra = 46.2 nm can be reduced to Ra = 0.7 nm by a process combining DA process in a high temperature and pressure environment, SiC-C PE, and SiC-Si PE [9].

One issue with replacing machining process with DA is the undefined initial surface roughness range that can achieve Ra ≤ 0.2 nm. To define and expand this controllable range, it is essential to elucidate the physical mechanisms of macroscopic and microscopic planarization and to control the surface accordingly. In this study, to elucidate the mechanism of 4H-SiC (0001) planarization in thermal sublimation etching, we observed the MSB decomposition process by forming MSBs on surfaces in different initial machining states and debunching by slight DA etching with SiC-Si PE.

Experiments

For the macroscopic planarization experiment, we used 4° off 4H-SiC n-type substrates cut into small pieces of 10 × 10 mm, which had undergone CMP finishing (Ra ~ 0.06 nm) and DP (Ra ~ 0.6 nm) finishing. DA method with SiC-Si PE and SiC-C PE under ultra-high vacuum was conducted at temperatures of 1500-1800 ℃, 10-300 min process times. In the experiment to observe the MSB decomposition rate, an inverted mesa structure (depth:10 μm, width: 20 μm) was created on a substrate where MSBs had formed, using a 532 nm pulsed laser. A φ6-inch DP-finished wafer polished with loose abrasives was used to investigate defect reduction. The surface morphology of microscopic areas from several tens of nanometers to several microns was evaluated by SEM, macroscopic areas of several millimeters by laser microscopy, and the entire wafer surface by Laser light scattering (LLS). The surface roughness value Ra was calculated from AFM images (10 × 10 μm). The etch-pit method was used molten alkali as the defect detection method. After measuring the etch pits using an optical microscope, crystal defects were detected using an object detection AI.

Results

Figs.1 (a), (b) and Figs. 2 (a), (b) show SEM and laser microscope images of the CMP- and DP-finished substrates, respectively. SEM and laser microscope images revealed that the CMP-finished substrate was very flat (Ra = 0.06 nm), whereas the DP-finished substrate was a rough surface (Ra = 0.6 nm). SEM and laser microscope images after DA etching with SiC-Si PE on the CMP- and DP-finished substrates are shown in Figs. 1 (c)-(f) and Figs. 2 (c)-(f). A flat surface with a height of about 1 nm was observed on the CMP-finished substrate after DA etching with SiC-Si PE. On the other hand, MSB was observed on the DP-finished substrate, which was confirmed by laser microscopy

and showed residual scratch marks. The surface morphology of the substrate was hardly changed after additional DA etching with SiC-Si PE.

Next, SEM and laser microscope images of DA etching with SiC-C PE on the CMP- and DP-finished substrates are shown in Figs. 1 (g), (h) and Figs. 2 (g), (h). On these substrates, MSBs with a height of approximately 10 nm were observed. DA etching with SiC-Si PE was used to debunch MSBs formed on CMP- and DP-finished substrates by DA etching with SiC-C PE. MSBs formed on the CMP-finished substrate remained after DA etching with SiC-Si shown in Figs. 1 (i) and (j). On the other hand, MSBs formed on the DP-finished substrate were not observed after DA etching with SiC-Si PE, resulting in a flat surface with steps of about 1 nm in height across the entire substrate area Figs 2 (i) and (j). The results suggest that the surface morphology of the initial substrate makes a difference in the ease of debunching of the MSBs. Fig. 1 (k) and Fig. 2 (k) show that the optimal treatment method depends on the initial surface morphology. For very flat surfaces such as CMP-finished substrates, DA etching with SiC-Si PE is optimal. On the other hand, for rough surfaces such as DP-finished substrates, it was indicated that a flat surface can be obtained by uniformly roughening the entire surface with MSB prior to DA etching with SiC-Si PE.

We investigated the differences in MSBs formed in SiC-C PE due to the different initial substrates. SEM images of DA etching with SiC-C PE on the CMP- and DP-finished substrates are shown in Figs. 3 (a) and (b). MSB formed on the DP-finished substrate showed many ramified structures. On the other hand, no ramified structure was observed in the MSBs formed on the CMP-finished

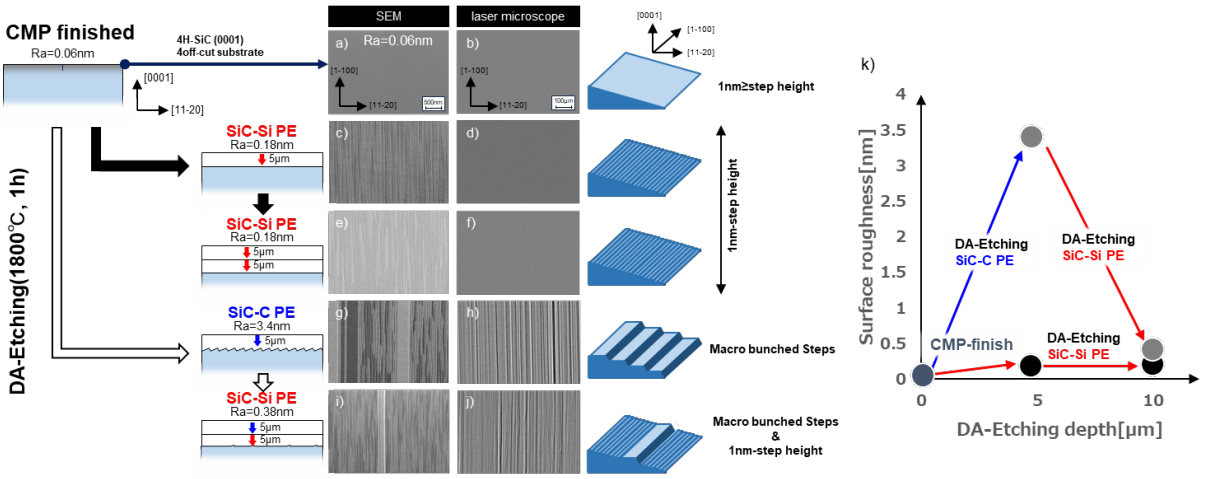

Fig. 1. (a)-(j) SEM and laser microscope images of 4H-SiC (0001) substrates after CMP and DA etching under various SiC-Si and SiC-C PE. (k) the dependence of the etching depth on surface roughness of CMP-finished surface.

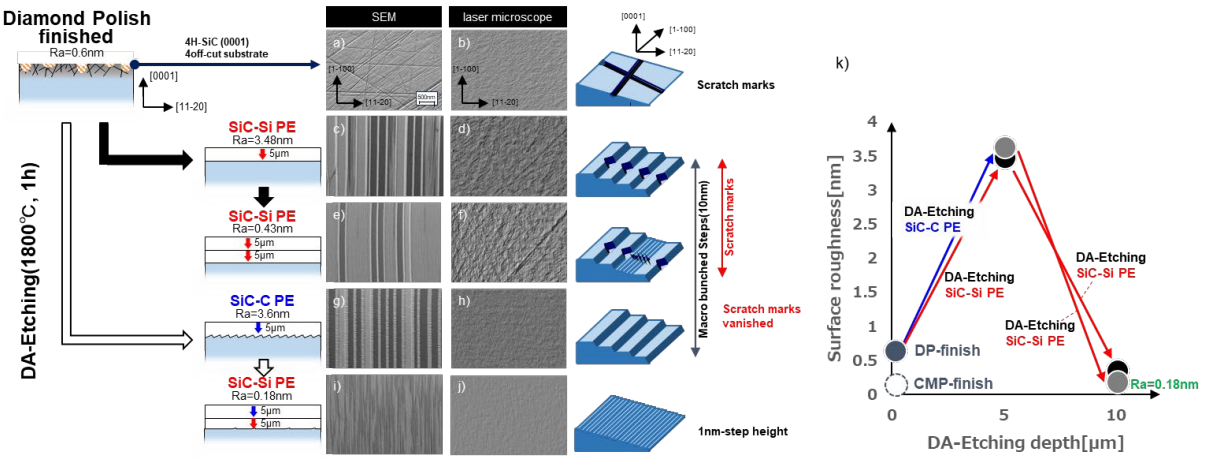

Fig. 2. (a)-(j) SEM and laser microscope images of 4H-SiC (0001) DP-finished substrates and after each DA etching under SiC-Si and SiC-C PE conditions. (k) The dependence of DA etching depth on surface roughness of DP-finished substrate.

substrate. The ramified structure is considered to affect MSB decomposition. Therefore, we performed DA etching with SiC-Si PE (etching depth: 1μm) on the substrates containing MSBs with and without ramified structures. The same locations were observed using SEM on these substrates before and after the treatment. (Figs. 4 (a)-(d)). The MSBs with ramified structures are decomposed starting from the structures, which MSBs shortened toward <1-100>. On the other hand, most of the MSBs without the structures remained after DA etching. It is noted that MSBs without the structures were also decomposed as a rare case.

To investigate the frequency of MSB decomposition, we observed 200 MSBs formed on DP-finished substrates at the same locations before and after DA etching with SiC-Si PE (etching depth: 1 μm). Among these, there were 68 MSBs with ramified structures, of which 46 decomposed, indicating that 68% of these steps bunching decomposed. In contrast, among the 132 MSBs without ramified structures, 25 decomposed due to SiC-Si PE, showing that 14% of these steps bunching

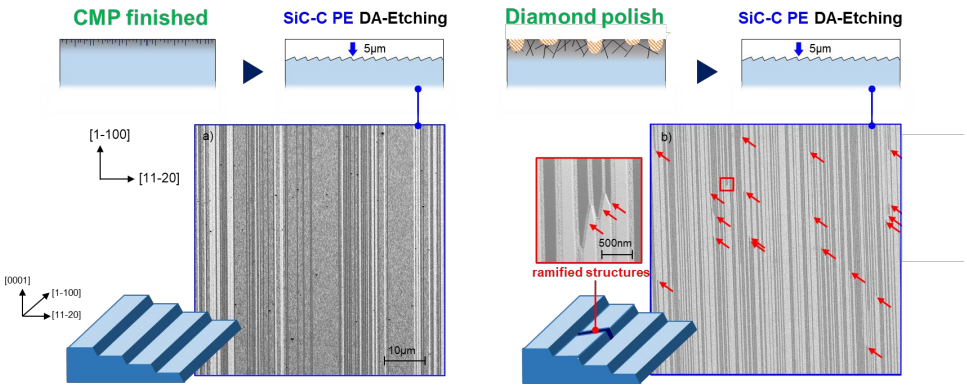

Fig. 3. SEM image of MSB formed on (a) CMP-finished substrate by DA etching with SiC-C PE and (b) DP-finished substrate with by DA etching SiC-C PE.

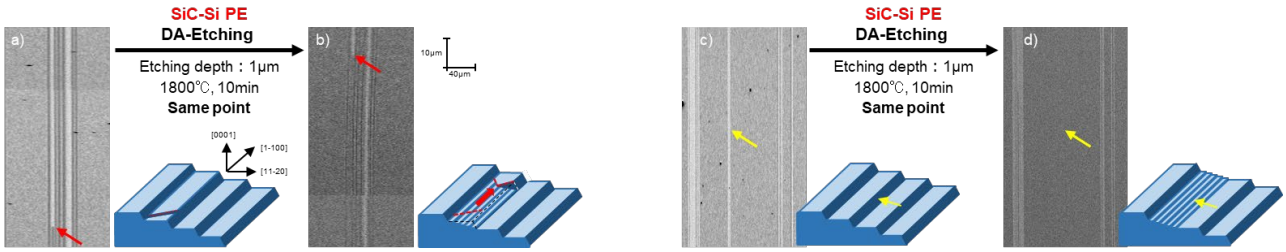

Fig. 4. SEM images of substrates with MSBs before and after DA etching with SiC-Si PE. (a), (b) MSB with ramified structure. (c), (d) MSBs without ramified structure.

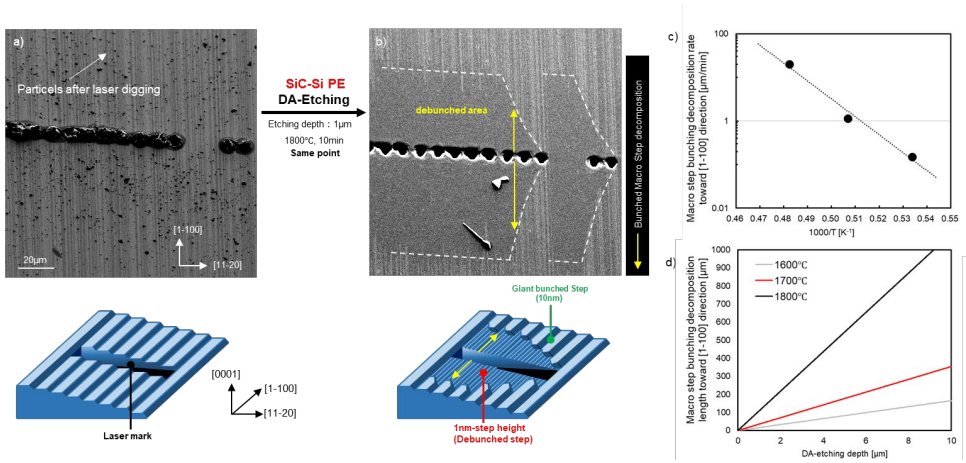

Fig. 5. (a) SEM image of the MSBs formed edges by a laser. (b) SEM image of the same location as in (a) after DA etching with SiC-Si PE. The MSB decomposition rate to [1-100] with respect to (c) etching temperature and (d) etching depth.

decomposed. Therefore, it was found that when the MSB has an edge, such as the ramified structure, the decomposition of the MSB progresses sequentially from the edge toward the <1-100> direction.

To investigate the temperature dependence of MSB decomposition, a laser was applied to the MSB-formed substrate to create an edge on the MSB, which was then DA-etched (1600, 1700, 1800 °C) with SiC-Si PE. Figs. 5 (a) and (b) shows SEM images of the same location before and after DA etching with SiC-Si PE, where the laser was applied. The relationship between the MSB decomposition rate toward [1-100] direction and temperature is shown in Fig. 5 (c), and the relationship between MSB decomposition length and etching depth is shown in Fig. 5 (d). MSB decomposition proceeded faster at higher temperatures and with increasing etching depth.

We have reported an epitaxial defect-free process for CMP-finished substrates by controlling the surface morphology before and after epitaxial growth [7]. This approach required a pre-growth surface roughness of $Ra \leq 0.2$ nm, which posed challenges for DP-finished substrates. The planarization process in this study removed the scratch marks from the substrates, making it possible to fabricate the very flat surface consisting of steps with a height of about 1 nm. Therefore, using the planarization process described above, we attempted surface planarization and epi-defect reduction on the DP-finished φ6-inch wafers. Figs. 6 (a)-(c) shows the AFM, SEM, and LLS images of the DP-finished wafer. Scratch marks were observed on the wafer (Ra = 0.6 nm). Figs. 6 (d)-(f) shows the AFM, SEM, and LLS images of the wafer after the planarization process in this study. The processed wafers were observed to have a flat surface with Ra = 0.18 nm and no scratch marks. This shows that these planarization processes can be adapted to wafers. After the planarization, DA growth in SiC-C PE was performed to create epi-defect-free grown layer. Fig. 7 (a) shows the BPD distribution on a DP-finished φ6-inch wafer before DA process. The density was 584 cm^{-2}. Fig.7 (b) and (c) show the BPD and IGSF distributions after DA planarization process and DA growth. The BPD and IGSF densities were 0.32 cm^{-2} and 0.09 cm^{-2}, respectively. 99.95% of BPDs were successfully converted into TED. The defect density was less than that of direct DA growth on the CMP-finished wafer as shown in Fig. 7 (d) and (e) (BPD density: 2.4 cm^{-2}, IGSF density: 0.95 cm^{-2}).

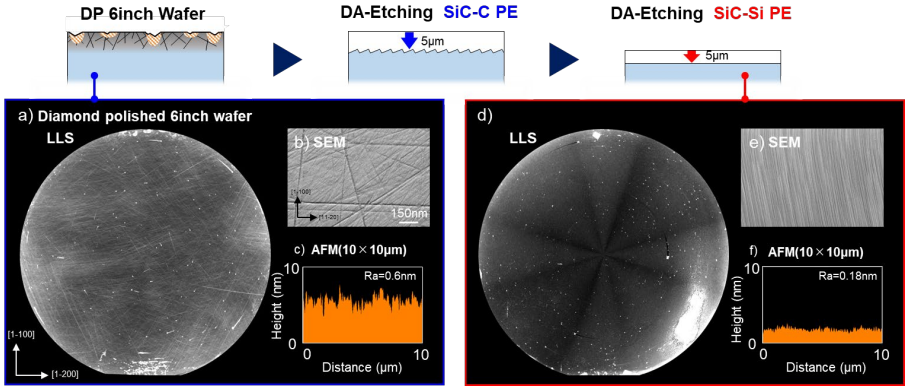

Fig. 6. (a) Laser light scattering (LLS), (b) SEM, and (c) AFM images of the DP-finished φ6-inch wafer. (d) LLS, (e) SEM, and (f) AFM images of the wafer after DA planarization process.

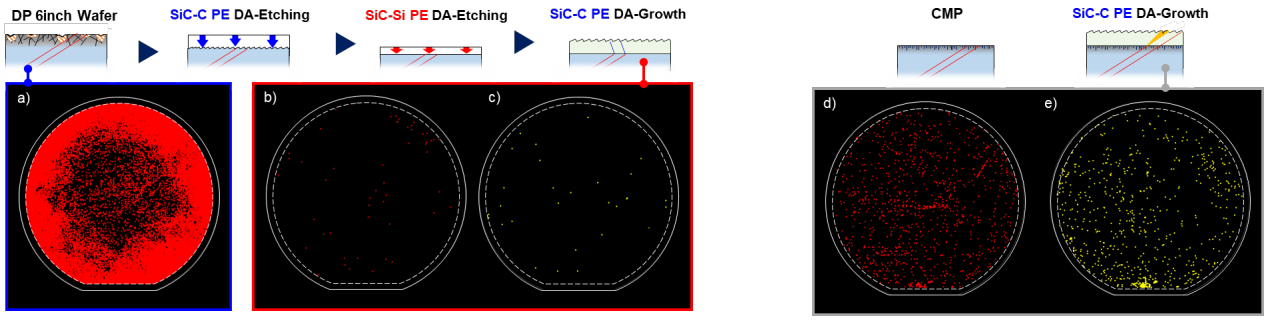

Fig. 7. (a) BPD map visualized by KOH melt etching of DP-finished φ6-inch 4H-SiC (0001). (b) BPD and (c) IGSF maps of the wafer after DA planarization process and DA growth. (d) BPD and (e) IGSF distributions when DA growth was performed directly on the CMP-finished wafer.

Summary

In this study, macroscopic and microscopic planarization mechanisms were established through the controlled adjustment of the C/Si ratio during DA sublimation etching. Utilizing these approaches, we were able to planarize rough 4H-SiC wafers without CMP. Macroscopic planarization was achieved by inducing MSB via DA etching with high C/Si ratio and eliminated scratch marks resulting from machining process. Microscopic planarization was accomplished by DA etching with low C/Si ratio. MSB debunching process occurred more rapidly on wafers prior to CMP, a phenomenon attributed to the higher density of MSBs with ramified structures that serve as initiation sites to debunch. Moreover, the rate at which the MSBs were shortened by step debunching increased with temperature, reaching approximately 20 μm/min at 1800 °C. By employing these mechanisms, high-quality planarization was achieved for φ6-inch 4H-SiC wafers, reducing the roughness (Ra = 0.6 nm) to 0.18 nm without CMP. Furthermore, DA sublimation growth on these planarized wafers resulted in an IGSF density of 0.09 cm^{-2} and a BPD to TED conversion ratio of 99.95 %.

Acknowledgments

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