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The Application of Dynamical Thermal Annealing Processes after Mechanical Slicing as an Integrated Contactless SiC Wafering Method to Control Crystal Defects

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Abstract. We have developed a novel, material-lossless silicon carbide (SiC) wafer manufacturing process that eliminates the need for conventional grinding and polishing. Utilizing a thermal sublimation growth and etching technique called Dynamic AGE-ing® (DA), we simultaneously performed thermal sublimation etching and growth on both the Si-face and C-face of single-crystal SiC wafers. This study investigated the impact of surface undulations—arising during DA planarization of as-sliced wafers with varying slicing qualities—on the densities of basal plane dislocations (BPDs) and in-grown stacking faults (IGSFs) in the epitaxial layers. Our findings demonstrate that larger pre-growth surface undulations correlate with higher BPD and IGSF densities in the DA-grown layers. By optimizing the initial wafer quality and DA process conditions, we achieved epitaxial layers with low defect densities (BPD density of 0.09 cm^{-2} and IGSF density of 1.37 cm^{-2}) without any material loss. This advancement offers a significant breakthrough in SiC device manufacturing, potentially reducing material costs and enhancing device performance by suppressing killer defects in the epitaxial layers.

Introduction

In improving the yield of devices using high-cost 4H-SiC materials, it is crucial to reduce material loss during wafer surface planarization processes and suppress killer defects in the epitaxial growth process. Generally, wafers sliced from SiC boules undergo mechanical processing such as lapping, grinding, and chemical mechanical polishing (CMP) to enhance flatness and remove subsurface damage (SSD) introduced due to contact between the surface and abrasive grains during slicing. In this process, approximately 100 μm (about 20 %) of material loss occurs when producing a 350 μm thick wafer, necessitating efforts to reduce this loss.

Moreover, while CMP-finished wafers exhibit extremely high flatness with $Ra \leq 0.2$ nm, elastic strain that decreases exponentially over several micrometers across the entire wafer remain as SSD. We have reported that this elastic strain causes the formation of in-grown stacking faults (IGSF) and the propagation of basal plane dislocations (BPD) into the epitaxial growth layer [1]. These defects lead to the deterioration of electrical properties during device operation [2]. Therefore, a thermal process that can achieve flatness equivalent to CMP-finished wafers from as-sliced SiC wafers without material loss, and further enable the growth of epitaxial layers without killer defects, would represent a significant breakthrough in SiC device manufacturing processes.

We are attempting to develop a novel, material-lossless SiC wafer manufacturing process that is free from grinding and polishing, using a thermal sublimation growth and etching process called Dynamic AGE-ing® (DA) [3]. DA is a process capable of simultaneously performing thermal sublimation etching or growth on both sides (Si-face and C-face) of a single-crystal SiC wafer (Fig. 1). The single crystal SiC wafer is placed inside a semi-closed polycrystalline SiC container, and heating it forms a phase equilibrium (PE) environment inside. Under this environment, a slight

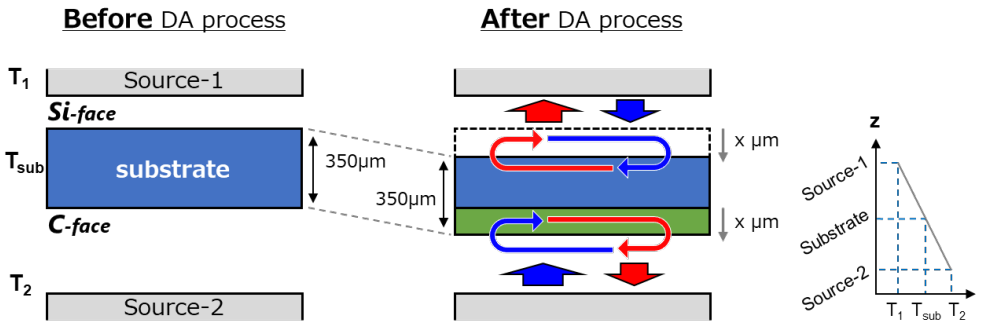

Fig. 1. Schematic diagram of simultaneous control of both sides (Si-face, C-face) of SiC wafer by DA. Since the amount of DA-etching on the Si-face and the amount of DA-growth on the C-face are equivalent, the total thickness of the wafer remains the same before and after DA.

temperature gradient serves as the driving force, causing sublimation growth on the higher temperature side of the wafer and sublimation etching on the lower temperature side. The notable aspect of this method is that by etching one side (Si-face) while simultaneously growing the backside (C-face) at the same rate, it is possible to eliminate material loss during the process. There are three types of DA process conditions depending on the SiC wafer surface planarization method: DA annealing, which maximizes the self-organization effect under high temperature (≥ 2000 °C) and high back pressure (≥1 kPa); SiC-C PE, which utilizes macro step bunching (MSB); and SiC-Si PE, which can debunch step bunching to the full unit cell height of 4H-SiC, which is 1 nm. Here, SiC-C PE and SiC-Si PE represent environments with high C/Si ratio and low C/Si ratio, respectively, controlled by the introduction of Si supply materials [4].

We have demonstrated that by sequentially applying these processes—DA-annealing, SiC-C PE, and SiC-Si PE—a multi wire saw (MWS) as-sliced SiC wafer with an initial roughness of Ra = 46.2 nm can be planarized to Ra = 13.7 nm after DA-annealing, then to Ra = 6.1 nm after SiC-C PE etching, and finally to Ra = 0.7 nm after SiC-Si PE etching [3]. On the other hand, when using a CMP-finished surface as the initial surface, a surface flatness of Ra ≤ 0.2 nm can be achieved after DA-etching in a SiC-Si PE environment [4]. In this case, using DA-growth, we have demonstrated a BPD-to-TED conversion rate of 100% and an IGSF density of 0.1 cm^{-2} within an area of 10 × 20 mm^2 [2, 4]. The cause of the large Ra after the planarization process when using a mechanically as-sliced SiC wafer as the initial surface is the undulations that appear on the SiC surface [3].

We refer to macro-scale uneven structures with a periodicity of several micrometers perpendicular to the steps as undulations. Undulations can form locally wide (0001) terraces, potentially causing two-dimensional nucleation that leads to defect formation. However, the cause of undulations occurring during the DA planarization process on MWS as-sliced SiC wafers and the extent of their impact on epitaxial growth remain unclear.

Therefore, in this study, we performed DA planarization processes and DA-growth on three as-sliced wafers (loose abrasive) with different MWS slicing qualities to investigate how the undulations present on the pre-growth surface, which depend on the initial substrate, affect the BPD and IGSF densities in the epitaxial growth layer. Furthermore, to verify the extent to which terrace length adversely affects DA-growth, we conducted DA-growth on CMP-finished low off-angle substrates and examined the growth modes that emerge.

Experiments

In this study, we used 3-inch and 6-inch 4H-SiC as-sliced wafers with a 4° off-cut toward the [11-20] direction (designated as Wafers A, B, and C) as samples. These wafers were sliced using a multi-wire saw with loose abrasive. To measure the surface morphology of the Si-face of these wafers, we employed the laser light scattering method [5], atomic force microscopy (AFM), and scanning electron microscopy (SEM). To flatten these as-sliced wafers, we performed three DA processes (Fig. 2). First, we conducted DA-annealing (Step-1) in a high-temperature (≥2000 °C) and high

backpressure (≥1 kPa) environment. Next, a DA-etching process (Step-2) in SiC-C PE was performed on the Si-face at 1800 ℃ and a back pressure of 10^{-5} Pa. Subsequently, the DA-etching process (Step-3) in SiC-Si PE was carried out under the same conditions. At this stage, AFM measurements were performed to confirm the undulations on the Si-face. Finally, we conducted DA-growth (Step-4) on the Si-face of these wafers to fabricate an epitaxial growth layer free of BPDs and IGSFs. The conditions were SiC-C PE at 1800 ℃ and a back pressure of 10^{-5} Pa. For the measurement of BPD and IGSF densities, we used UV photoluminescence (PL) imaging (light source: Hg–Xe lamp, excitation wavelength: 313 nm, detection filter: 510–610 nm band-pass filter) and KOH etching (500 ℃, 6 min 20 s). An electronic caliper was used for wafer thickness measurements.

To investigate the growth modes of DA-growth on low off-angle substrates, we used CMP-finished 4H-SiC substrates with off-angles of on-axis, 0.8°, 1°, 2°, and 4°. DA-growth was performed in SiC-Si PE and SiC-C PE at temperatures of 1600 ℃ and 1800 ℃, with a back pressure of 10^{-5} Pa. A Nomarski differential interference contrast (DIC) microscope was used to observe the surface morphology of these substrates.

Results

Figs. 2 (a)-(c) shows the Si-face mapping images of Wafer A, B, and C obtained by laser light scattering method. The mode values of light scattering intensity for Wafer A, B, and C were 217 mV, 3983 mV, and 3819 mV, respectively. The higher its intensity, the greater the surface roughness Ra [5]. Therefore, Wafer A is assumed to have a smaller surface roughness than Wafer B and C. After the planarization process (Step-1, 2, 3) by DA-annealing and DA-etching was performed on these three as-sliced SiC wafers, the surface of the Si-face was measured by AFM. The cross-sectional height profiles of each wafer are shown in Figs. 2 (e)-(g). The undulation was observed on the surface of these wafers. The peak-to-valley of Wafer A, B, and C are 8.2 nm, 11.8 nm, and 21.6 nm, respectively. The surface of Wafer A is estimated to have the smallest undulation. On the other hand, in the microscopic view shown in Figs. 2 (g)-(i), these wafers have a flat surface covered with steps of 1 nm in height.

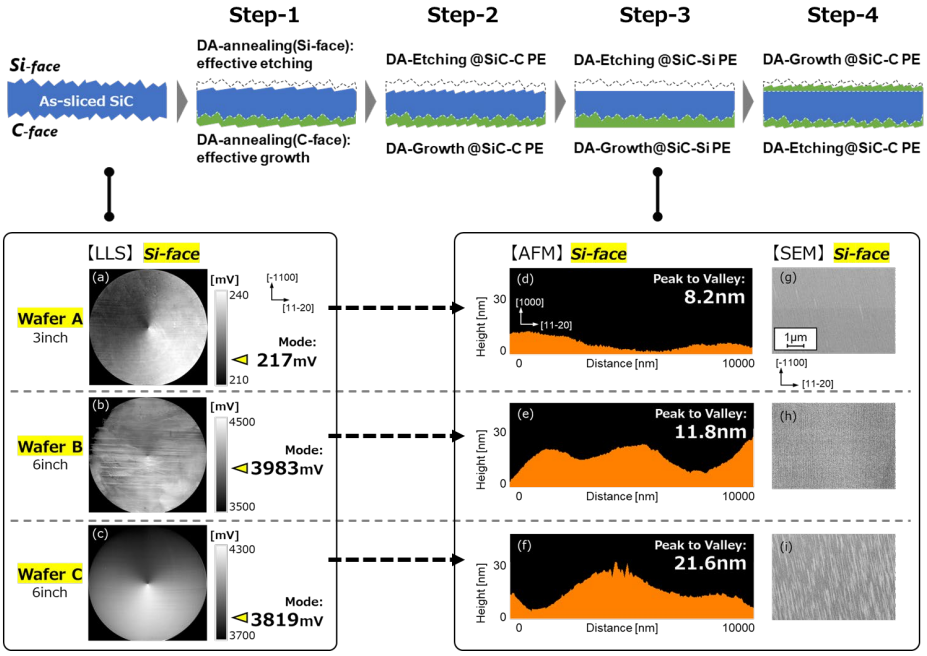

Fig. 2. (a)-(c) Mapping images of the Si-face of Wafer A, B, and C obtained by laser light scattering method. Cross-sectional height profiles (d)-(f) and SEM images (g)-(i) of the Si- face of Wafer A, B, and C after DA-etching with SiC-Si PE (Step-3).

Then, DA-growth under SiC-C PE (Step-4) was performed on these wafers to investigate the BPD and IGSF density of the epitaxially grown layers. The defect densities of the DA-grown layers on Wafer A, B, and C measured in the central Φ1inch range of the wafer were 0.2 cm^{-2}, 10.5 cm^{-2}, and 25.1 cm^{-2}, respectively. The relationship between the defect densities and the peak-to-valley values of the surfaces of the Si-face after DA-etching under SiC-Si PE (Step-3) is shown in Fig. 3. According to this graph, if the undulation of the surface before its growth is large, it causes a larger BPD/IGSF density in the DA-grown layer.

Figs. 4 (a) and (b) show PL images of Wafer A before and after DA-growth under SiC-C PE (Step-4). These images are in the same area. BPD observed before DA-growth is no longer observed after the growth (Step-4). The BPD and IGSF distributions of the DA-grown layer on Wafer A are shown in Figs. 4 (c) and (d), respectively. It is noted that 5 mm from the edge of the wafer is excluded. The BPD and IGSF densities for the entire wafer were 0.09 cm^{-2} and 1.37 cm^{-2}, respectively. The epitaxial layer with low defect density can be grown on as-sliced SiC wafer with loose abrasive (Wafer A) without material loss by integrating the macroscopic-scale planarization function and the microscopic surface control function of the DA process.

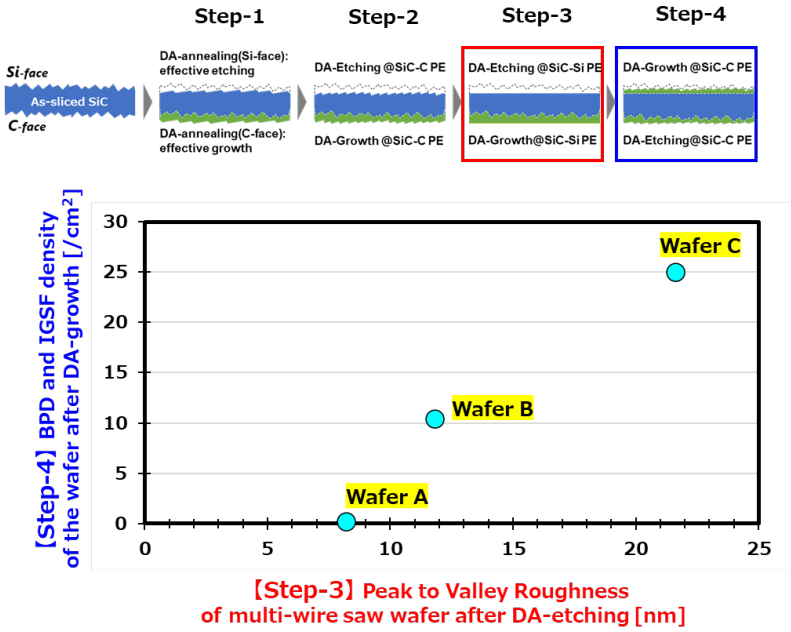

Fig. 3. The relationship between BPD and IGSF density of DA-grown layer and peak-to-valley after DA-etching under SiC-Si PE (Step-3).

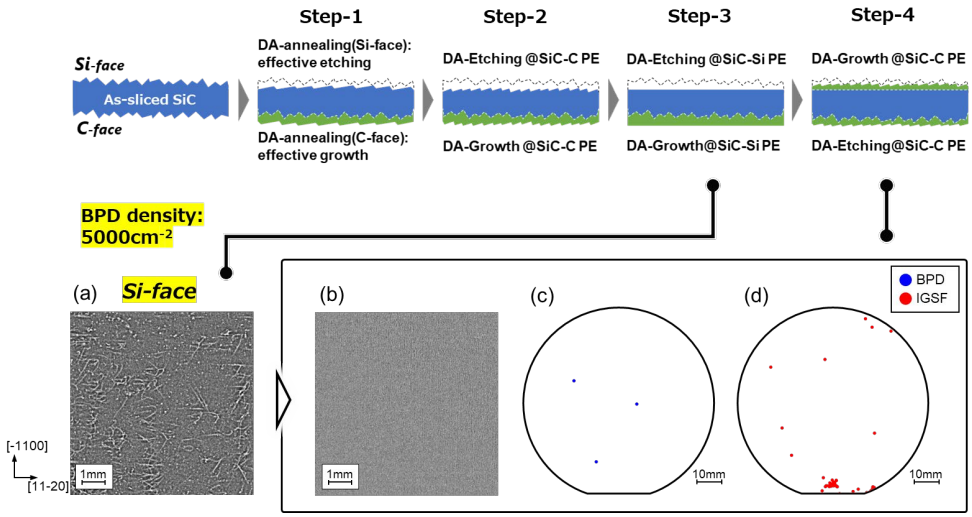

Fig. 4. (a), (b) PL images of Wafer A after DA-etching under SiC-Si PE (Step-3) and DA-growth under SiC-C PE (Step-4). (c) BPD and (d) IGSF distributions of DA-grown layer on Wafer A.

Fig. 5 shows the variation of total thickness of Wafer A by DA-annealing and DA-etching for planarization, and DA-growth for epitaxial growth. The wafer total thickness increased by about 20 µm from 959 µm to 981 µm before and after these DA processes. It indicates that material loss, such as occurs in conventional machining processes for planarization, has been completely suppressed in the DA process.

Then, Fig. 6 shows Nomarski differential interference contrast (DIC) microscope images of the Si-face of on-axis and 0.8°, 1°, 2°, and 4° off-cut 4H-SiC substrates after DA-growth at temperatures of 1600 ℃ and 1800 ℃ in both SiC-Si PE and SiC-C PE environments. Substrates with smaller off-cut angles have wider terraces formed by the steps on their surfaces; therefore, during epitaxial growth under conditions with short diffusion lengths, heteropolytypes are more likely to be incorporated due to two-dimensional nucleation. Since DA-growth in SiC-C PE does not result in the incorporation of heteropolytypes even on the wide terraces of on-axis substrates, it is considered to have a very long diffusion length. Even under such growth conditions with a long diffusion length, epitaxial growth layers with high densities of BPDs and IGSFs were formed on substrates like Wafer B and C, which had large undulations after DA-etching under SiC-Si PE (Step-3). This suggests that the undulations on the SiC surface before epitaxial growth induce BPD propagation and IGSF formation into the grown layer. Therefore, it is considered that in as-sliced wafers with better surface quality after slicing, or in wafers that have undergone further mechanical processing such as lapping or grinding, it is possible to fabricate epitaxial growth layers with sufficiently low defect densities using this process.

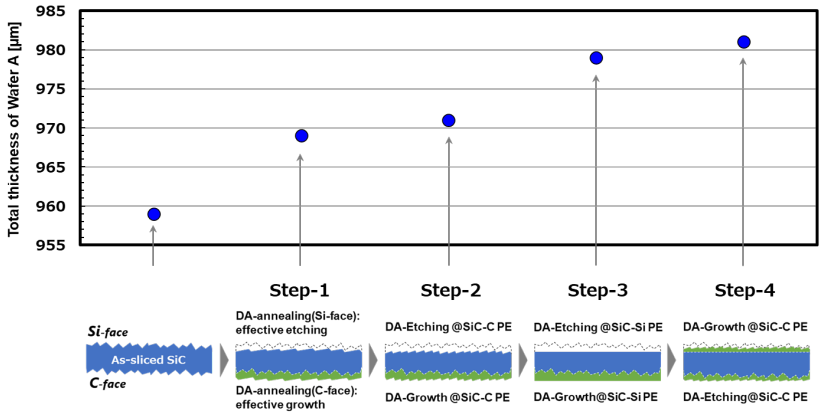

Fig. 5. The Variation of total thickness of Wafer A during DA Processes.

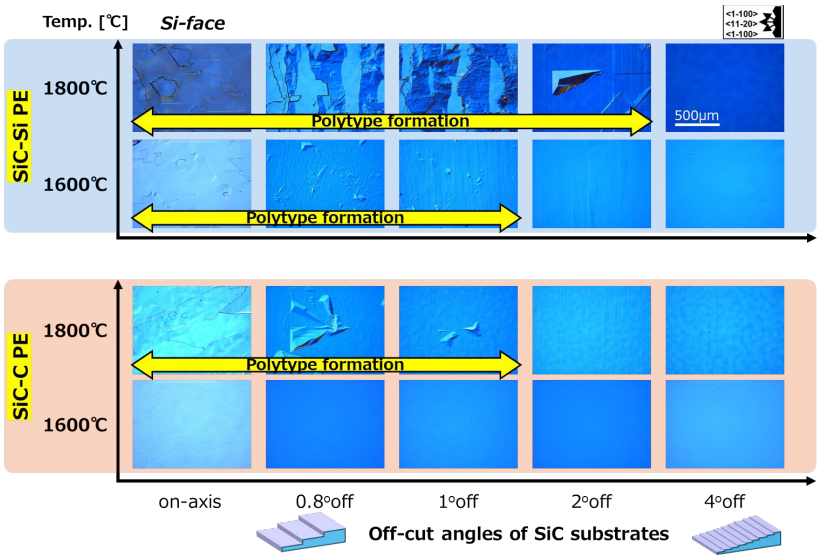

Fig. 6. Nomarski DIC microscope images of Si-face of on-axis, 0.8, 1, 2, 4°off 4H-SiC substrates after DA-growth (Temperature:1600 ℃ ,1800 ℃) under SiC-Si or SiC-C PE.

Summary

In this study, we introduced a novel, contactless silicon carbide (SiC) wafer manufacturing process that eliminates material loss and minimizes crystal defects by utilizing the Dynamic AGE-ing® (DA) sublimation growth and etching method. We sequentially applied DA-annealing, SiC-C phase equilibrium etching, and SiC-Si phase equilibrium etching to as-sliced SiC wafers, achieving significant planarization without the need for grinding or polishing. Our investigation revealed a quantitative correlation between the peak-to-valley (P-V) undulation heights after DA planarization, and the defect densities in epitaxial layers after DA-growth. Specifically, Wafer A had the LLS intensity of 217 mV, the P-V of 8.2 nm, and the defect density of 0.2 cm^{-2}. Wafer B showed the LLS intensity of 3983 mV, the P-V of 11.8 nm, and the defect density of 10.5 cm^{-2}, while Wafer C exhibited the LLS intensity of 3819 mV, the P-V of 21.6 nm, and the defect density of 25.1 cm^{-2}. These results demonstrate that higher initial surface roughness leads to larger surface undulations after planarization, which correlate with increased defect densities in the epitaxial layers. By optimizing the initial surface quality through improved slicing techniques that reduce LLS intensity after Step 1 and carefully controlling the DA process conditions, we successfully fabricated epitaxial layers with low defect densities (BPD density of 0.09 cm^{-2} and IGSF density of 1.37 cm^{-2}) without any material loss on to the MWS sliced φ3 inch 4H-SiC (0001) wafer. The total wafer thickness increased by approximately 20 μm after the DA processes, confirming the absence of material loss. This innovative, material-lossless DA process holds significant promise for enhancing the yield and performance of SiC-based devices. Our findings highlight the importance of initial wafer quality and provide valuable insights into reducing material costs and suppressing killer defects in epitaxial layers, representing a substantial advancement in SiC device manufacturing technology.

Acknowledgments

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