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Isolation Structure for Monolithic Integration of Planar CMOS and 1.7 kV Vertical Power MOSFET on 4H-SiC by High Energy Ion Implantation

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Abstract. In this study, we developed an ion implantation process to create a P-type junction isolation (P-iso) structure, which effectively isolates CMOS and 1700-V VDMOSFET devices on a single 4H-SiC wafer. To ensure a sufficiently high blocking voltage and to prevent punch-through or reach-through in all p-n junctions during operation, Sentaurus TCAD was used to optimize the conditions for the P-well, N-well, P-iso region, and multi-floating zone (MFZ) design. A high-energy ion implantation, reaching up to 2.5 MeV, was then conducted to verify the breakdown voltage (V_{BD}) of the P-iso and MFZ structures. Experimental verification confirms a breakdown voltage (V_{BD}) exceeding 2000 V.

Introduction

As SiC device fabrication technology matures, the development of SiC integrated circuits (ICs) has become both possible and attractive [1-4]. The need for SiC CMOS arises from several concerns associated with using Si substrates for circuits that drive power MOSFETs. Si off-chip circuits require long conduction lines to control the gate of power MOS devices, leading to increased area consumption and parasitic effects such as electrical signal overshoot or oscillation caused by parasitic parameters [5]. Additionally, Si ICs lack thermal stability, whereas SiC power devices can operate at high temperatures and in harsh environments [6-7]. Therefore, a heat sink is essential to dissipate heat in hybrid power systems, potentially undermining the exceptional physical properties of SiC.

To integrate planar CMOS with a vertical power MOSFET on a single chip, the N-well of the PMOSFET must be isolated from the n-type substrate that serves as the drain of the power MOSFET. Without this isolation, a significant potential could be conducted to the body of the PMOSFET when the power MOSFET is in blocking mode, leading to malfunction of the CMOS circuits. A monolithic

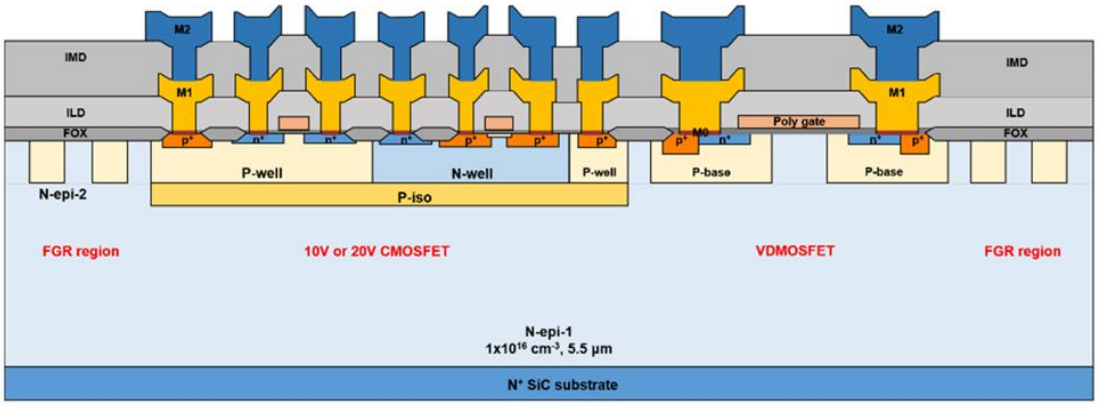

Fig. 1 Schematic cross-sectional structure of the monolithic integration of CMOS and 600 V VDMOSFET on 4H-SiC using P-iso structure [4].

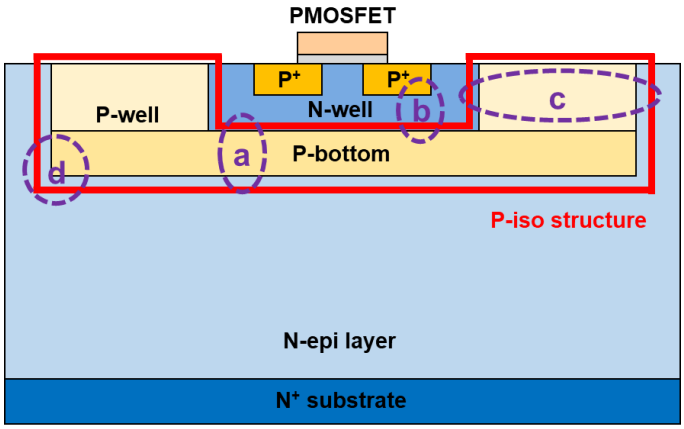

Fig. 2 Schematic cross-sectional P-iso structure and the four criteria.

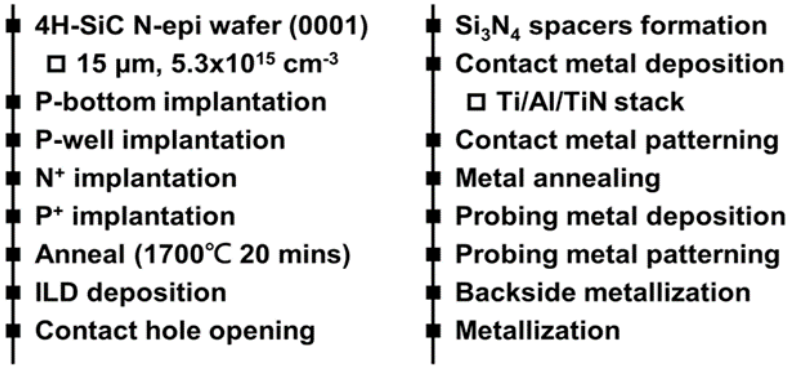

Fig. 3 Main process steps to fabricated the P-iso test structure.

integration of SiC CMOS circuits and 600-V-class VDMOSFET has been demonstrated by using the P-iso structure formed by P-bottom ion implantation followed by n-type epitaxial layer growth as shown in Fig. 1 [8]. Since Al atoms may out-diffuse during the growth of the n-type epitaxial layer and contaminate the epi-tool, it is problematic for production. In light of this, a single epitaxy method combined with high-energy implantation can effectively separate the N-well from the epi-layer, simplifying the process and reducing contamination issues. In this work we demonstrate a P-iso structure formed by high energy ion implantation achieving an isolation ability beyond 2 kV.

Experiments

We primarily used TCAD simulations to introduce the P-iso structure through high-energy ion implantation and conduct a thorough investigation to determine the optimal conditions. Fig. 2 presents a cross-sectional schematic diagram of a PMOSFET featuring the P-iso structure. To ensure isolation under reverse bias, the P-iso structure design must address several factors: (a) reach-through at the N-well/P-bottom and P-bottom/N-epi junctions. (b) punch-through at the P+/N-well and N-well/P-bottom junctions. (c) lateral reach-through at the N-well/P-well and P-well/N-epi junctions. (d) the P-iso edges can withstand the high voltage from the drain of vertical power MOSFET. The low-voltage CMOS is designed to operate at a supply voltage of 20 V. To ensure flexibility, a 20% higher voltage (24 V) was applied in the simulation. The target voltage rating for the VDMOSFET is 1.7 kV, with the edge termination design requiring a V_{BD} exceeding 2 kV.

According to the simulation results, test structures were designed to verify the 1.7 kV P-iso structure. The main fabrication steps are illustrated in Fig. 3, while Fig. 4 presents the cross-sectional and top views of the test structure. The starting material is an N-type SiC substrate, overlaid with an N-type SiC epitaxial layer doped with nitrogen, featuring a thickness of 15 μm and a concentration of 5.3×10^{15} cm^{-3}. The buffer layer is 1 μm thick with a doping concentration of 1.0×10^{18} cm^{-3}. The

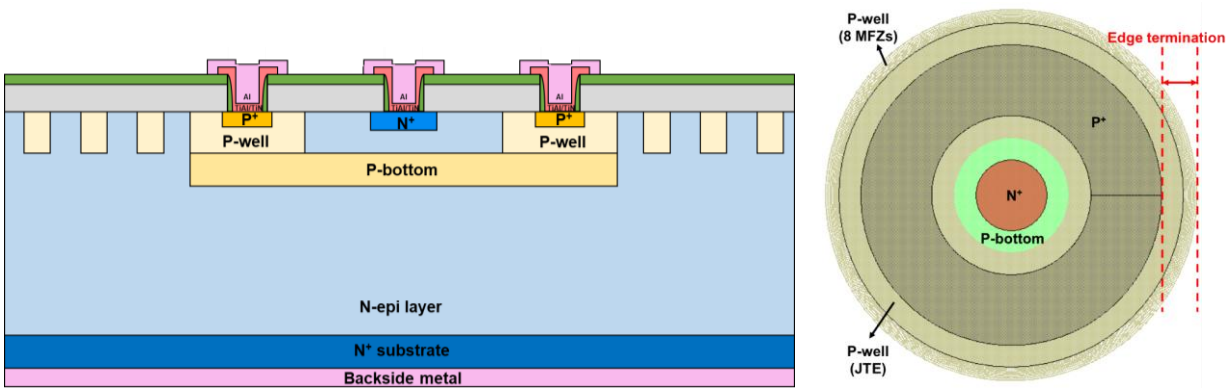

Fig. 4 (Left) Cross-sectional and (right) top view of the P-iso text structure.

surface of this epitaxial layer is (0001) Si-face, angled 4º off-axis toward the $\{11\bar{2}0\}$ direction. In this structure, the electrode potential of the N-well is applied to 24 V, and the P-well to 0 V. Since the P-iso is connected to the P-well, its potential is also 0 V, while a high voltage is applied to the substrate. The actual V_{BD} is determined by the voltage at which the substrate current reaches 1 μA.

Results and Discussion

TCAD simulation began with an ideal one-dimensional parallel plate junction, free of edge corners, was modeled, including the N-well, P-well, and P-bottom, with fixed well conditions. Fig. 5 shows the breakdown voltage as a function of ion implantation energy for the P-bottom at different doses. When the dose is $1x10^{13}$ cm^{-2}, reach-through occurs in the P-bottom, resulting in a V_{BD} significantly lower than 1.7 kV. As the dose increases beyond $2x10^{13}$ cm^{-2}, V_{BD} exceeds 2.4 kV and the breakdown mechanism changes to avalanche breakdown. The results also indicate that higher ion implantation energy reduces the likelihood of reach-through, as increased energy raises both R_p and ΔR_p, leading to a thicker P-bottom layer that is more resistant to reach-through. Later in this paper, the P-bottom implantation dose is maintained at 3.0×10^{13} cm^{-2}.

Next, the susceptibility of the N-well to punch-through under reverse bias at both the P+/N-well junction and the N-well/P-bottom junction must be addressed. The depth of the N-well, influenced

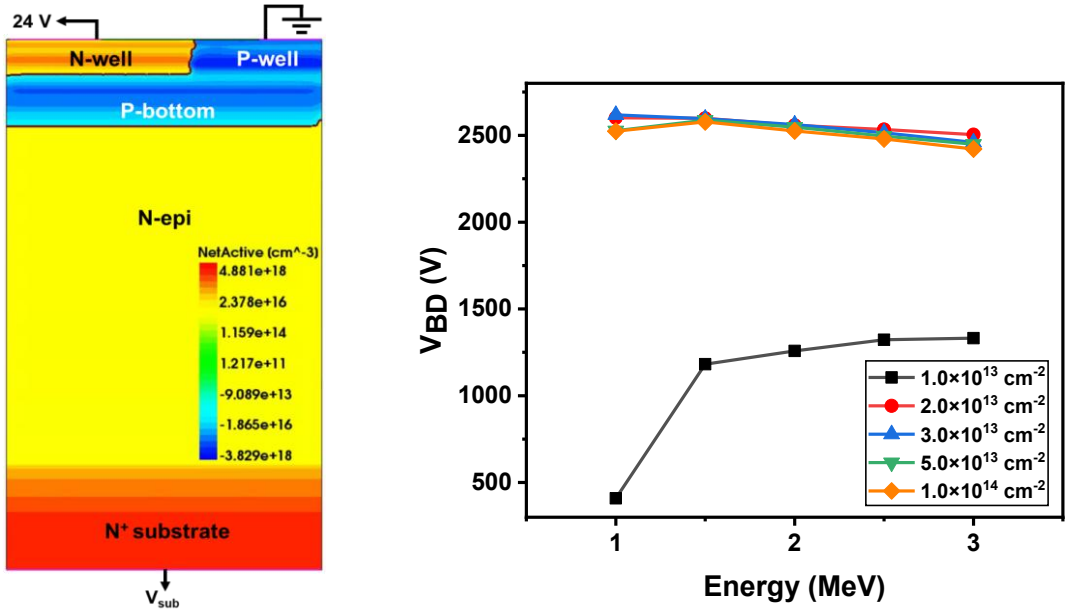

Fig. 5 (Left) Simulated structure and (right) Breakdown voltage as a function of ion implantation energy of the P-bottom with difference doses. (Criterion a)

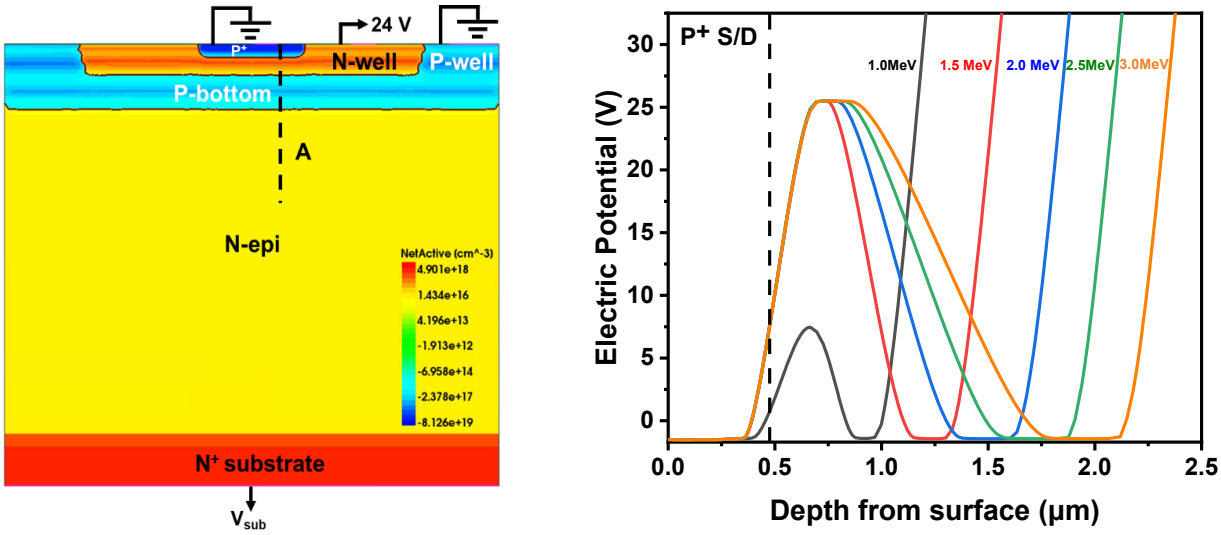

Fig. 6 TCAD simulated electrical potential distribution along the cut line A at substrate bias 2000 V. (Criterion b)

by the ion implantation energy of the P-bottom, is critical; insufficient depth could lead to punch-through during CMOS operation. Simulations were performed using the potential setup shown in Fig. 6, which models a 20 V-operated CMOS inverter in a low-output state under high substrate bias, with the substrate set to 2000 V. When the P-bottom implantation energy is 1.5 MeV or lower, a narrow plateau at the maximum potential can be seen in Fig. 6, indicating a risk of punch-through. To avoid this, it is recommended that the implantation energy exceed 1.5 MeV to ensure the N-well is deep enough to prevent punch-through.

The P-well serves as the pick-up layer for the P-bottom, stabilizing its electric potential and preventing it from remaining in a floating state. The width of the P-well should be kept as small as possible to minimize the layout area it occupies; however, caution must be taken to avoid lateral reach-through if the P-well is too narrow. Fig. 7 shows the relationship between the V_{BD} and the width of the P-well. Though there appears to be no significant dependence between them, likely because the V_{BD} is limited to around 1050 V due to the concentration of the electric field at the lower edge corner of the P-iso structure because edge termination structure is not included in this simulation. We can observe that higher ion implantation energy results in a higher V_{BD}. As the implantation energy

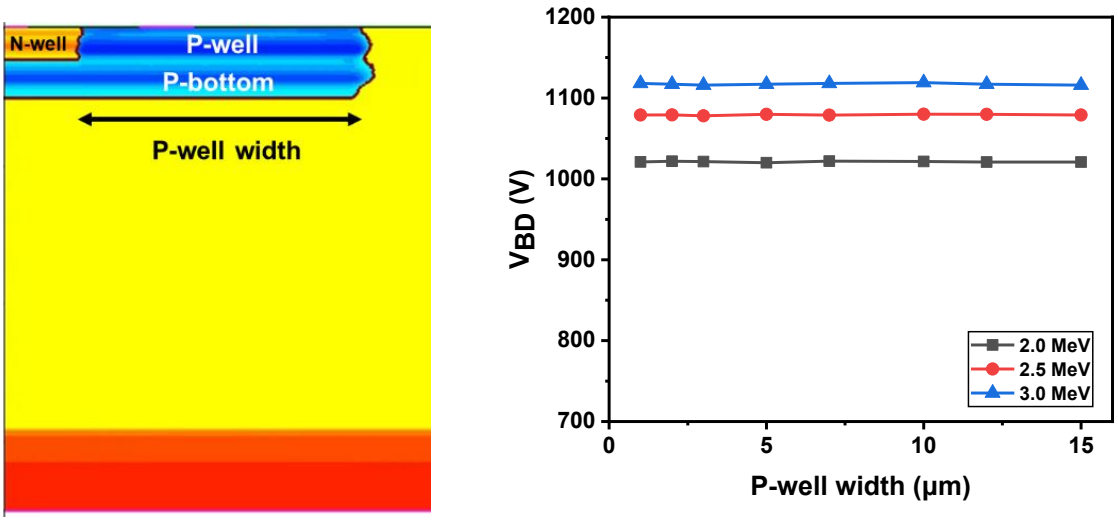

Fig. 7 TCAD simulated breakdown voltage as a function of the width of P-well. (Criterion c)

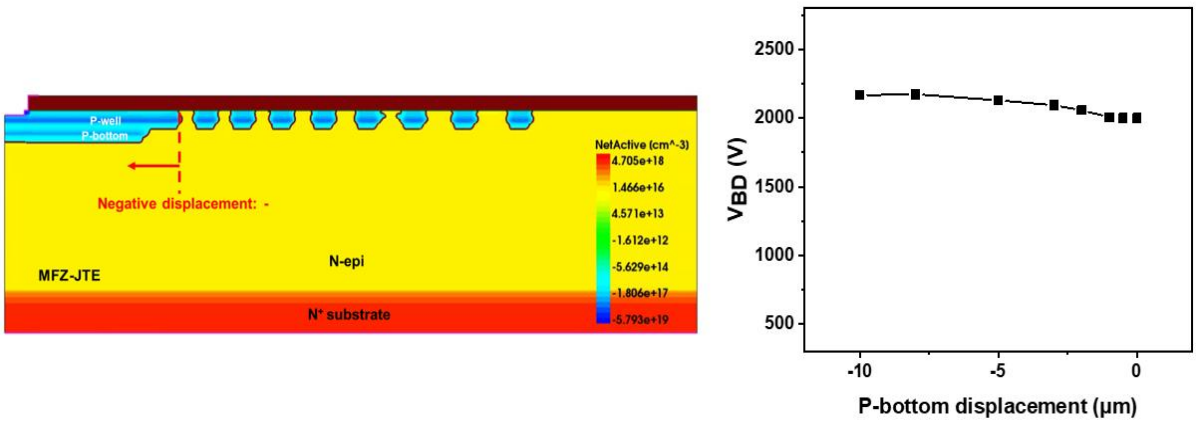

Fig. 8 TCAD simulated breakdown voltage as a function of the displacement of P-bottom to P-well. (Criterion d)

for the P-bottom increases, it penetrates deeper, reducing the overlap between the P-well and P-bottom. This reduced overlap decreases the doping concentration gradient at the lower edge corner of the P-iso structure, leading to a higher V_{BD}.

Continue the previous paragraph, we need an edge termination design to protect the corner of the P-bottom and MFZ-JTE is employed in this work. After optimizing the structural design, the width of the JTE was set to 15 μm, and an 8-zone MFZ configuration was selected. Each zone has a width of 1.5 μm, with the spacing between rings set to 1.7, 1.7, 1.9, 2.1, 2.3, 2.5, 2.9, and 3.3 μm from the innermost to the outermost zone as shown in Fig. 8. The P-bottom is initially aligned with the P-well. The V_{BD} of this edge termination structure is approximately 2000 V, about 80% of the V_{BD} of the parallel plate junction, meeting the blocking voltage requirements. Finally, the relative position between the P-bottom and P-well should also be simulated, as the corner might protrude due to lateral diffusion from implantation or process alignment inaccuracies. A negative displacement of the P-bottom effectively extends beyond it, helping to disperse the electric field and increase the V_{BD}. When the P-bottom is displaced by 8 μm, the V_{BD} is maximized, improving by approximately 8.7%.

Fig. 9 demonstrates that the isolated PMOSFET exhibits identical transfer characteristics at a substrate bias of either 0 V or 2 kV, indicating complete isolation between the N-well and N-epi. Using the same P-bottom ion implantation conditions, Fig. 10 shows the V_{BD} as a function of epi-layer thickness with varying doping concentrations. This confirms that the high-energy ion implantation method can effectively form a P-iso structure, even for devices with higher voltage ratings.

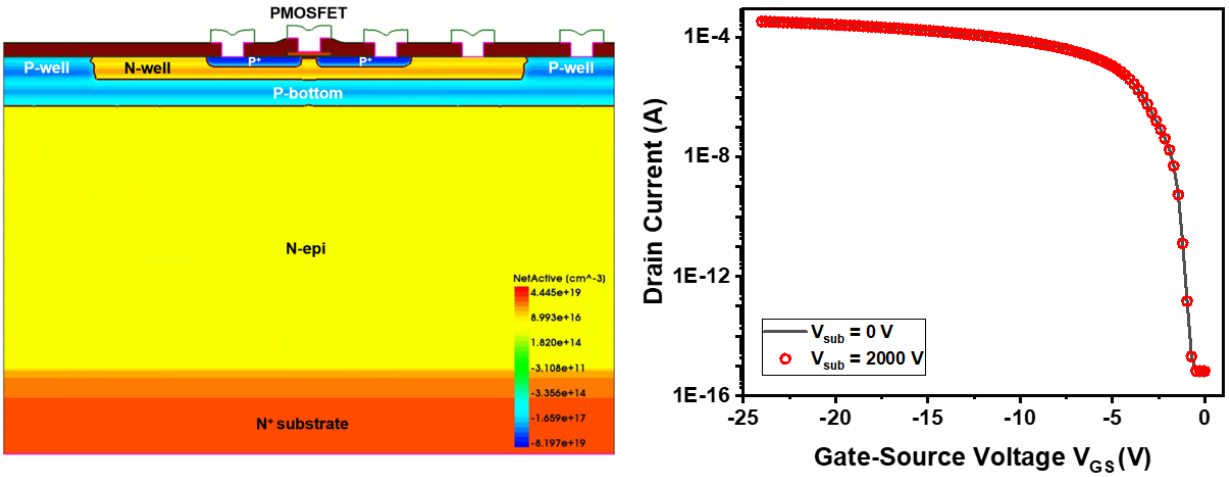

Fig. 9 TCAD simulated transfer characteristics of a PMOSFET in the isolated N-well at substrate bias of 0 V and 2000 V.

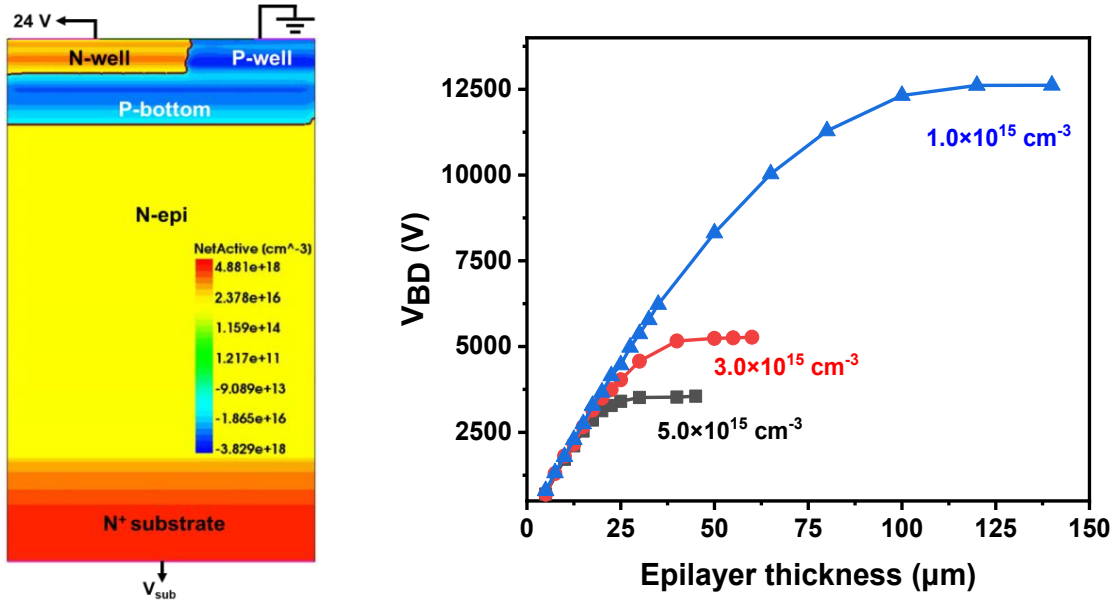

Fig. 10 TCAD simulated breakdown voltage as a function of epi-layer thickness with different doping concentration.

The simulation results are verified by the test structure shown in Fig. 3. Fig. 11 shows the SIMS profile of the P-bottom and simulated results by SRIM and TCAD. Both P-bottom profiles are quite similar, with the SIMS-analyzed profile showing a slight tail at the end. The SRIM simulation does not account for channeling effects in the crystal, so the deep tails present in the implanted profile are not evident in the figure. Fig. 12 shows the measured blocking characteristics of the test structures with different P-well width. Low leakage current and V_{BD} around 2 kV is demonstrated. Based on these results, we can conclude that we successfully fabricated the designed structure and achieved the target blocking voltage.

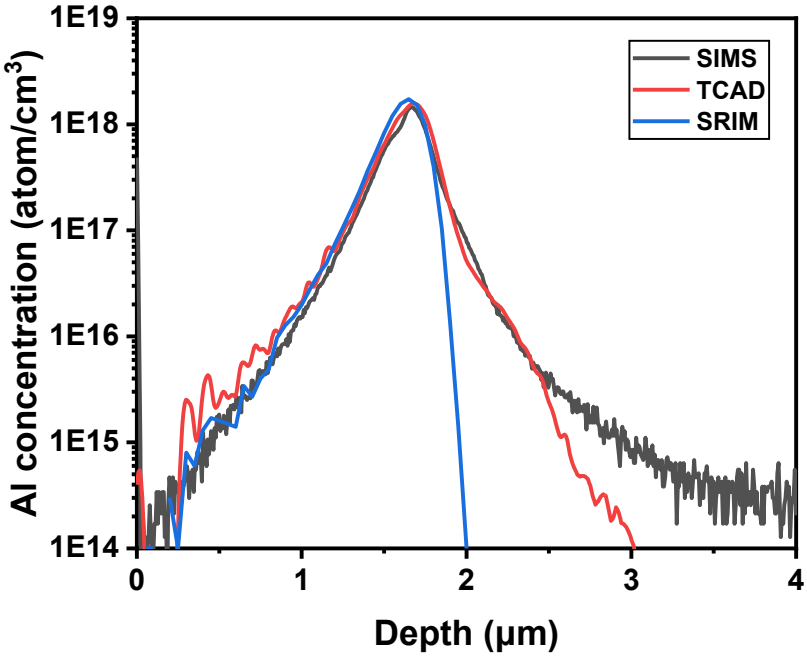

Fig. 11 The Al concentration profiles for the P-bottom, including SIMS, TCAD simulation, and SRIM simulation.

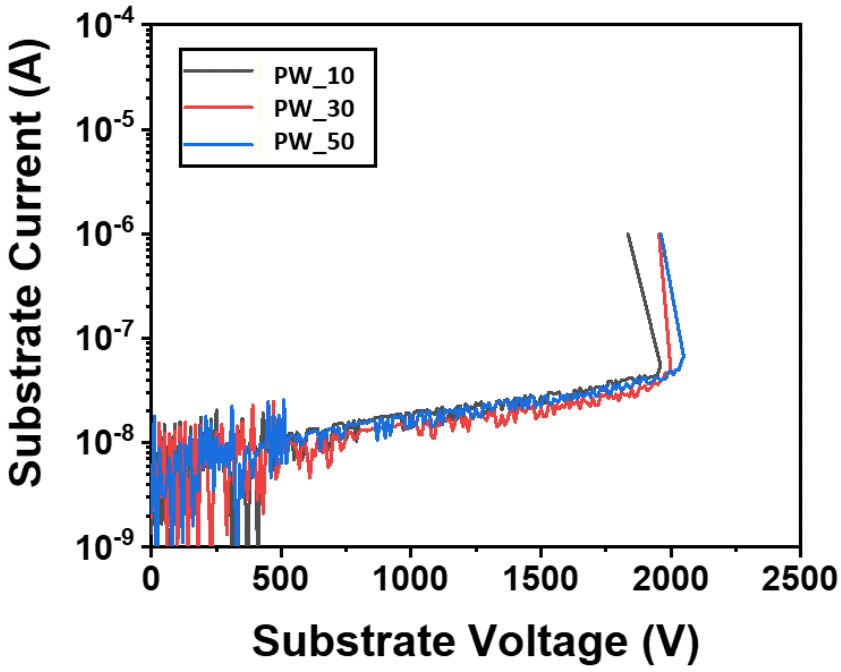

Fig. 12 Measured blocking characterstics of the 1.7 kV P-iso test structure with P-well width of 10, 30, and 50 μm.

Summary

A P-iso structure for monolithic integration of planar CMOS and 1.7 kV VDMOSFET on 4H-SiC formed by high energy ion implantation is studied. Design parameters are evaluated by TCAD simulation. The better process condition is then verified by actual test structures. A 2 kV blocking capability is achieved. It is believed that the high energy ion implantation method has the potential to be used in isolation above 1.7 kV.

Acknowledgements

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