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Impact of Interfacial SiO_2 Layer Thickness on the Electrical Performance of SiO_2/High-k Stacks on 4H-SiC

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Abstract. This study investigates the role of the electrical failure of the SiO_2 film in the breakdown of SiO_2/ZrO_2 and SiO_2/HfO_2 stacks. Our findings indicate that the breakdown is governed by the SiO_2 film, regardless of its thickness. This highlights the importance of carefully considering the interfacial SiO_2 layer when using high-k materials in SiC devices. We demonstrate that thicker SiO_2 layers offer several benefits, including reduced leakage, enhanced thermal stability and electrical strength, and decreased trapping. In contrast, stacks with thinner SiO_2 have a higher effective k value, exploiting the benefits of high-k dielectrics. Our experimental results suggest that a 7 nm SiO_2 layer underlying 30 nm crystalline ZrO_2 or HfO_2 provides optimal performance. Furthermore, we present calculations that reveal the trade-off between SiO_2 thickness, k value, and breakdown voltage for a 50 nm thick dielectric stack. Our results imply that a k value exceeding 20 does not yield significant benefits in 50 nm thick SiO_2/dielectric stacks.

Introduction

The use of SiO_2 (dielectric constant k = 3.9) as a gate dielectric has become a limiting factor in the development of high-performance silicon carbide (SiC) power devices. It is widely recognized that replacing SiO_2 with high-k dielctrics can overcome these limitations and offer new opportunities for device optimization [1]. However, the SiC/oxide interface poses a significant challenge. The lattice mismatch between the crystalline dielectric and the SiC substrate is a common issue for most high-k oxides [1], [2], [3]. Furthermore, the natural growth of carbon-rich SiO_2 on SiC during the deposition or annealing of the high-k oxide is unavoidable [4]. Both effects can lead to interface defects, which can significantly deteriorate the device performance [1], [5].

To address the challenges associated with the SiC/oxide interface, numerous studies have demonstrated the benefits of intentionally adding a high-quality interfacial SiO_2 film. This interlayer provides several advantages, including a low density of interface states (D_{it}) [6], high channel mobility [7], smooth interface morphology [8], low trap density in the bulk of the SiO_2 film [1], [9] and low frequency dispersion [6]. Additionally, the SiO_2 interlayer provides a high band offset towards the conduction/valence band (E_C/E_V) of SiC [3], which positively impacts the leakage current [9], [10] and flatband voltage V_{FB} [10]. However, the SiO_2 film reduces the effective k value of the stack [4], which undermines the benefits of introducing high-k dielectrics. To our knowledge, there is a lack of comprehensive studies that explore a wide range of SiO_2 interlayer thicknesses and consider parameters relevant to power devices. Therefore, a conclusion still needs to be drawn regarding the optimal compromise for the interfacial SiO_2 layer thickness. This study aims to bridge this gap by systematically investigating the implications of different SiO_2 thicknesses on power device performance.

Experimental

This study investigates the behavior of MOS capacitors with SiO_2/high-k stacks on n-type 4H-SiC substrates. Hafnium oxide (HfO_2) or zirconium oxide (ZrO_2) films with a target thickness of 30 nm were deposited by atomic layer deposition (ALD) on top of SiO_2 films with thicknesses ranging from 2 to 45 nm (Fig. 1a). The ALD deposition was done at 250°C with O_3 as oxidant and a tris(dimethylamino)-cyclopentadienyl-Zirconium-(C_5H_5)-Z[$N(CH_3)_2$]$_3$ precursor for ZrO_2 and a tris(dimethylamino)cyclopentadienyl-hafnium-Hf(C_5H_5)($N(CH_3)_2$)$_3$ precursor for HfO_2. Both HfO_2 and ZrO_2 are promising materials for high-k dielectric films [1], [2], [8], [12]. The SiO_2 films were deposited and subsequently nitrided to ensure high quality interfaces meeting cutting-edge industry standards. A titanium nitride / titanium / platinum stack was deposited as the top electrode. Following deposition, the samples were annealed in Argon ambient at 500°C for 1 minute, resulting in crystallization of the high-k layer (Fig. 1b, c). The layer thicknesses were determined using X-ray reflectometry (XRR) and verified by transmission electron microscopy (TEM). The crystallographic phase of the high-k films was determined from the peak positions in grazing incidence X-ray diffraction measurements (GIXRD). The k value was calculated from the MOS capacitance in the accumulation regime, representing an "effective" k that accounts for the entire dielectric stack, including SiO_2 and the high-k layer. The k value of the high-k film was calculated using an equivalent circuit model consisting of two capacitors in series, the measured layer thicknesses, and the k value of SiO_2. The leakage current density J_{leak} and the electric breakdown field E_{BD} were determined using current-voltage (IV) measurements. A positive voltage was applied to the top electrode to induce accumulation in the metal / insulator / SiC structure. The E_{BD} was defined at a J_{leak} of 10 mA/cm^2.

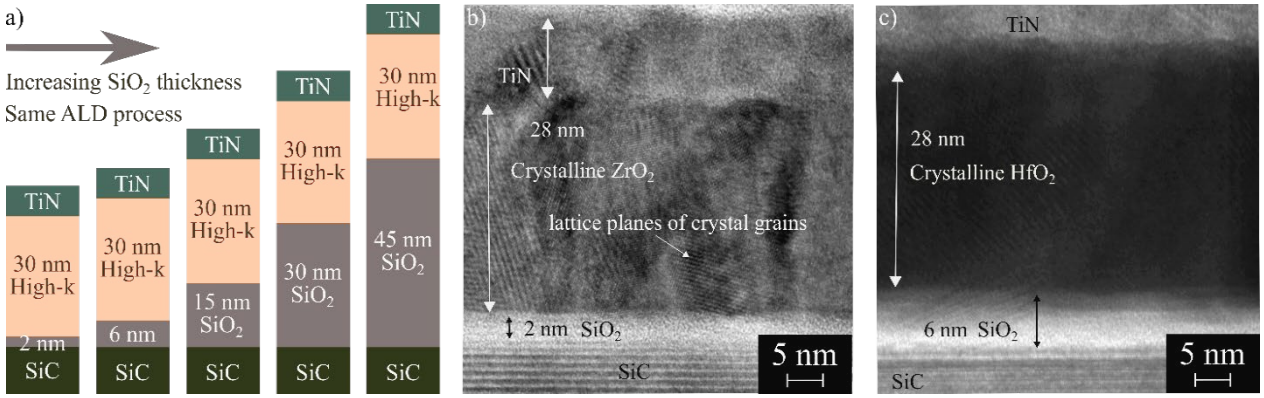

Fig. 1. (a) Schematic representation of the investigated samples. TEM image of a sample with (b) 2 nm SiO_2 and ca. 30 nm ZrO_2 and (c) ca. 6 nm SiO_2 and ca. 30 nm HfO_2, revealing the lattice planes of the crystal grains.

Results

Stacked capacitors with thicker SiO_2 layers demonstrate a higher E_{BD} and lower k (Fig. 2a), which is attributed to the higher breakdown strength and lower k of SiO_2. In contrast, capacitors with pure SiO_2 follow the opposite trend because thinner oxide films generally exhibit a higher E_{BD}. The latter was measured on reference capacitors with SiO_2 film only and aligns well with literature values (Fig. 2a) [13]. For the samples with thin SiO_2 layers, the ZrO_2 stacks exhibit a higher E_{BD} than the HfO_2 samples. This can be explained by the more suitable band alignment for ZrO_2 on SiC [1]: although HfO_2 and ZrO_2 have a similar bandgap of 5.7 eV and 5.6 eV, respectively, the conduction band offset between ZrO_2 and SiC is 1.8 eV, which is larger than between HfO_2 and SiC (0.7 eV) [1]. However, for the samples with thicker SiO_2, the physical distance between the semiconductor and the high-k oxide reduces this effect. As a result, the breakdown of the SiO_2 plays a more significant role: the higher k value of the tetragonal crystalline ZrO_2 (k~30) [1], [8] compared to the monoclinic crystalline HfO_2 (k~20) [1], [14] leads to a higher electric field within the SiO_2 film at the same applied voltage. Consequently, the critical breakdown field within the SiO_2 film is reached at lower voltages for the ZrO_2 stacks, resulting in a lower E_{BD}.

The breakdown of the SiO_2 film plays a crucial role in the breakdown behavior of the dielectric stack, as illustrated in Figure 2b: the IV curves reach the breakdown condition when the electric field within the SiO_2 film (E_{SiO2}) reaches the SiO_2 breakdown values presented in Fig. 2a [13]. This observation leads to the conclusion that the SiO_2 breakdown governs the breakdown of the stacked dielectric film. A slight deviation towards higher fields can be attributed to the omission of the contribution of the surface potential [15] and the shift in V_{FB} (cf. Fig. 4). E_{SiO2} was calculated using eq. (7) in [15]

$$E_{SiO2} = \frac{V_{Gate}-V_{FB}}{t_{SiO2}} \frac{C_{high-k}}{C_{high-k}+C_{SiO2}} = \frac{V_{Gate}-V_{FB}}{t_{SiO2}} \frac{k_{high-k}/t_{high-k}}{k_{high-k}/t_{high-k}+ k_{SiO2}/t_{SiO2}}, \quad (1)$$

with V_{Gate} as the applied voltage, $k_{SiO2} = 3.9$, and the V_{FB} determined from capacitance-voltage (CV) measurements.

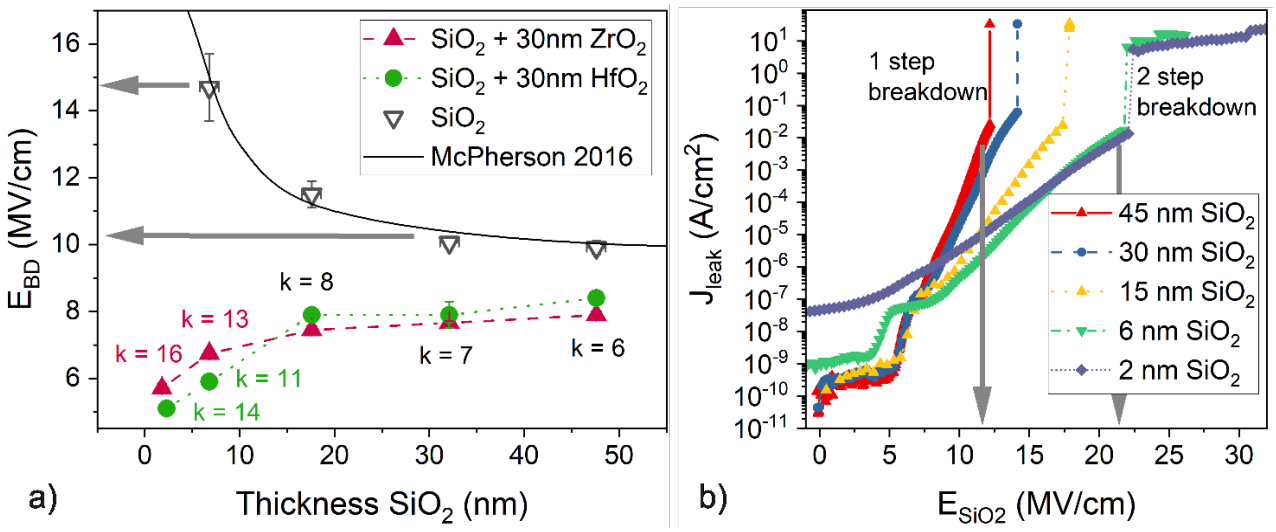

Fig. 2. (a) Electric breakdown field E_{BD} of SiO_2 and stacks of SiO_2 and high-k dielectric. (b) J_{leak} of the SiO_2 and ZrO_2 stacks versus the electric field within the SiO_2 film.

The exact breakdown mechanism has been described in detail by Kumta et al. [16]. Our samples exhibit a similar behavior: after the SiO_2 film breakdown, the entire applied voltage drops across the remaining high-k layer. For stacks with thick SiO_2 films, this leads to an immediate breakdown of the stack (1-step breakdown). In contrast, samples with thin SiO_2 reach the breakdown limit in SiO_2 at lower applied voltages. The high-k oxide remains intact, exhibiting a high leakage current, and breaks down subsequently (2-step breakdown). This phenomenon was validated by measuring a monitor current during the dielectric relaxation of the internal polarization within the high-k dielectric [16], i.e., at 0V applied. The procedure is illustrated in the inset of Fig. 3a. When the externally applied field is removed, a decaying current in the opposite direction to the leakage current can be measured. This relaxation current (J_{relax}) stems from free hopping charges that neutralize the internal bound charges that previously caused the polarization of the dielectric. Notably, J_{relax} is negligible for SiO_2 but can be detected in HfO_2 and ZrO_2 until the dielectric undergoes a breakdown [16]. The leakage curve and the corresponding monitor current in Fig.3a clearly demonstrate the 2-step breakdown of the stack with 2 nm SiO_2 and HfO_2.

For a more comprehensive understanding of the breakdown phenomena of the stacks, I-V measurements were carried out at elevated temperatures (exemplary data for ZrO_2 stacks shown in Fig. 3b). For the stacks with thin SiO_2 film, the primary conduction mechanism is trap-assisted tunneling with a significant temperature dependence [17]. At 200°C, the E_{BD} is reduced by 40% compared to the measurements at 25°C, and the J_{leak} at 2 MV/cm is increased by four orders of magnitude. For the sample with 45 nm SiO_2, Fowler-Nordheim tunneling is the predominant mechanism, which shows much less temperature dependence [17]. For measurements performed at 200°C, J_{leak} at 2 MV/cm remains within the detection limit, and E_{BD} is reduced by only 11% as

compared to measurements at 25°C. The reduction of E_{BD} can be attributed to the temperature-dependent Fermi-Dirac distribution of the electrons, which translates to an increased availability of electrons for tunneling at higher temperatures.

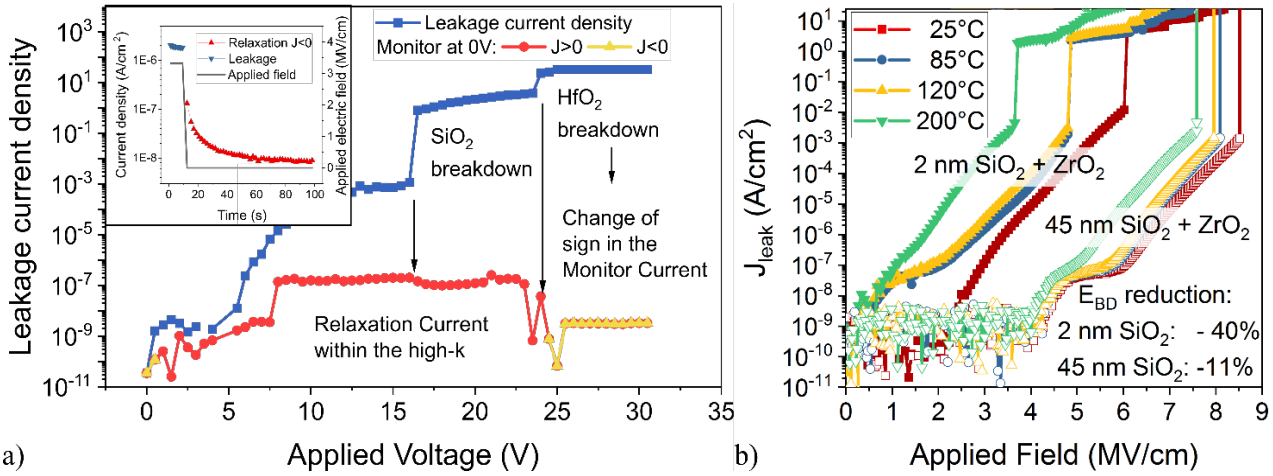

Fig. 3. (a) Leakage and relaxation current in the stack of 2 nm SiO_2 and HfO_2. The relaxation current was measured after a 1 s delay time. The inset displays the presence of the relaxation current over time. (b) J-E plot for the sample with 2 nm SiO_2 and 45 nm SiO_2 measured at temperatures between 25°C and 200°C.

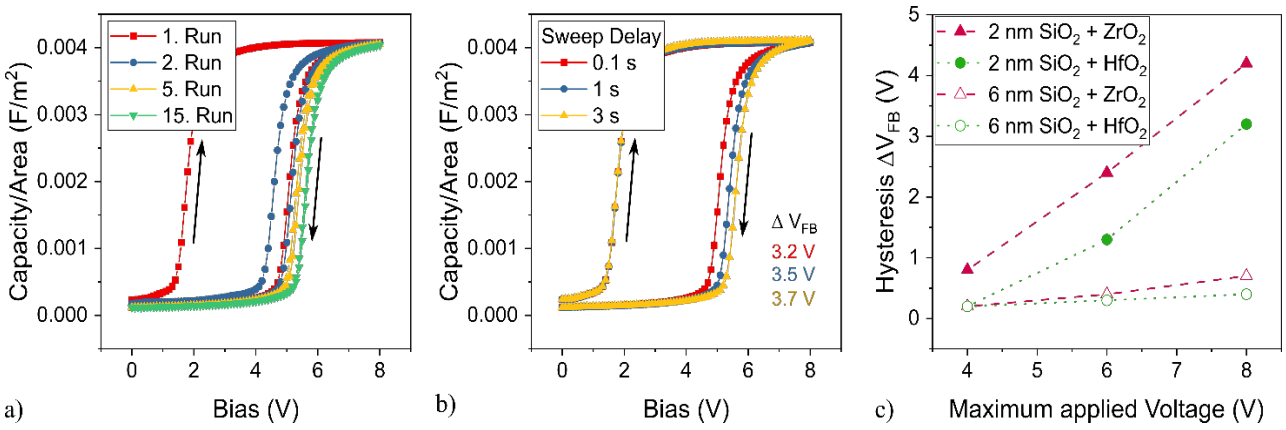

Fig. 4. (a) Consecutive CV measurements of the sample with 2 nm SiO_2 with HfO_2. (b) Several CV measurements with different sweep delays, i.e., the time intervals between voltage application and capacitance measurement (2 nm SiO_2 with HfO_2). (c) Hysteresis of the first CV sweep for samples with 2 and 6 nm SiO_2, depending on the maximum applied bias.

CV measurements were performed to determine the k-value and trapping behavior of the stacks. Stacks with thin SiO_2 exhibit a significant hysteresis between the up-sweep and down-sweep curves (Fig. 4), indicating that electrons from the SiC accumulation layer are trapped at the SiO_2/high-k interface or within the high-k [5]. With every subsequent measurement, the CV curve shifts towards higher voltages, resulting in a higher V_{FB} and smaller hysteresis (Fig. 4a). This implies that trapped electrons are not released during the down-sweep [18]. The shift saturates after a certain number of measurements, indicating that all accessible traps are filled after a specific time.

The hysteresis is found to increase under two conditions i) when the sweep delay of the measurement is increased (Fig. 4b), and ii) when the maximum applied bias is increased (Fig. 4c). The sweep delay refers to the time interval between applying the bias and measuring the corresponding capacitance. At slower sweep rates, the electrons have more time to fill so-called "slow" traps. At higher maximum bias, the electrons possess more energy and can access traps, which are energetically not accessible at lower fields. Both effects lead to an increase in the number of trapped charges, resulting in a larger hysteresis.

The shift of V_{FB} was evaluated over several measurement runs in Fig. 5a. The figure shows the saturation effect mentioned earlier and the difference in behavior for different SiO_2 thicknesses. Notably, the charge trapping is more pronounced in films with thin SiO_2. In contrast, a thicker SiO_2 film acts as both a physical and an electrical barrier, inhibiting electrons from tunneling towards the high-k oxide [4]. Fig. 5b shows the decline of the hysteresis for thicker SiO_2 films. The hysteresis was measured during the first measurement run. The maximum applied voltage was adjusted to ensure the same field (2.7 MV/cm) for all samples, i.e., 8 V for the sample with 2 nm SiO_2 and 20 V for the sample with 45 nm SiO_2. Fig. 5c shows the decline of the V_{FB}, measured at the first up-sweep, for samples with thicker SiO_2. The ideal V_{FB}, i.e., in complete absence of any trapped, fixed, or mobile charges within the dielectric, depends only on the work function of the electrode metal and the electron affinity of the semiconductor. In our case, for SiC and TiN, it has a value of 1.0 V [19]. Predominantly, the trapped and fixed charges located in the oxide and at the interfaces shift V_{FB}. Negative charges trapped in the dielectric shift V_{FB} towards higher positive voltages. With thicker interfacial SiO_2, the trapped charges within the high-k material are further away from the SiC surface which weakens their influence on the voltage shift [5]. Moreover, the shift of V_{FB} towards negative values is associated with an accumulation of positive charges within the SiO_2 [11]. The more negative V_{FB} with thicker SiO_2 could be explained by positive fixed charges in the SiO_2. The difference between the HfO_2 and ZrO_2 series indicates a corresponding difference in fixed charges within the bulk of the high-k or at the high-k/SiO_2 interface.

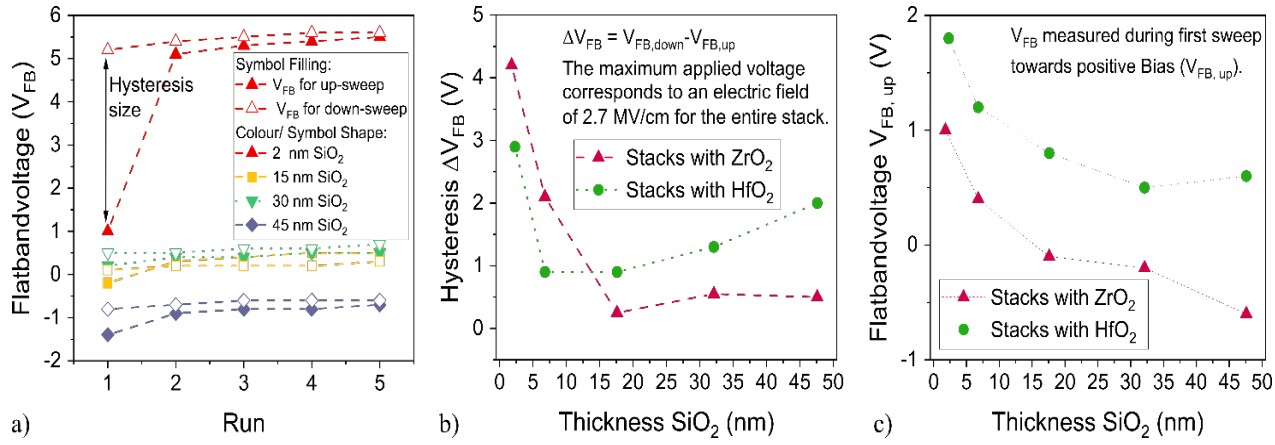

Fig. 5. (a) Flatband voltage V_{FB} of consecutive CV runs. (b) CV hysteresis versus SiO_2 thickness. (c) V_{FB} of the first up-sweep in CV measurements versus the SiO_2 thickness of the sample. For all measurements, the maximum applied bias was 2.7 MV/cm, i.e., the maximum voltage was adjusted according to the stack thickness.

These results highlight the importance of carefully designing the thickness ratio of the SiO_2 and high-k films for a particular application. Therefore, field calculations are presented in Fig. 6. A stack with a total thickness of 50 nm, consisting of a SiO_2 film and a high-k film, was assumed. The thickness of the SiO_2 layer varied from 0 to 50 nm, resulting in the SiO_2 fraction in the stack ranging from 0% to 100%. The k value of the high-k material was varied from 0 to 40. The electric fields within the two dielectric films at a specific applied voltage V_{Gate} were calculated by using eq. (1). The breakdown condition of the stack is reached when the field within the SiO_2 film surpasses the breakdown limit of SiO_2 as presented in [13] and confirmed in Fig. 2a. In both plots, Fig. 6a and b, the curves resemble the breakdown condition for the SiO_2 film, i.e., the voltage at which the field within the SiO_2 film exceeds the breakdown limit. Several effects determine the shape of the curves in both plots: i) a high k value of the high-k oxide, i.e., a strong polarization, pushes the electric field towards the SiO_2, ii) for a given k value and applied voltage, the electric field in the SiO_2 is lower for a thicker film than for a thin film, iii) thinner films exhibit a higher breakdown field. The last two effects are contrary and lead to the crossing of the curves in Fig. 6a. In this plot, each line shows the expected breakdown voltage for a particular stack combination. The crossing occurs at a range of k values between 12 and 20, revealing that in that range, the variation of SiO_2 thickness between 2

and 10 nm has only a small influence on the breakdown voltage. Hence, the favored SiO_2 thickness is as small as possible to maintain a high effective k value. At higher k values, the polarization of the high-k material is so strong that the electric field reached within the SiO_2 film is exceedingly high. Therefore, the E_{SiO2} must be reduced by increasing the SiO_2 film thickness.

Fig. 6b provides further guidance for the stack composition: To withstand a specified voltage, the stack must be designed in such a way that the combination of its SiO_2 thickness and k value lies above the curve. The area below the curve represents all stack combinations where the electric field within the SiO_2 exceeds the breakdown limit. The background of the graph area visualizes the overall k value of the specific stack combination calculated from the thicknesses and k values by using

$$k_{\text{stack}} = \frac{t_{\text{stack}}}{\frac{t_{\text{high-k}}}{k_{\text{high-k}}} + \frac{t_{\text{SiO2}}}{k_{\text{SiO2}}}}. \quad (2)$$

Both plots suggest that using high-k materials with k > 20 in a stack with SiO_2 is not beneficial. This is because either the breakdown voltage is very low or the SiO_2 thickness has to be increased significantly. This, in turn, reduces the effective k value of the stack (k_{stack}), which negates the effort of increasing the k value of the oxide stack.

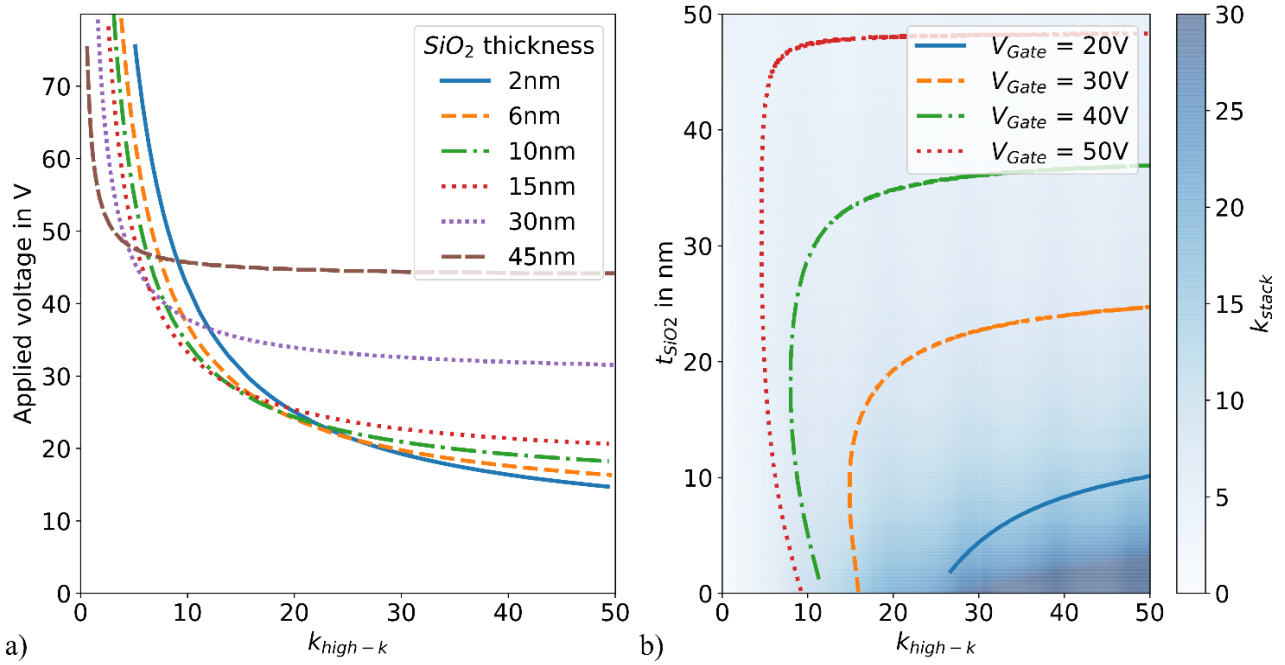

Fig. 6. Theoretical field calculation for capacitors with SiO_2/high-k oxide stacks with t_{SiO2} as the SiO_2 film thickness, k_{high-k} as the k value of the high-k oxide, and V_{Gate} as the voltage applied to the entire stack, and flatband voltage V_{FB} = 2V. The total stack thickness is constant at 50 nm. (a) The curves represent the breakdown voltage for a stack consisting of a SiO_2 film with the specified thickness and a high-k dielectric with the specified k value. (b) The background color displays the effective k value of the stack. The curves represent the breakdown condition of the SiO_2 film: in stacks that appear below the curve the E_{SiO2} at the specified voltage is higher than the breakdown field of SiO_2 resulting in a breakdown of the stack.

Discussion

This study demonstrates that in SiO_2/ZrO_2 and SiO_2/HfO_2 stacks, the SiO_2 film breaks down first, independent of its thickness. The electrical failure of the SiO_2 film leads to a significant increase in the leakage current and, ultimately, to the breakdown of the stack. With thicker SiO_2, the Fowler-Nordheim mechanism dominates the carrier conduction, enabling low leakage and high breakdown field at 200°C. However, thick SiO_2 significantly reduces the effective k value of the stack. For a final decision about the most suitable trade-off, Fig. 7 compares the relevant parameters for all the

investigated SiO_2 thicknesses. The samples with 7 nm (green area) provide the best compromise between all parameters, including a comparatively high k value. Therefore, we conclude that 7 nm of interfacial SiO_2 below 30 nm of crystalline ZrO_2 or HfO_2 offers the best trade-off. For these stacks, the dielectric constant remains high, at 13 for the ZrO_2 stack and 11 for the HfO_2 stack. The hysteresis at an applied bias of 2.7 MV/cm is reduced by 50% for the ZrO_2 and 60% for the HfO_2 samples compared to the stack with 2 nm. The average breakdown fields of the entire stack are 6.7 MV/cm and 6 MV/cm, respectively, which is reasonably high. The leakage current density at 2 MV/cm for the ZrO_2 stacks is $6.6 \cdot 10^{-9}$ A/cm^2 and $3.7 \cdot 10^{-10}$ A/cm^2 for the HfO_2 stacks. This is well below the leakage limit of 100 nA/cm^2 widely accepted in literature [20].

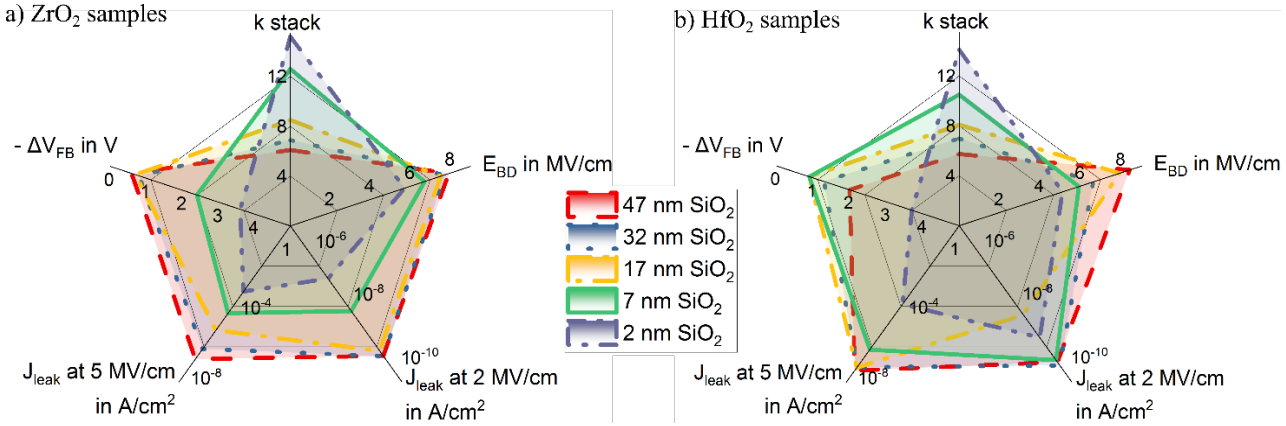

Fig. 7. Comparison of (a) ZrO_2 and (b) HfO_2 samples with all 5 investigated SiO_2 thickness values. For clarity, the graph axes are defined such that the least favorable values are centralized. The desired metrics, e.g., high E_{BD} and low J_{leak}, are furthest away from the center. Consequently, a larger area encompassed by a sample indicates a more suitable performance.

Conclusion

The results highlight the importance of thoughtfully designing the thickness ratios of the SiO_2 and high-k films in dielectric stacks. Theoretical calculations of the electric fields in a 50 nm stack indicate that the k value of the high-k material should be lower than 20 to avoid early breakdown due to SiO_2 breakdown.

Acknowledgments

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References

[1] A. Siddiqui, R. Y. Khosa, and M. Usman, “High-k dielectrics for 4H-silicon carbide: present status and future perspectives,” *J. Mater. Chem. C*, vol. 9, no. 15, Art. no. 15, 2021.

[2] M. Nawaz, “On the Evaluation of Gate Dielectrics for 4H-SiC Based Power MOSFETs,” *Active and Passive Electronic Components*, vol. 2015, pp. 1–12, Dec. 2015.

[3] J. Robertson, “Band offsets of wide-band-gap oxides and implications for future electronic devices,” *J. Vac. Sci. Technol. B*, vol. 18, no. 3, Art. no. 3, 2000.

[4] J. Robertson, “High dielectric constant oxides,” *Eur. Phys. J. Appl. Phys.*, vol. 28, no. 3, pp. 265–291, Dec. 2004.

[5] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*, Third edition. Hoboken, NJ: Wiley-Interscience, 2007.

[6] C.-M. Hsu and J.-G. Hwu, “Investigation of carbon interstitials with varied SiO2 thickness in HfO2/SiO2/4H-SiC structure,” *Applied Physics Letters*, vol. 101, no. 25, p. 253517, Dec. 2012.

[7] J. Urresti, F. Arith, S. Olsen, N. Wright, and A. O’Neill, “Design and Analysis of High Mobility Enhancement-Mode 4H-SiC MOSFETs Using a Thin-SiO_2/Al_2O_3 Gate-Stack,” *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 1710–1716, Apr. 2019.

[1] A. Siddiqui, R. Y. Khosa, and M. Usman, “High-k dielectrics for 4H-silicon carbide: present status and future perspectives,” *J. Mater. Chem. C*, vol. 9, no. 15, Art. no. 15, 2021.

[2] M. Nawaz, “On the Evaluation of Gate Dielectrics for 4H-SiC Based Power MOSFETs,” *Active and Passive Electronic Components*, vol. 2015, pp. 1–12, Dec. 2015.

[3] J. Robertson, “Band offsets of wide-band-gap oxides and implications for future electronic devices,” *J. Vac. Sci. Technol. B*, vol. 18, no. 3, Art. no. 3, 2000.

[4] J. Robertson, “High dielectric constant oxides,” *Eur. Phys. J. Appl. Phys.*, vol. 28, no. 3, pp. 265–291, Dec. 2004.

[5] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*, Third edition. Hoboken, NJ: Wiley-Interscience, 2007.

[6] C.-M. Hsu and J.-G. Hwu, “Investigation of carbon interstitials with varied SiO2 thickness in HfO2/SiO2/4H-SiC structure,” *Applied Physics Letters*, vol. 101, no. 25, p. 253517, Dec. 2012.

[7] J. Urresti, F. Arith, S. Olsen, N. Wright, and A. O’Neill, “Design and Analysis of High Mobility Enhancement-Mode 4H-SiC MOSFETs Using a Thin-SiO_2/Al_2O_3 Gate-Stack,” *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 1710–1716, Apr. 2019.

[8] M. Gutowski *et al.*, “Thermodynamic stability of high- *K* dielectric metal oxides ZrO2 and HfO2 in contact with Si and SiO2,” *Applied Physics Letters*, vol. 80, no. 11, Art. no. 11, Mar. 2002.

[9] K. Y. Cheong, J. H. Moon, D. Eom, H. J. Kim, W. Bahng, and N.-K. Kim, “Electronic Properties of Atomic-Layer-Deposited Al_2O_3 Thermal-Nitrided SiO_2Stacking Dielectric on 4H SiC,” *Electrochem. Solid-State Lett.*, vol. 10, no. 2, p. H69, 2007.

[10] R. Mahapatra, A. K. Chakraborty, A. B. Horsfall, N. G. Wright, G. Beamson, and K. S. Coleman, “Energy-band alignment of HfO2⁄SiO2⁄SiC gate dielectric stack,” *Applied Physics Letters*, vol. 92, no. 4, p. 042904, Jan. 2008.

[11] K. Iwamoto *et al.*, “Experimental evidence for the flatband voltage shift of high-k metal-oxide-semiconductor devices due to the dipole formation at the high-k⁄SiO2 interface,” *Applied Physics Letters*, vol. 92, no. 13, p. 132907, Mar. 2008, doi: 10.1063/1.2904650.

[12] S. Krause, T. Mikolajick, and U. Schroeder, “Improving HfO_2 Thick Films for SiC Power Devices by Si, Y and La Doping,” *SSP*, vol. 359, pp. 29–34, Aug. 2024.

[13] J. W. McPherson, “Increases in Lorentz Factor with Dielectric Thickness,” *WJCMP*, vol. 06, no. 02, pp. 152–168, 2016.

[14] C. Richter *et al.*, “Si Doped Hafnium Oxide—A ‘Fragile’ Ferroelectric System,” *Adv. Electron. Mater.*, vol. 3, no. 10, Art. no. 10, Oct. 2017.

[15] R. G. Southwick, J. Reed, C. Buu, R. Butler, G. Bersuker, and W. B. Knowlton, “Limitations of Poole–Frenkel Conduction in Bilayer HfO_2/SiO_2 MOS Devices,” *IEEE Trans. Device Mater. Relib.*, vol. 10, no. 2, Art. no. 2, Jun. 2010.

[16] A. Kumta, Rusli, and J. H. Xia, “Breakdown phenomena of Al-based high-k dielectric/SiO2 stack on 4H-SiC,” *Applied Physics Letters*, vol. 94, no. 23, p. 233505, Jun. 2009.

[17] A. Paskaleva, D. Spassov, and D. Dankovic, “Consideration of conduction mechanisms in high-k dielectric stacks as a tool to study electrically active defects,” *Facta Univ Electron Energ*, vol. 30, no. 4, Art. no. 4, 2017.

[18] A. Vasilev *et al.*, “Oxide and Interface Defect Analysis of lateral 4H-SiC MOSFETs through CV Characterization and TCAD Simulations,” *MSF*, vol. 1090, pp. 119–126, May 2023.

[19] R. G. Southwick and W. B. Knowlton, “Stacked Dual-Oxide MOS Energy Band Diagram Visual Representation Program (IRW Student Paper),” *IEEE Trans. Device Mater. Relib.*, vol. 6, no. 2, pp. 136–145, Jun. 2006.

[20] J. Weckbrodt, N. Ginot, C. Batard, and S. Azzopardi, “Monitoring of Gate Leakage Current on SiC Power MOSFETs: An Estimation Method for Smart Gate Drivers,” *IEEE Trans. Power Electron.*, vol. 36, no. 8, Art. no. 8, Aug. 2021.