Materials Science Forum
ISSN: 1662-9752, Vol. 1158, pp 33-40
doi:10.4028/p-7Bd8tb

Submitted: 2024-09-11
Revised: 2025-08-19
Accepted: 2025-08-19
Online: 2025-09-08

Rapid Thermal Anneal with Conductive Heating for SiC Contact Formation

Xavier Pagès[*1,a], Simon van der Linde[1,b], Jeppe Oterdoom[1,c], Mark Steltenpool[1,d], Vladimir Kuznetsov[1,e], Jaap Beijersbergen[1,f], Mickael Sanchez[2,g], Sebastien Kerdiles[2,h]

[1]Levitech b.v; Neonweg 42; 1362AE Almere, The Netherlands

[2]Université Grenoble Alpes, CEA-LETI, Grenoble, France

[a]xavier.pages@levitech.nl, simon.van.der.linde@levitech.nl, jeppe.oterdoom@levitech.nl; mark.steltenpool@levitech.nl; Vladimir.kuznetsov@levitech.nl; jaap.beijersbergen@levitech.nl; mickael.sanchez@cea.fr; sebastien.kerdiles@cea.fr

Keywords: Silicide top contact; rapid thermal anneal (RTA), conductive heating

Abstract: This paper explains the potential of a heat conduction based RTA (Rapid Thermal Anneal) system (Levo) to overcome the main shortcomings of conventional lamp heated tools systems for silicide top contact anneal during SiC MOSFET device fabrication. The advantage of conductive heating is that the radiation-related properties, like transparency of the wafer, does not play a role, and consequently, that the whole rapid thermal anneal becomes independent of wafer type. In this study SiC wafers and Si wafers (both 200mm) were annealed consecutively without any system adjustment. The silicon wafers were used to qualify the process (contamination / within-wafer uniformity and wafer-to-wafer repeatability).

Introduction

SiC crystal is today one of the most promising semiconductor material for next-generation of high-temperature and high frequency electronic devices applications [1]. It has a wide band gap (3.3 eV), a high breakdown field of (3×10^6 V/cm; 10 times higher than Silicon), a high thermal conductivity (5 W/cm K), a high thermal stability [2] and a very high carrier mobility and electron saturation drift velocity (2.7×10^7 cm/s). As a matter of fact, enormous progress has been recorded in 4H-SiC power devices like Metal Oxide Semiconductor Field Effect Transistor (MOSFET) over the last decade [4–6].

Today the fabrication of vertical silicon carbide (SiC) MOSFET devices (DMOS and UMOS) involves multiple annealing steps along the process flow. It is interesting to note that the techniques used to anneal SiC wafers differ greatly depending on the progress in the manufacturing process.

First, the formation of the doped areas (p channel / n+ source / etch termination) requires post implantation annealing process at high temperature (typically between 1700 °C and 2100 °C). This step is typically performed in batch furnaces for several minutes. These long anneals are possible because the diffusion coefficients of dopant in the SiC wafer remains extremely low, even at very high annealing temperatures (above 1500 °C) [7]. Nevertheless, two challenges are usually associated with the annealing of ion implanted areas. First, the generation of crystal structure damages that, for high-dose implantation, can lead to amorphization of the material. This effect will be reduced if implantation is performed at high temperature (typically around 500 °C). Second, the requested high temperature annealing of 1600 °C or higher, causes Si evaporation and surface roughness. This surface degradation process is avoided by depositing a dense carbon film by sputtering prior to activation anneal. Because of the two above mentioned issues, both source and base regions can sometimes be formed epitaxially (UMOSFET) which enable the fabrication process free of ion-implantation and the associated high-temperature annealing, preventing therefore the device from surface degradation.

Second, the formation of the top contact (silicided based) which is typically done with lamp-based RTA (Rapid Thermal Anneal) systems. A common technique to form contacts on SiC is to deposit a suitable metal in a heavily doped n- or p-type region, followed by post-deposition anneal typically at 900 – 1000 °C. The most promising material is nickel (Ni) for n-type regions and aluminum-titanium (Al-Ti) for p-type region. SiC devices need contacts with a contact resistance (ρ_C) in the range of 10^{-6} Ωcm^2 or lower [13]. The ρ_C strongly depends on the contact material, the doping level, and annealing conditions. The main challenge lamp RTA systems face when processing transparent SiC wafers is to meet the temperature control requirements, which originate from the fact that SiC wafers are transparent to IR radiation and must be inserted into graphite boxes. This complicates wafer temperature measurement, making "true" RTA impossible (the thermal mass of graphite box considerably slows down wafer heat up and cooldown rates) and enhances the sensitivity to residual oxygen contamination. Other important parameters are the surface preparation before metal deposition [8, 9], surface roughness [10], organic and metal contamination [11], natural oxide formation [11] and graphitized skin [12],

Finally, the formation of the bottom contact is performed using laser annealing system after wafer backside thinning. Wafer grinding was introduced to reduce the resistive contribution of the substrate. It has been calculated that thinning the wafer thickness from 350 down to 110 μm decreases the resistive contribution down to 44% of the total RON [6]. The tunable laser energy density combined with ultrashort irradiation time allows heat accumulation at the wafer surface only. Therefore, laser annealing in back Ohmic contact formation enables the possibility to complete the device front side first, and then to process the back-side contact without detrimental effects.

In the following sections we will explain the potential of conductive based RTA system (Levo) to overcome the main shortcomings of conventional lamp heated systems for silicide top contact anneal during SiC MOSFET device fabrication. The advantage of conductive heating is that the radiation-related properties, like transparency of the wafer, does not play a role, and consequently, that the whole RTA process becomes independent of wafer type.

Theoretical Considerations

Current lamp-based systems use pyrometers and measure the substrate emissivity to monitor the heating power to control the substrate temperature during anneal. Unfortunately, this procedure does not work when, like for SiC wafers, the substrate is transparent to IR radiation or when large emissivity variations are present on the device side of the wafer. For that reason, it makes sense to consider conductive heating systems that are not sensitive to substrate type and not sensitive to variations in emissivity (Levo RTA systems).

Since the contribution of convection is very small, the general heat flux can be written like in Equation 1. The first and second terms on the right represent the heat transfer (W/m^2) from the reactor surface to the wafer from the conductive and radiative contributions, respectively. All the parameters shown in equation 1, with the exception of the emissivity ε, are bulk properties of materials and material dimensions. The heat transfer mechanism is strongly depending on the gap distance (g) between the wafer and the reactor surface. In the case of Levitech RTA systems, the gap distance (g) is typically in the range of 0.15 - 0.3 mm (depending on wafer thickness). Annealing in Levo RTA system is therefore dominated by the conduction which has strong technological advantages for processing of transparent SiC wafers.

$$\rho C d\frac{dT_w}{dt} = \underbrace{2\lambda\frac{T_{plate}-T_w}{g}}_{\text{conduction}} + \underbrace{2\varepsilon\sigma(T_{plate}^4-T_w^4)}_{\text{radiation}}$$

Equation 1: Heat flux (W/m^2) from the reactor to the wafer:. dT_w/dt is the rate at which the temperature of the wafer changes with time. The factor 2 stems from the fact that the wafer is heated from both sides.

ρ = specific density of the wafer;
C = specific heat capacity of the wafer;
d = wafer thickness;
t = time (s);
T_{plate} = temperature of the reactor (K);
T = wafer temperature;
λ = thermal conductivity of the bearing gas ($Wm^{-1}K^{-1}$),
g = gap distance between wafer and hot reactor wall
ε = emissivity of the wafer
σ = Stephan-Boltzmann constant

In figure 1, Equation 1 is solved as a function of time. In this calculation, a 200mm (500 µm thick) SiC wafer is heated from 20°C to a process temperature of 1000°C.

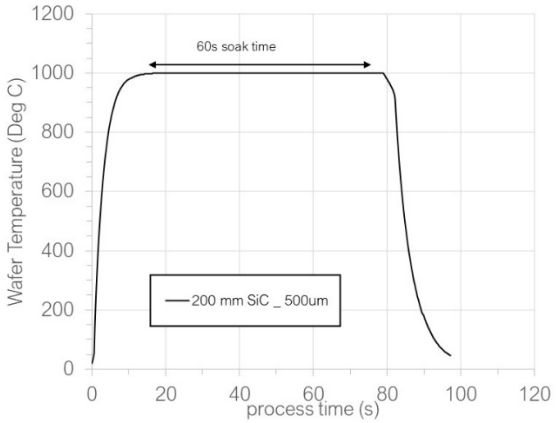

Fig.1. Heating profile of 500 µm thick SiC (200mm) with Levitor RTA system for process temperatures of 1000°C.

The SiC wafers are directly inserted inside the reactor chamber without using graphite boxes. This allows to skip the (too) long purging step prior anneal. The heating and cooling speeds are high (> 200 °C/s) (see figure 1). High heat-up and cool-down rates enable a perfect control of the silicidation process because the uncontrolled silicidation, wich is occuring during heat up (and natural cooling), of the SiC wafer is avoided. The absence of a stabilization step during heat up (in figure 1 the SiC wafer is annealed directly from room temperature to process temperature) combined with a forced cooldown guarantee a high throughput.

Experimental Setup and Discussion

In this study both 200 mm (+/- 0.5mm) SiC wafers with a thickness of 500µm (+/- 50µm) and (200 mm) Si wafers were annealed consecutively without any system adjustment with a 200mm Levo conductive RTA system at CEA Leti.

The Levo system heats the wafer by placing it in an axial gas bearing in between two heated reactor gas divider (see figure 2). Gas flowing through a radial gas bearing keeps the wafer centered in the horizontal plane. Wafer centering is achieved by building-up a pressure difference along the wafer

edge whenever the wafer is shifted out of its central position. Such construction ensures that the wafer never touches the reactor gas divider. The thin and uniform gas layer ensures very fast wafer heating through gas conduction. The wafer heat-up rate is determined by the thermal conductivity λ of the bearing gas. At a gap of 150 µm, when nitrogen is used, a heat up rate of approximately 200 – 300 °C/s is realized. (see figure 1), however when helium is used, heat-up rates up to 900 °C/s are reached. Reactive gases (NH_3 for surface Nitridation, H_2 for metal reduction or surface cleaning process) or inert gas like Argon (when nitrogen sensitive ALD layers are present on the wafer before anneal) can also be part of the gas system for Rapid Thermal Process (RTP).
After annealing in the reactor, the wafer is transferred to a cooling station by a quartz wafer carrier enclosed by a quartz guard (edge) ring. This guard ring prevents slip (crystal defects at the edge of the wafer) during transport.
In the cooling station, the same bearing principle is used as in the reactor section. Similar to the reactor section, different gases can be used as bearing gas

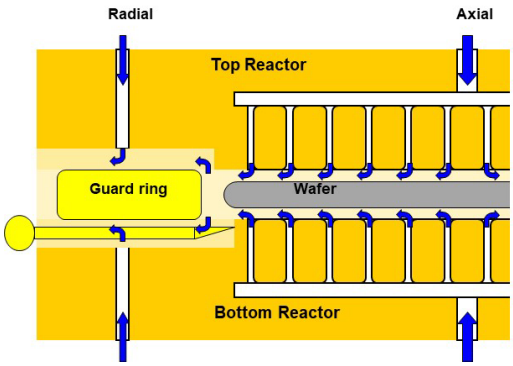

Fig. 2. Cross section of the Levitor chamber with a wafer being processed.

Figure 3 shows the 200mm SiC wafer and the 200mm Si wafer before process in the atmospheric front end of the Levitor 200 mm system. The silicon wafers were used to qualify the process.

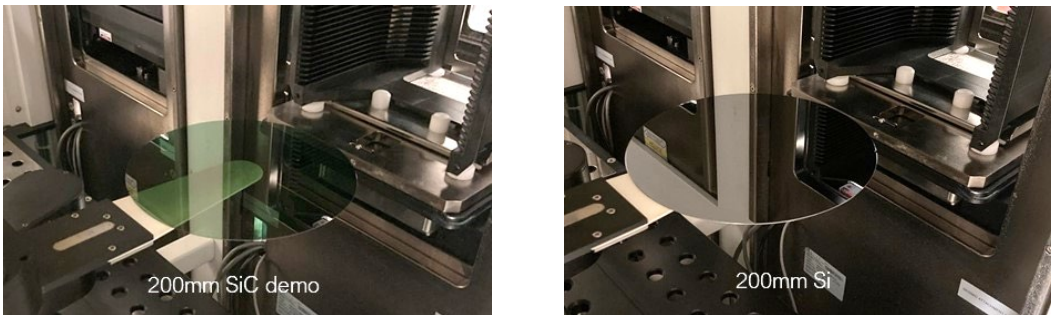

Fig. 3.

These wafers were annealed at 1000°C for 60s under nitrogen in order to get a representative Nickel silicidation process step. The associated wafer temperature transient and pressure measurement during anneal are shown in figure 4.

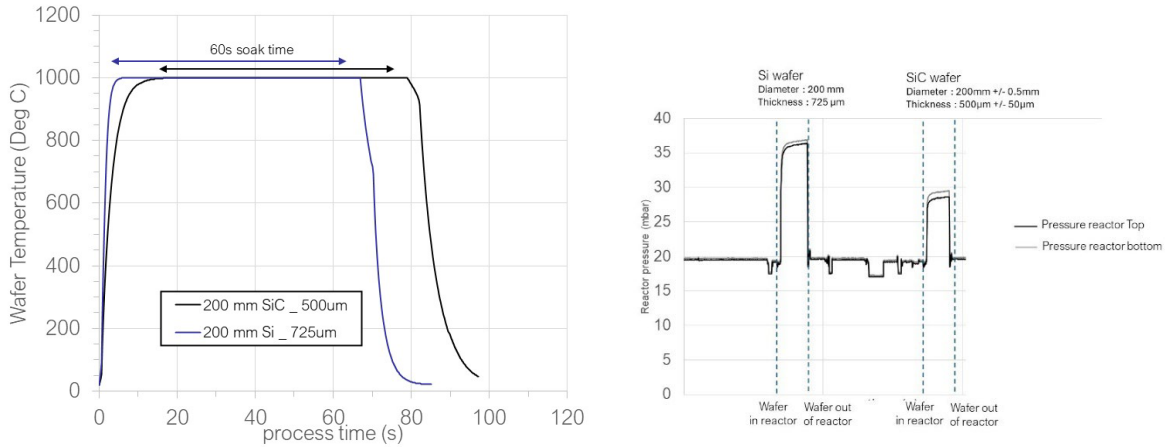

Fig. 4. left = wafer temperature transient of 200mm SiC and 200mm Si wafers annealed at 1000°C for 60s in nitrogen; right = Reactor pressure during process.

When soak anneal processes are carried out in the Levo RTA system, the wafer temperature becomes equal to that of the heating reactor gas divider within a few seconds. Because the wafer cannot exceed reactor surface temperature, temperature overshoot is physically impossible. The silicon wafer reaches the process setpoint temperature in ~6 seconds whereas the SiC wafer requires ~12 seconds to be at process temperature. This difference arises from the different specific heat capacity Cp (see equation 1) of silicon and 4H SiC crystal at high temperature (see figure 5). The wafer cooling process exhibits 2 different slopes. The first part of the cooling (right after the 60s soak process) depicts the radiative cooling of wafers during their transfer from the reactor to the cooling station. This step takes exactly 2,6s (1,6s to transfer the wafer from reactor to cooling station and 1s to close the cooling station). The slower radiative cooling rate of the SiC wafer is caused by the high heat capacity of SiC. After the cooling station is closed, a forced cooling through conduction enables fast wafer cooling and it takes less than 10s to reach temperature of lower than 70°C for wafer unloading.
The right part of figure 4 shows the partial pressure inside the reactor during process for both the 200mm silicon (first peak) and the 200mm SiC wafer (2nd peak). The difference in peak pressure results from difference in wafer thickness, the SiC wafer was only 500 µm thick whereas the Silicon wafer is 720 µm thick. The distance between the upper and lower surfaces of the reactor is fixed. Consequently, the gap distance between reactor and wafer (see figure 2) is slightly larger for the SiC wafer which results in a lower pressure build up during anneal.

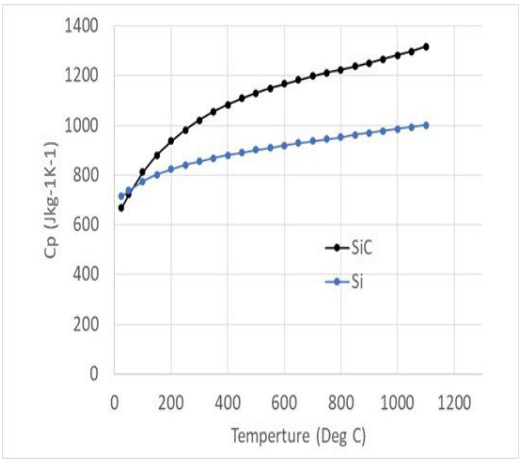

Fig. 5. Specific heat capacity Cp of silicon and 4H SiC wafer as a function of temperature

High heat-up and cooldown rates enable a perfect control of the silicidation process. The uncontrolled silicidation wich is occuring during slow heat-up (and during radiative cooling) of the SiC wafer is avoided. This is important because SiC MSOSFET silicided top contacts are generally performed

using a two step annealing process (RTA1 at ~700 ºC / selective etch to remove unreacted nickel / RTA2 at ~1000 ºC). In this two-step approach, the PVD Ni layer is deposited on the entire wafer surface and an uncontrolled RTA1 anneal will cause excessive Ni diffusion leading to undefined Ni silicide thickness after RTA1. This effect is a well known issue on advanced planar silicon transistor at advanced technology node.

Figure 6 shows the estimated throughput for SiC wafers annealed with process time representative of silicide contact.

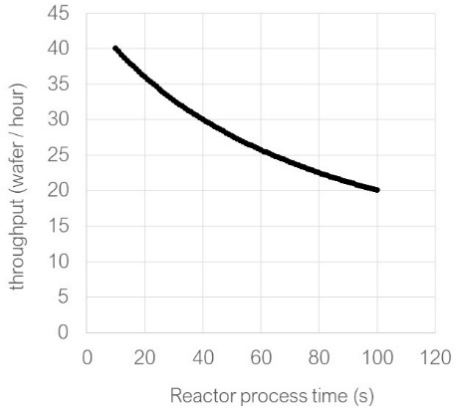

Fig. 6. Estimated throughput for SiC wafer processed in Levitor as a fonction of process time.

The absence of both long purging time prior heat-up and stabilization step during heat-up (in figure 1 the SiC wafers are annealed directly from room temperature to process temperature) combined with a forced cooldown guarantees a high throughput.

The silicon wafers were used to qualify the process (contamination, within-wafer uniformity and wafer-to-wafer repeatability). Table 1 reports the metal contamination levels before and after annealing. The residual oxygen level during anneal was less than 1ppm.

Table 1. Contamination level atoms/cm^2 (VPD ICPMS) before and after anneal at 1000 ºC for 60 s in N_2

	Before anneal	After anneal
Al; Ca; Co; Cu; Na;Ta; Ti; V;W; Zn	Not detected	Not detected
Cr	Not detected	1,5E9
Fe	6,4E8	5,8E8
Mn	Not detected	6,3E7
Ni	Not detected	5,2E9

The within-wafer uniformity and wafer-to-wafer repeatability was measured on high energy (30 keV) Arsenic implanted silicon wafers. The advantage of such deep implant is that the dopant activation process remains sensitive to temperature variation even after long soak annealing time at 1000 ºC. It is therefore considered as a good indicator of the wafer temperature uniformity during silicidation anneal at 1000 ºC for 30 s. The anneals were performed without any process tuning (i.e in the same configuration as for the SiC wafer). Figure 7 shows the sheet resistance measurements after annealing.

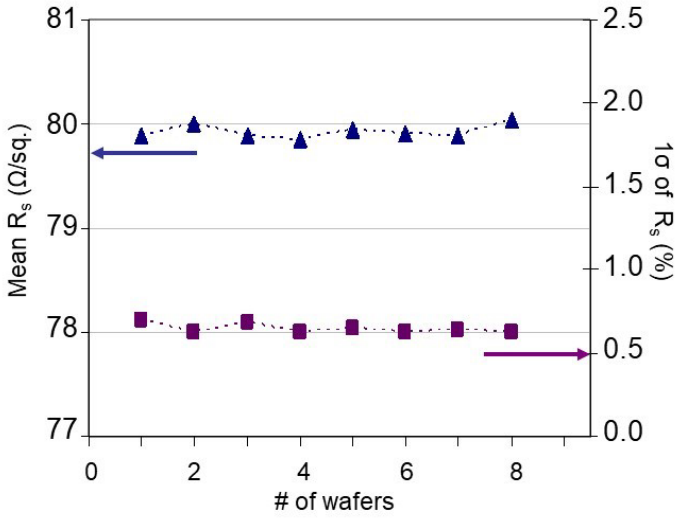

Fig. 7. Arsenic_1E16 As/cm^2 _ 30 keV implanted wafers after anneal at 1000 ºC for 30 s. the left hand scale is the sheet resistance (5 mm edge exclusion) the right hand scale shows the wafer uniformity.

The high accuracy (~10 ms) mechatronics of the Levitor system ensure an excellent wafer-to-wafer (WtW) temperature repeatability. The temperature sensitivity was calculated by measuring the Rs deviation after processing 2 extra wafers at + 5 deg and -5 deg as compared to setpoint. The calculated temperature sensitivity was of 0.35 Ω/sq/ºC which correspond to a WtW temperature uniformity of 0.2 ºC.

Conclusion

The advantage of conductive heating is that annealing of SiC wafers becomes independent of emissivity, providing better uniformity and repeatability of wafer temperature. Si wafers can be used for rapid and accurate process montoring. Uncontrolled silicidation occurring during heating and cooling of the SiC wafer could be avoided by high heating and cooling rates. Long purge time is not needed and the risk of residual oxygen is reduced because no graphite boxes are used. The wafer cools down quickly because there is no need of successive cooling steps caused by the thermal mass of the graphite box. This allows achieving high throughput, e.g. > 20 wph for process time of 60 s. The technology used in the Levitor RTA system (conductive heating of a wafer supported by gas bearings) allows low contamination level (all below ≤ 1E10 at/cm2). The pressure created in the gas bearing during wafer processing ensures oxygen levels during annealing are less than 1 ppm.

References

[1] Kimoto, T.; Cooper, J.A. Fundamentals of Silicon Carbide Technology, 1st ed.; John Wiley & Sons: Singapore, 2014.

[2] Roccaforte, F.; Fiorenza, P.; Greco, G.; Lo Nigro, R.; Giannazzo, F.; Patti, A.; Saggio, M. Challenges for energy efficient wide band gap semiconductor power devices. Phys. Status Solidi A **2014**, 211, 2063–2071.

[3] Z. Wang, S. Tsukimoto, M. Saito and Y. Ikuhara; Introducing Ohmic Contacts into Silicon Carbide Technology; WPI Research Center, Advanced Institute for Materials Research, Tohoku University 2-1-1 Katahira, Aoba-ku, Japan Silicon Carbide – Materials, Processing and Applications in Electronic Devices

[4] Kimoto, T. Material science and device physics in SiC technology for high-voltage power devices. Jpn. J. Appl. Phys. 2015, 54, 040103.

[5] She, X.; Huang, A.Q.; Lucía, Ó.; Ozpineci, B. Review of silicon carbide power devices and their applications. IEEE Trans. Ind. Electron. 2017, 64, 8193–8205.

[6] F. Roccaforte, G. Brezeanu, P.M. Gammon, F. Giannazzo, S. Rascunà, M. Saggio, Schottky contacts to silicon carbide: physics, technology and applications, in "Advancing Silicon Carbide Electronics Technology vol. I", Mater. Res. Found. 37(2018) 127–190

[7] F. Roccaforte, F.Fiorenza, P.Vivona, M.; Greco, G.; Giannazzo, Selective Doping in Silicon Carbide Power Devices. Materials **2021**, 14, 3923

[8] L.M. Porter, R.F. Davis: Mater. Sci. Eng. B **34**, 83 (1995)

[9] J. Crofton, L.M. Porter, J.R. Williams: phys. stat. sol. (a) **202**, 581 (1997)

[10] M.J. Bozack: phys. stat. sol. (a) **202**, 549 (1997)

[11] S.W. King, R.J. Nemanich and R.F. Davis: J. Electrochem. Soc. **146**, 2648 (1999)

[12] L. Muehlhoff, W.J. Choike, M.J. Bozack, J.T. Yates, Jr.: J. Appl. Phys. **60**,2842 (1986))

[13] R.J. Trew: phys. stat. sol. (a) **162**, 409 (1997)