Materials Science Forum
ISSN: 1662-9752, Vol. 1158, pp 67-74
doi:10.4028/p-q2IYST

Submitted: 2024-09-20
Revised: 2025-08-06
Accepted: 2025-08-06
Online: 2025-09-08

Investigation of Interface and Reliability of 3C- and 4H-SiC MOS Structures through Gate Dielectric Stacking and Post-Deposition Annealing

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Keywords: high-κ dielectrics, atomic layer deposition, post-deposition annealing

Abstract. This study investigates the interface and reliability of metal-oxide-semiconductor capacitors (MOSCAPs) based on 3C-SiC and 4H-SiC using atomic layer deposition (ALD) and post-deposition annealing (PDA). SiO_2 and HfO_2/SiO_2 were used as dielectric layers, with systematic PDA treatments conducted at 600°C, 900°C, and 1100°C in N_2 or forming gas (FG, a mixture of H_2 and N_2) environments to evaluate the impact of the PDA conditions on the interface characteristics of SiC MOSCAPs. The flat-band voltage for 3C-SiC MOSCAPs averaged at 0.68 ± 0.05 V for SiO_2/3C-SiC/Si samples and 2.35 ± 0.01 V for HfO_2/SiO_2/3C-SiC samples when MOSCAPs annealed at 1100°C in FG. PDA in forming gas also significantly reduced hysteresis, dropping from 1.75 V to 0.18 V for SiO_2/3C-SiC and from 2.49 V to 0.04 V for HfO_2/SiO_2/3C-SiC samples. For 4H-SiC MOSCAPs, as-deposited devices exhibited high oxide charges and poor interface quality. The average flat-band voltages for SiO_2/4H-SiC were 9.01 ± 0.15 V, while HfO_2/SiO_2 MOSCAPs showed 6.65 ± 0.02 V. After PDA at 1100°C, the flat-band voltage improved to -0.65 ± 0.035 V for SiO_2/4H-SiC and -0.50 ± 0.05 V for HfO_2/SiO_2/4H-SiC. Additionally, hysteresis was reduced from 0.61 V to 0.15 V for SiO_2/4H-SiC and from 0.23 V to 0.05 V for HfO_2/SiO_2/4H-SiC samples. We propose a figure of merit (FOM) which is defined as the ratio of the breakdown field to the product of flatband voltage shift, hysteresis effect, and density of interface states. The results demonstrate that PDA significantly enhances the interface quality and electrical characteristics of the MOS capacitors (MOSCAPs), with nitrogen (N_2) PDA yielding higher FOM for 4H-SiC stacks and forming FG PDA showing superior interfacial quality for 3C-SiC stacks.

Introduction

In 2019, emissions from transportation, including aviation fuels, accounted for 25.9% of the overall greenhouse gas emissions in the European Union-27 [1]. Transition to electric vehicles, and improving their power electronics efficiency, is one of the best choices to decelerate global warming and reduce the effects of climate change. Due to their superior physical and electrical properties, silicon carbide (SiC)-based metal oxide semiconductor field-effect transistors (MOSFETs) have become commercially competitive with silicon insulated-gate bipolar transistors (IGBTs) in power

applications requiring blocking voltages between 600V and 1700V [2, 3]. One major challenge that reduces the yield and long-term reliability, hence the further uptake of the technology, is a high density of interface states at the SiO_2/SiC interface, which is typically two to three orders of magnitude higher than in Si-based counterparts [4, 5].

Although SiC is the only compound semiconductor that can form a native SiO_2 layer by consuming the SiC during thermal oxidation, this process differs from the thermal oxidation of Si. During the oxidation of SiC, Si reacts with O_2 to form SiO and SiO_2 products. Then the removal of the resultant carbon from the SiC must be considered. When the initially grown oxide is thin, the carbon in the matrix reacts and diffuses out in products of CO, CO_2 and CO_x. However, as the layer becomes thicker (>25nm) the diffusion of these products through the oxide and outside the oxide/atmosphere surface becomes limited. There has been evidence showing residual carbon near or at the SiC/SiO_2 interface, with strong evidence of high interface densities thereby low channel mobilities of SiC MOSFETs [6, 7]. Alternative deposition methods for SiC gate dielectrics are particularly appealing, as they prevent substrate consumption and avoid leaving excess carbon atoms, effectively addressing this issue. Due to its ability to provide highly accurate control over thickness (typically within a few angstroms), uniformity, reproducibility, and conformal deposition, atomic layer deposition (ALD) has emerged as a favoured method for depositing gate dielectrics on 4H-SiC [8]. ALD operates by sequentially introducing pairs of gaseous chemical precursors into a reaction chamber.

Gauss's law expresses the electric field in an insulator to an adjacent semiconductor by the following equation:

$$E_{ins} = \frac{\kappa_s}{\kappa_{ins}} E_s \qquad \text{Eq. 1}$$

$$C = \frac{\kappa \epsilon_o A}{t_{ox}} \qquad \text{Eq. 2}$$

where E_s is the electric field in the semiconductor κ_s and κ_{ins} are the dielectric constant of the semiconductor and insulator, respectively [4], [7]. The dielectric constant of SiO_2 is approximately 2.5 times lower than the dielectric constant of SiC. This causes the breakdown of SiO_2 first in SiO_2/SiC-based devices hence, preventing SiC from reaching its full potential. Equation 1 suggests that using insulators with a dielectric constant similar to or greater than that of SiC would be ideal for minimizing electrical stress in SiC-based electronics. As shown in Equation 2, using a high-κ material allows for the same or even greater capacitance with a physically thicker dielectric layer. Having a thicker dielectric layer helps to reduce leakage current, which in turn improves reliability and helps maintain the desired performance. In this equation, ε_0 represents the permittivity of free space, A is the area of the capacitor, and t_{ox} denotes the thickness of the dielectric layer [9]. This initiates an investigative effort into the utilization of high-κ dielectrics as the gate dielectric layer in silicon carbide (SiC) based electronic devices. Some of the properties of an ideal dielectric for SiC should be as follows. The dielectric should have low fixed and mobile oxide charges and low density of fixed and mobile interface states. Moreover, the dielectric should have a high breakdown field, a large energy band gap, a high dielectric constant, and a high band offset with SiC to minimise leakage current. Despite having several reported studies of high- κ dielectrics-SiC with good electrical properties [5, 10-12]. High leakage current still is a huge hampering factor. To resolve this problem scientists proposed a high- κ material with a thin SiO_2 layer to have an initial large band offset in high-κ/SiO_2/SiC structures.

Oxide deposition techniques such as atomic layer deposition (ALD) and low-pressure chemical vapour deposition (LPCVD) have already been shown to offer a solution to improve control of the interface and circumvent SiC-specific defects, such as carbon clusters, which are inherent in industry-standard thermal oxidation processes [8]. Post-deposition anneals (PDAs) of ALD-deposited SiO_2 layers in forming gas (FG) mixture of H_2-N_2 and N_2 have had a positive impact on both mobility and reliability [8, 13].

In this investigation, we further explore the effect of PDAs on ALD-formed dielectric stacks on 3C-SiC and 4H-SiC MOS-capacitors (MOSCAPs). The dielectric stacks, comprising SiO_2 and HfO_2/SiO_2 underwent PDAs across a temperature range from 600°C to 1100°C in either pure N_2 or a forming gas (5% H_2 in N_2). The ALD as-deposited SiO_2/4H-SiC and HfO_2/SiO_2/4H-SiC MOSCAPs exhibit a high oxide charge and poor interface quality, which are significantly enhanced after undergoing a PDA process. In contrast, the ALD as-deposited 3C-SiC MOSCAPs show slightly better initial interface characteristics compared to their 4H-SiC counterparts, and they too display notable improvements following the PDA treatment. Interface characteristic metrics such as interface state density, flatband voltage shift, hysteresis, and breakdown voltages in the annealed samples are analyzed to assess the improvements brought by the PDA process. To evaluate the overall quality of the MOSCAPs, a figure of merit (FOM) is proposed, defined as the ratio of the breakdown field to the product of the flatband voltage shift, hysteresis, and interface state density. Our analysis revealed that PDA in N_2 ambient produces higher figures of merit (FOM) for the 4H-SiC MOSCAPs, while FG PDA results in higher FOMs for the 3C-SiC MOSCAPs, indicating better interfacial quality in the latter.

Experimental Details

4H-SiC wafers with low-doped epilayers and 3C-SiC epilayers grown on highly doped Si wafers were cleaved into approximately 1 cm x 1 cm chip-sized samples. The 3C-SiC epilayers are 3 μm thick with unintentional doping, while the 4H-SiC epilayers are 9.7 μm thick with intentional doping of 2×10^{15} cm^{-3}. The detailed growth process can be found here[14]. Cleaved samples then underwent a solvent clean (acetone, isopropyl alcohol and deionised water), and RCA process (Hydrofluoric acid (HF), RCA-1, HF, RCA-2 and HF). Then samples were loaded into a plasma-enhanced ALD chamber to deposit dielectrics. SiO_2 and HfO_2 were deposited using oxygen plasma at 200°C, with Bis(DiEthylAmido)Silane (BDEAS) as the silicon precursor and Tetrakis(dimethylamido)Hafnium (TDMAH) as the hafnium precursor. The growth rate for SiO_2 was approximately 0.05 nm per cycle, while the HfO_2 growth rate was around 0.1 nm per cycle. After the deposition of the dielectric or stacked dielectric layers, the samples underwent selective annealing process, to investigate the effects of different ambient conditions. Annealing was performed under 5 standard liter per meter (slm) flow of forming gas (5% H_2 in N_2) or in a pure N_2 atmosphere for 1 hour at temperatures of 600°C, 900°C, and 1100°C. This process was critical for studying the impact of the PDA on the material properties, as highlighted in previous work [8]. Table 1 illustrates the fabrication matrix of SiC MOSCAPs. A standard photolithography lift-off and metal deposition processes were applied to pattern Al dots with a thickness of 200 nm. Before backside metal contact the backsides of the wafers were etched to eliminate any native oxide layer.

Table 1. A comprehensive overview of the substrate materials, dielectric stack compositions, and post-deposition annealing conditions employed in the fabrication of SiC MOSCAPs.

Substrate	Dielectric Stack	Post-deposition annealing ambient conditions	Post-deposition annealing temperature conditions
• 4H-SiC • 3C-SiC	• SiO_2 (30 nm) • HfO_2/SiO_2 (25nm/5nm)	• As-dep • N_2 • Forming Gas (5 % H_2 in N_2)	• As-dep • 600°C • 900°C • 1100°C

Results and Discussion

Figure 1(a) presents a schematic illustration of the fabricated HfO_2\SiO_2\4H-SiC MOSCAPs. The MOSCAPs with only a single SiO_2 layer had a 30 nm thick SiO_2 layer deposited, while those with HfO_2 included a 5 nm SiO_2 interfacial layer before the HfO_2 deposition. The thin SiO_2 layer is essential in reducing leakage current, as HfO_2 has a lower bandgap and, therefore, a smaller conduction band offset with SiC compared to SiO_2, which can increase leakage. The higher conduction band offset of the SiO_2 layer acts as a barrier, effectively minimizing leakage while still allowing the HfO_2 to enhance capacitance [9, 15]. This combination significantly improves the overall performance of the MOSCAP. Figure 1(b) shows a TEM image of the thin intermediate SiO_2 (5.21 nm) layer and HfO_2 (24.3 nm) layer. MOSCAP structures.

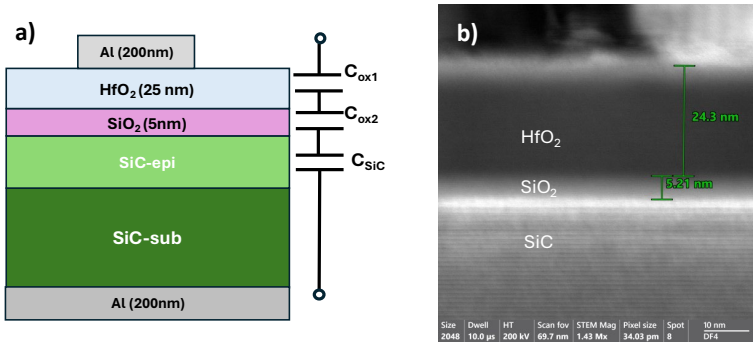

Fig. 1. (a) Schematic representation of the fabricated MOSCAPs and associated circuitry. **(b)** Cross-sectional TEM image demonstrating the thickness of the HfO_2\SiO_2 stack in the MOSCAP structures.

Electrical Characterization

To further investigate the interface characteristics of the ALD-deposited dielectrics on 3C-SiC and 4H-SiC MOSCAPs, room temperature capacitance-voltage measurements were carried out. Figure 2 shows normalized C-V responses were taken from 12 devices at 1 kHz to 1 MHz frequencies.

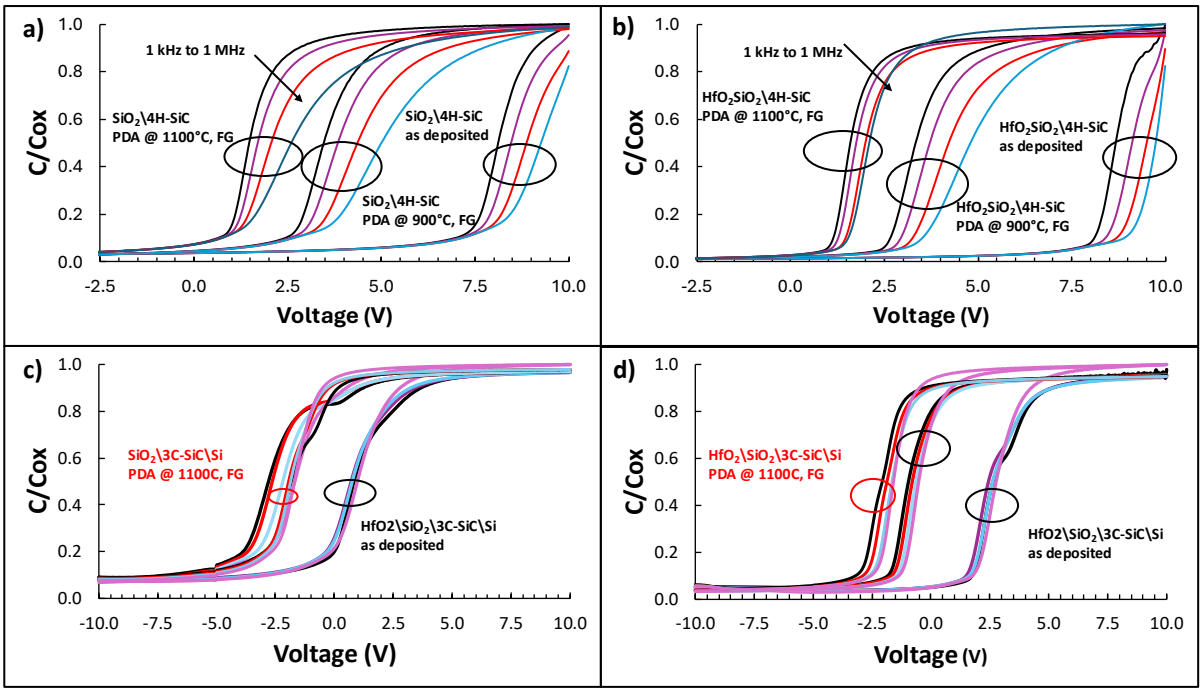

Fig. 2. C-V curves of 4H-SiC a) and b) and 3C-SiC (c and d) MOS capacitors with different gate dielectric stacks annealed at various temperatures in FG gas ambient. The device area for each device is 1.26 $x10^{-3}$ cm^2.

4H-SiC MOSCAPs

As-deposited 4H-SiC MOSCAPs with SiO_2 and $HfO_2\backslash SiO_2$ dielectric layers as the gate oxide typically exhibit significant quantities of net negative charge, both within the oxide and at the interface. This is reflected in their flat band voltages, with SiO_2 MOSCAPs averaging 9.01 ± 0.15 V, while HfO_2/SiO_2 MOSCAPs show a lower average of 6.65 ± 0.02 V. Additionally, these devices do not display accumulation mode, suggesting a leaky oxide layer as it can be seen in figure 3. While the breakdown voltage of SiO_2 MOSCAPs improves with both FG and N_2 annealing, the breakdown voltage of HfO_2/SiO_2 improves only with N_2 annealing. This phenomenon requires further investigation to elucidate the underlying factors influencing this behaviour. However, after annealing the devices at 600°C, 900°C, and 1100°C, the C-V curves begin to shift to the left, indicating passivation of the negative charges. Notably, after annealing, the capacitance of the device saturates entirely when they are swept into deep accumulation, further confirming improvements in the oxide quality. When annealed at 1100°C for 1 hour in forming gas (FG) ambient, the average flat-band voltages improved to -0.65 ± 0.035V and -0.50 ± 0.05 V, reflecting a reduction in net negative charge for $SiO_2\backslash$4H-SiC and $HfO_2\backslash SiO_2\backslash$4H-SiC samples, respectively. In addition to improving the flat band voltage, annealing the 4H-SiC samples significantly reduces hysteresis. The hysteresis was notably reduced, improved from 0.61 V to 0.15 V for the SiO_2/4H-SiC MOSCAPs, and from 0.23 V to 0.05 V for the HfO_2/SiO_2/4H-SiC MOSCAPs. Alongside the reduction in hysteresis, a low level of density of interface states (D_{IT}) was obtained, which was extracted using the high-low C-V measurement method, with 300 Hz as low frequency and 1 MHz as high frequency. The density of interface states for 4H-SiC MOSCAPs averaged at $1.14 \pm 0.16 \times 10^{12}$ $cm^{-2}eV^{-1}$ for $SiO_2\backslash$4H-SiC and $1.04 \pm 0.04 \times 10^{12}$ $cm^{-2}eV^{-1}$ for $HfO_2\backslash SiO_2\backslash$4H-SiC at 0.2 eV below conduction band (E_C-E_t=0.2 eV) after annealing at 1100°C in an N_2 ambient.

3C-SiC MOSCAPs

On the other hand, with a narrower band gap (2.3 eV), 3C-SiC has several advantages over 4H- and 6H-SiC: it requires a lower electric field for inversion and has a significantly lower trap density at the 3C-SiC/SiO_2 interface. Additionally, the high density of near-interface traps in the conduction band does not affect channel current, further improving the performance of 3C-SiC MOS structures compared to 4H-SiC. Furthermore, the larger conduction band offset at the 3C-SiC/SiO_2 interface (3.7 eV), which even exceeds that of the Si/SiO_2 interface, suggests that 3C-SiC devices may offer greater reliability [15,16]. Consequently, as-deposited 3C-SiC samples exhibit strong accumulation, near-ideal flat band voltage, and narrower C-V curves between high and low frequencies as can be seen in Figures 2 c) and d). The flat band voltages were found to average at 0.68 ± 0.05 Vand 2.35 ±0.01 V for $SiO_2\backslash$3C-SiC\Si and $HfO_2\backslash SiO_2\backslash$3C-SiC\Si samples, respectively. They showed similar behaviours compared to 4H-SiC samples post-annealing. When annealed at 1100°C for 1 hour in FG ambient, the average flat-band voltages shifted to -1.73 ± 0.04 V and -1.86 ± 0.06 V. Although annealing the 3C-SiC samples doesn't seem to improve the flat band voltages, it greatly reduces the hysteresis. The hysteresis effect was significantly improved, reducing from 1.75 V to 0.18 V for the $SiO_2\backslash$3C-SiC\Si sample, and from 2.49 V to 0.04 V for $HfO_2\backslash SiO_2\backslash$3C-SiC\Si sample. 3C-SiC MOSCAPs, showed slightly better D_{IT} values, achieving $0.38 \pm 0.02 \times 10^{12}$ $cm^{-2}eV^{-1}$ for $SiO_2\backslash$3C-SiC\Si and $0.85 \pm 0.05 \times 10^{12}$ $cm^{-2}eV^{-1}$ for $HfO_2\backslash SiO_2\backslash$3C-SiC\Si at E_C-E_t=0.2 eV after annealing at 1100°C in an FG ambient, demonstrating enhanced interface characteristics.

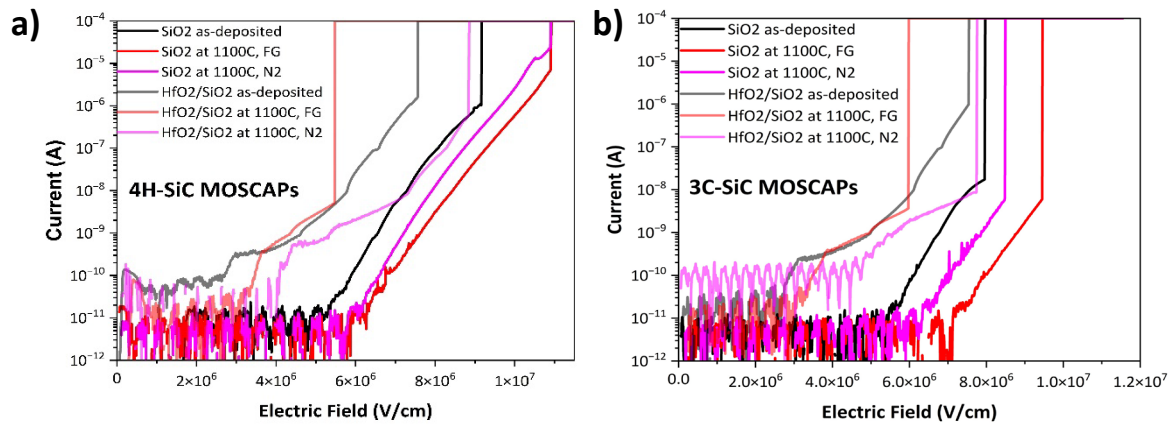

Fig. 3. Current-Voltage Characteristics of MOSCAPs: (a) 4H-SiC and (b) 3C-SiC with SiO_2 or $HfO_2\backslash SiO_2$ as dielectric layer annealed at 1100°C in FG or N_2 ambient.

Figure 4 a) and Figure 4 b) present a summary of the extracted parameters, including the breakdown field (V_{BD}), flatband voltage shift ($\Delta V_{FB} = \varphi_{ms} - V_{FB}$, where φ_{ms} is the difference between the metal and semiconductor work functions, and V_{FB} is the measured flatband voltage), hysteresis (H), and the density of interface states.

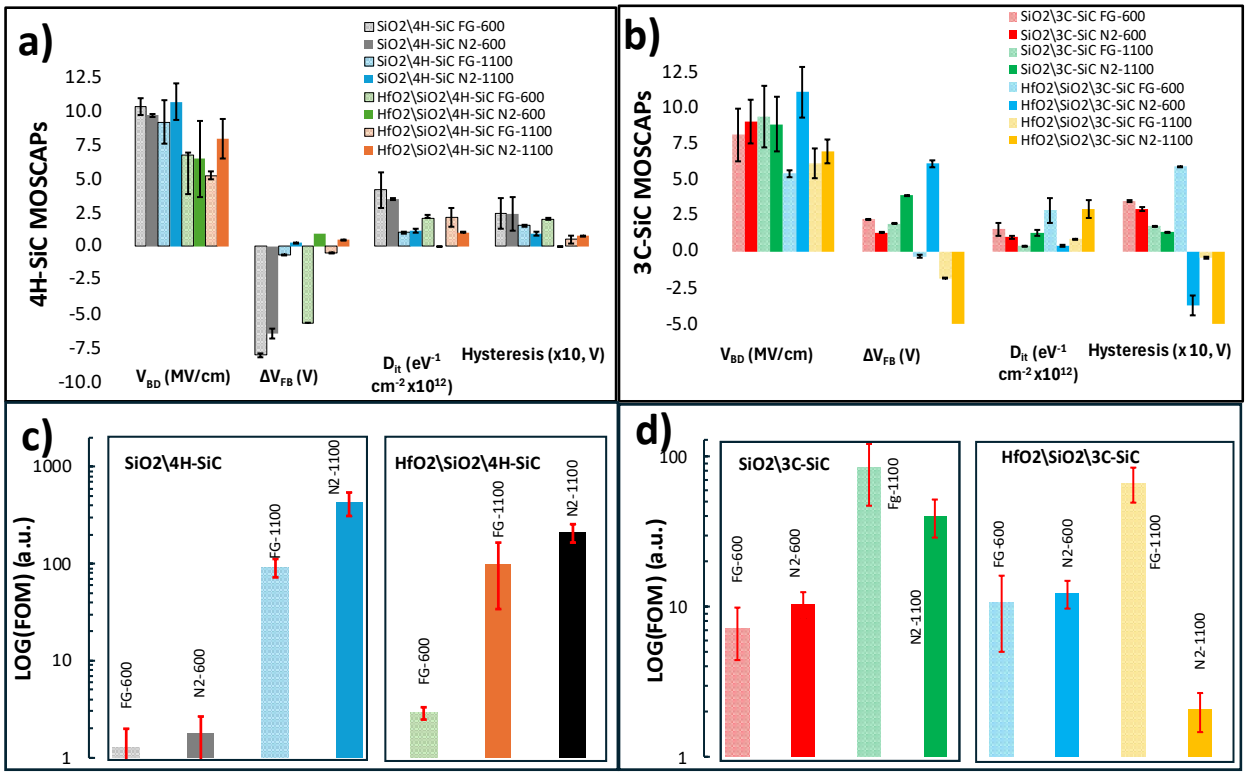

Fig. 4. a) and b) Summaries of extracted electrical parameters for the MOSCAPs, including breakdown field (V_{BD}), flatband voltage shift (ΔV_{FB}), hysteresis (H), and the density of interface states (D_{IT}). The hysteresis values scaled up 10 times. The density of interface states as measured at E_C-E_t=0.2 eV c) and d) Final calculated figures of merit (FOMs) used to determine the optimal gate dielectric stack and post-deposition annealing (PDA) conditions for 3C-SiC and 4H-SiC MOSCAPs.

For an ideal dielectric or dielectric stack, certain characteristics are desired: a high breakdown field a minimal shift in flat band voltage from its ideal value, low D_{IT}, and minimal hysteresis. To evaluate the overall quality of gate dielectrics, we propose a figure of merit (FOM) which shows the ratio of the breakdown field to the product of flat band voltage shift, hysteresis effect, and density of interface states:

$$FOM = V_{BD}/(\Delta V_{FB} * H * D_{it}) \quad \text{Eq.3}$$

We propose this as a metric to help gauge the effectiveness of gate dielectrics. The final calculated FOMs to evaluate the optimum gate dielectric stack and PDA condition for 4H-SiC and 3C-SiC MOSCAPs are shown in Figures 4c) and 4d). In our analysis, we observed that the N_2 PDA yields higher figures of merit (FOM) for the 4H-SiC stacks, whereas FG PDA demonstrates higher FOMs, indicating superior interfacial quality, for the 3C-SiC stacks.

Conclusion

The investigation into the interface and reliability of 3C-SiC and 4H-SiC MOS structures through gate dielectric stacking and post-deposition annealing has yielded promising results. The use of ALD for depositing SiO_2 and HfO_2\SiO_2 dielectrics, combined with PDA treatments, has proven to be an effective strategy for improving the quality of the SiO_2\SiC interface. The optimized PDA conditions, which differ for 3C-SiC and 4H-SiC MOSCAPs, have led to a reduction in interface trap density, oxide charge, and hysteresis, while overall device performance. The proposed figure of merit (FOM) has been instrumental in determining the optimal dielectric stack and PDA conditions for each SiC polytype. The findings underscore the importance of material and process optimization in realizing the full potential of SiC technology in the fight against climate change and in the development of sustainable energy solutions.

Acknowledgements

The project “Innovations in Power MOSFET Gate technology through the use of ALD oxides” has received funding from Innovate UK / InnoSuisse call UK-Switzerland Bilateral: Collaborative R&D under project no. 10089219. The authors would like to thank Richard Jefferies and Andrew Graham from the cleanroom facility at the School of Engineering, University of Warwick, for their generous support during device fabrication and characterization.

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