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Deep Implanted SiC Super-Junction Technology

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Abstract. GE Aerospace is developing a novel fabrication method for >3.3 kV devices using ultra-high energy deep implantation and epitaxial overgrowth. We report succesful fabrication of the world's first 3.5 kV SiC SJ deep implanted junction barrier Schottky (JBS) diodes and 5 kV SiC SJ deep implanted MOSFETs, which exhibit record low specific on-resistance (Ron,sp) and superior breakdown voltages. This innovative method offers a scalable path towards more efficient medium-voltage converters, outperforming traditional SiC unipolar devices.

Introduction

Medium-voltage (MV) power conversion systems (>3.3 kV) are currently limited to switching frequencies of several hundred hertz or below due to losses in solid-state switches and diodes. The existing conventional wide-bandgap solutions for MV-class switches and diodes are constrained by the lack of availability of uniform high-quality, very lightly doped thick SiC epitaxial layers with low defect densities. Additionally, conventional SiC unipolar switches and diodes rated >3.3 kV suffer from high conduction losses at high temperatures. SiC SJ devices promise the best performance at >3.3 kV, with lower conduction loss at elevated temperature.Prior to this work,, 1.2–3.3 kV multi-epitaxial SiC SJ devices have been demonstrated [1-4]. Fabricating such devices by conventional ion implantation of dopants requires many iterations of epi regrowth due to the shallow depth of conventionally implanted atoms in SiC. GE Aerospace is currently exploring a novel fabrication architecture for >3.3 kV devices using ultra-high energy deep implantation and epitaxial overgrowth.

Experimental

GE's deep-implanted SJ technology is based on processes developed for charge-balanced (CB) devices, an intermediate structure between conventional and superjunction designs [5-6]. In these devices, the drift layer consists of buried p-type charge-balanced regions that are electrically connected to the top anode or source terminal via high-energy implanted regions, referred to as P-Bus[Ref]. We demonstrated that these devices achieve record-low differential on-resistance, which is 40% lower than the SiC 1D-unipolar limit. However, CB devices exhibited a temperature-dependent turn-on delay that decreased at higher temperatures. We showed that the delay originated from the high resistance of the low-doped P-Bus, which decreases at higher temperatures due to the higher ionization rate of p-type charges. Recently, the team demonstrated the world's first 3.5 kV SiC SJ deep implanted junction barrier Schottky (JBS) diodes (Fig. 1). These devices are formed through a small number of thick (12 µm each) epitaxial overgrowths. After each overgrowth, 12 µm deep high-energy implants form P-doped and N-doped pillars extending through the full epilayer. Fig. 2 shows atwo layer SJ-JBS diode with an Ron,sp of 4.5 mΩ·cm² at room temperature and 9.6 mΩ·cm² at 150°C, which is ~45% below the SiC unipolar limit. The breakdown voltage is 3.8 kV with low leakage prior to breakdown.

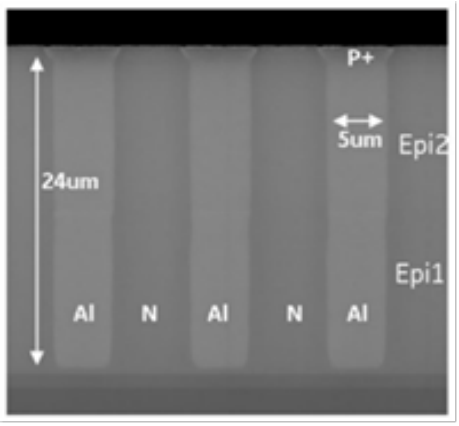

Fig. 1. SEM image of 3.5 kV (2× epi and deep-implanted) SiC SJ-JBS diode.

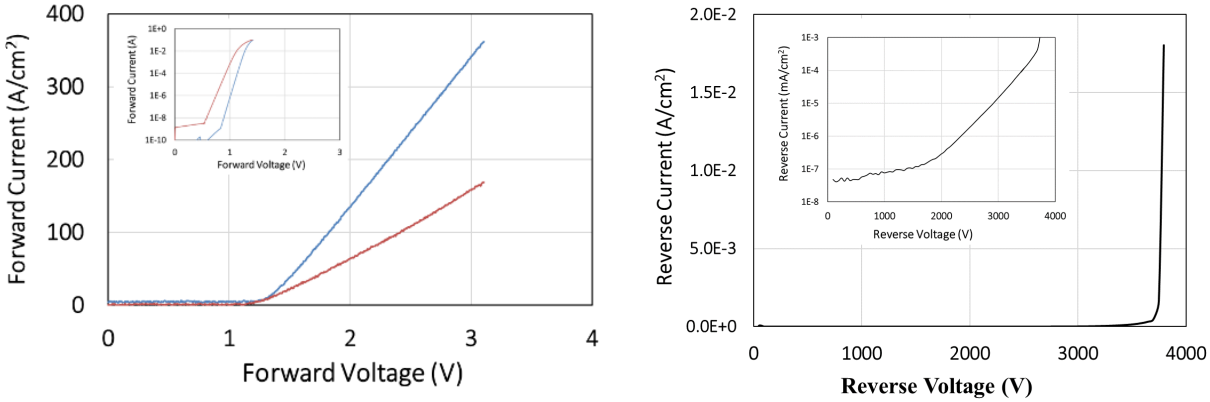

Fig. 2. Forward and reverese characteristics of 3.5kV SiC deep implanted SJ JBS diodes.

Reverse recovery measurements of SiC SJ diodes were performed using ITC57300/57220 with results shown in Fig. 3. No change in the turn-off current and voltage waveforms were observed when the junction temperature increased from room temperature to 150°C and the total device capacitive charge is estimated at <700nC/cm^2.

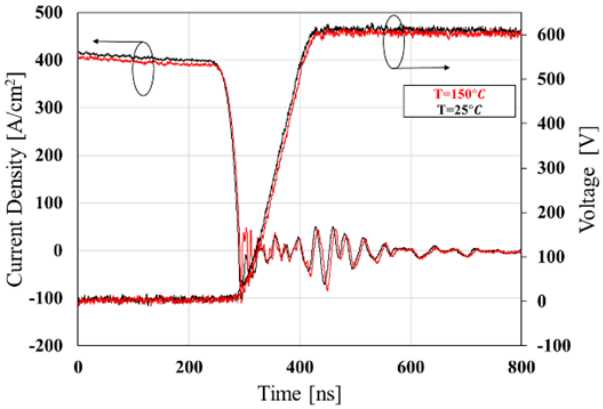

Fig. 3. Reverse recovery characteristics of 3.5kV SiC deep-implanted SJ JBS diodes at room temperature and 150°C.

The GE team also demonstrated the world's first 5 kV SiC SJ deep implanted MOSFETs (Fig. 4). These devices were formed with three rounds of ultra-high energy deep implantation and epitaxial overgrowth. The conduction and blocking characteristics of the 5 kV deep implanted SJ MOSFET are plotted in Fig. 5. The Ron,sp at room temperature is 9 mΩ·cm², which is 25% below the SiC unipolar drift region limit. The device demonstrates a sharp and stable avalanche breakdown voltage at 5.1 kV and a leakage current density of <10 μA/cm² below 4 kV. Fig. 6 illustrates the turn-off and turn-on characteristics of the SJ MOSFETs during double-pulse switching at 2000 V and 2 A. The total switching loss, calculated for 2000 V at 2 A (50 A/cm²) measurements, was 323 μJ (8.1 mJ/cm²), positioning these devices among the best in class for 5 kV MOSFETs. The turn-off time for the SJ MOSFET is noticeably longer than the turn-on time. This characteristic has been previously reported and is caused by the large superjunction p-n pillar junction area, which results in higher Coss capacitance in superjunction devices [7].

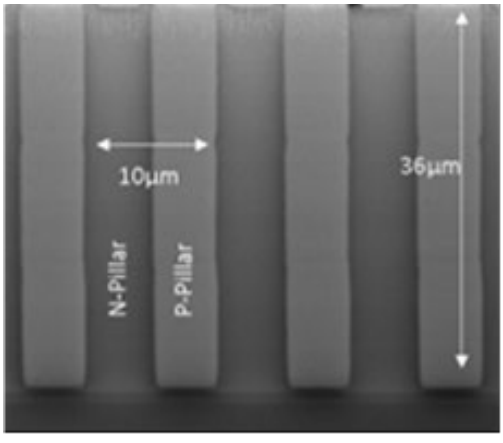

Fig. 4. SEM image of 5kV (3× epi and deep-implanted) SiC SJ-MOSFETs.

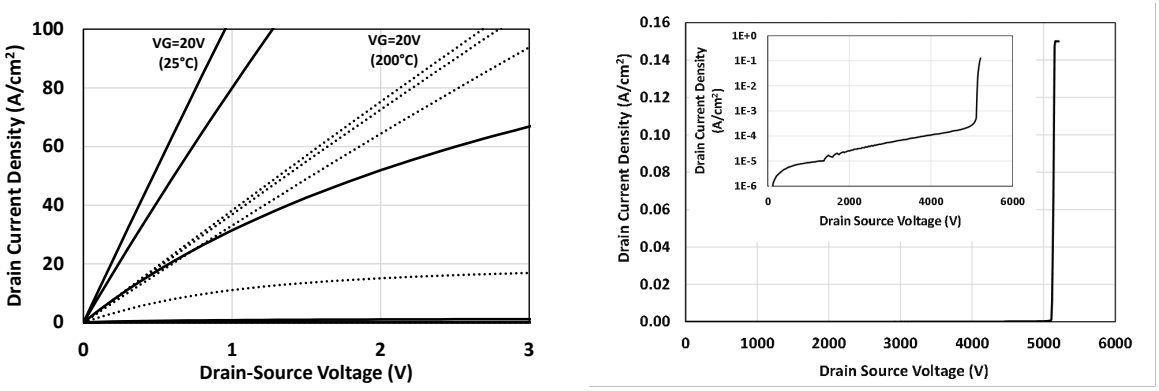

Fig. 5. Forward and reverese characetristics of 5kV SiC deep implanted SJ.

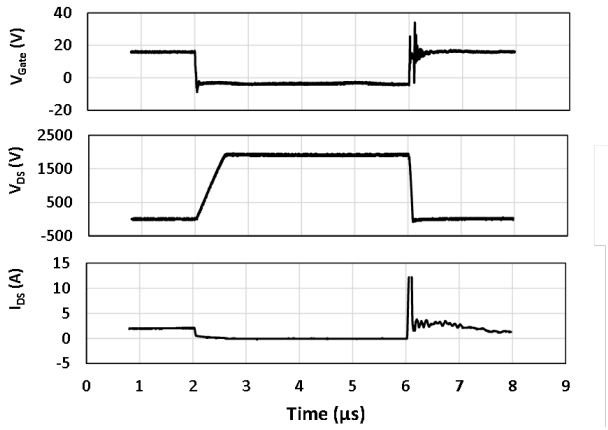

Fig. 6. Switching waveform characteristics of deep-implanted SJ MOSFETs under duple pulse testing.

The ultra high enregy implantation required for fabrication of these devices results in a new processing challenge. To fully recover defects following implantation, SJ devices need to undergo a high temperature activation anneal at 2000 °C; devices receiving only the conventional activation anneal at 1700 °C exhibit high leakage (Fig.7). This requirement emerged from an extensive Synchrotron X-ray Rocking Curve Topography (SXRCT) and Reciprocal Space Mapping (RSM) analysis, which revealed a high level of strain induced by high-energy implantation of Al and N in 4H-SiC [8]. The study showed that conventional annealing at 1700 ℃ was insufficient to recover the strain and suggests that higher annealing temperatures, as high as 2000 ℃, lead to better lattice recovery.

Fig.8 is a comparison between GE‘s CB and deep implanted SJ devices and the SiC unipolar entitlement showing a scalable path toward realization of more efficient MV conveters.

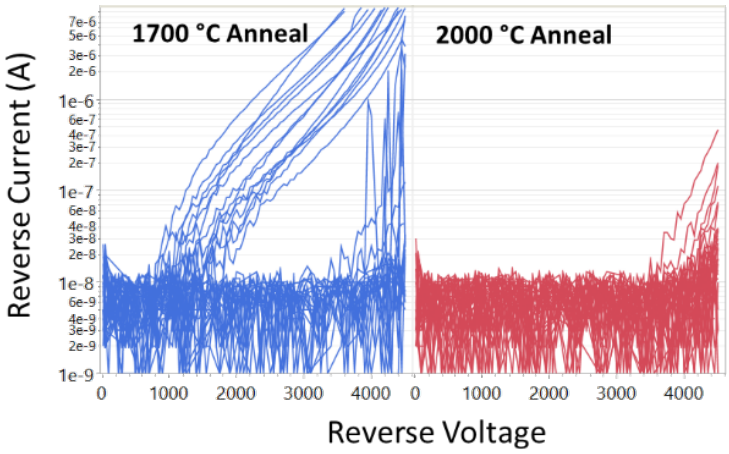

Fig. 7. Comparison of the leakage current of 4.5kV SiC SJ MOSFETs annealed at 1700°C and 2000°C.

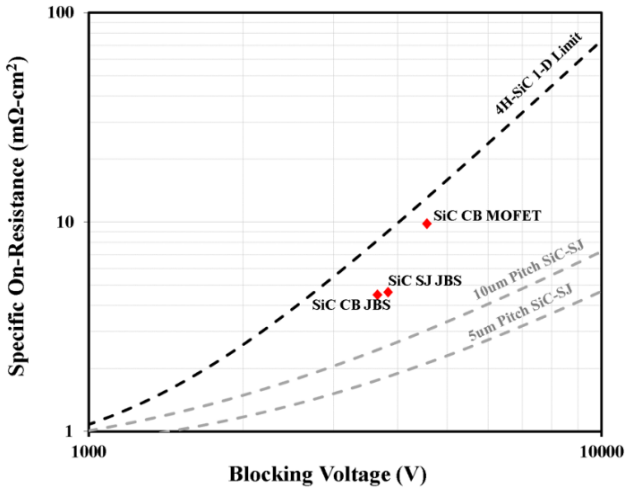

Fig. 8. Comparison between GE's reported CB and deep-implanted SJ devices, together with the 4H-SiC unipolar and SJ limits.

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