

Study of SiC Trench Etching Characteristics for Different Crystal Planes

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Abstract. We have successfully demonstrated comprehensive trench etching of 4H-SiC across various crystal orientations. The results show that both the trench profile and etching depth are unaffected by changes in crystal plane orientation. We achieved our target trench etching depth of 1.9 μm , with vertical sidewall profile angles ranging from 87° to 90° for different crystal planes. Additionally, we performed a qualitative analysis of sidewall roughness for various crystal planes using a 3DAFM scan. It was observed that crystal angles from -60° to -90° relative to the (11 $\bar{2}$ 0) plane exhibited lower surface roughness. We have also explained the mechanisms associated with these surface roughness characteristics.

Introduction

Superior properties of SiC, such as a wide band gap, high breakdown electric field, large thermal conductivity, and the ability to withstand high voltage, are highly beneficial for high power and high voltage device applications [1]. Out of three types of SiC-based devices, two types of vertical devices, the surface channel and the trench channel, have been commercialized. SiC trench power MOSFETs offer a high drive capability due to their ultra-low on-resistance, high channel mobility, and high breakdown voltage [1, 2]. Extensive research has been conducted on the properties of A-face or M-face trench MOSFETs [3, 4], but there is limited literature available on trench MOSFETs in different crystal planes [5]. To the best of our knowledge, no thorough study has been conducted on the etching characteristics of SiC trenches in relation to different crystal orientation planes. This report presents a comprehensive study, for the first time, on SiC trench etching depth, sidewall profile angle, and sidewall surface morphology in relation to various crystal plane orientations.

Methodology

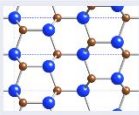
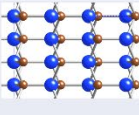
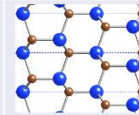

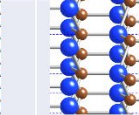
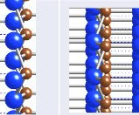
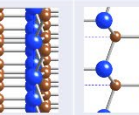
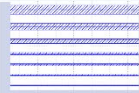
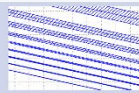
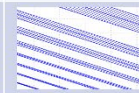
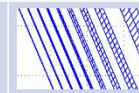
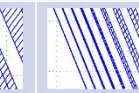
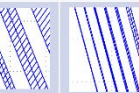
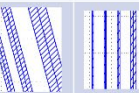
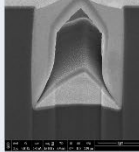
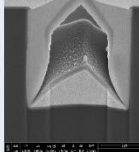
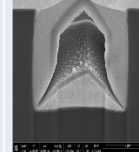
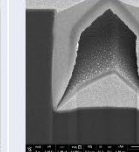
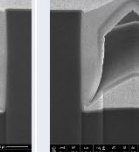
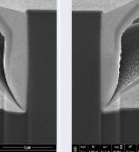
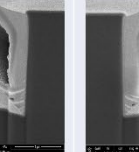
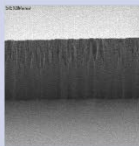
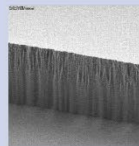
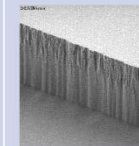
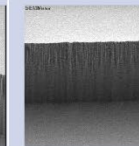
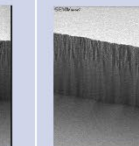
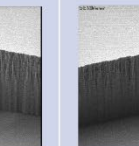
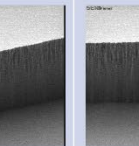
To initiate the study, a mask layout was designed with different crystal angles, each corresponding to a specific crystal plane orientation. The fabrication process was started by depositing a 2 μm SiO₂ hard mask on a 4-degree offcut, 6" 4H-SiC wafer and subsequently patterning it. Next, a dry etching process was employed to etch the 2 μm oxide hard mask under a photoresist (PR) mask using C₄F₈/Ar/O₂ gas chemistries. Subsequently, PR was stripped using O₂ plasma, and SiC trench etching was accomplished using a dry etching method with SF₆/Ar/O₂ gas chemistries under the oxide hard mask, which exhibited a SiC/oxide selectivity of 3:1. A cyclic recipe in loops with alternating gas chemistries was employed to achieve an anisotropic dry etch profile and a trench shape with vertical sidewalls, without micro-trenching. Each loop in the recipe consisted of 3 steps, having suitable gas chemistry for physical sputtering, SiC etching, and biproducts polymer removal during etching. The etching thickness and profile were verified using surface profiler measurements and a DRSEM scan. It was followed by the post-etch polymer removal using the NE14 wet clean method. Further, the

remaining oxide hard mask was removed using buffer oxide etchant (BOE), resulting in the final SiC trench profile. To analyze the trench etching depth and the sidewall profile, Focused Ion Beam Scanning Electron Microscopy (FIB/SEM) scans were conducted for each crystal angle. A qualitative analysis of the sidewall roughness for each crystal plane was performed using a 3DAFM scan.

Results and Discussion

The lattice parameters for all the crystal planes were theoretically calculated for each crystal angle. Subsequently, the corresponding crystal images were obtained by inserting the lattice parameters into the crystal maker software. Table 1 lists the crystal plane orientation, crystal images, and the mask layout corresponding to various crystal angles. In addition, the resulting FIB/SEM and DRSEM images of the SiC trench-etched profile for each crystal plane orientation are provided in this table. One of the undesirable phenomena that mostly occurs during SiC etching is micro-trenching, in which the etching at the edge of the trench is faster than at the centre [6]. This particular effect results in electric field crowding in the micro-trench region and causes early device breakdown. The SiC trench profile for each crystal angle was obtained with a vertical sidewall and without micro-trenching, as shown in the FIB/SEM images. Please note that, during FIB//SEM inspection, Platinum is coated on the sample for SEM measurement. Arrow like structures in the center of the trench is coming from the Platinum coating on the sample.

Table 1. Crystal images, mask lay-out and trench profile for various crystal planes.

Angle (°)	0	-15	-30	-45	-60	-75	-90
Crystal plane	11 $\bar{2}$ 0	21 $\bar{2}$ 0	20 $\bar{2}$ 0	31 $\bar{2}$ 0	4 $\bar{2}$ $\bar{2}$ 0	8 $\bar{6}$ $\bar{2}$ 0	1 $\bar{1}$ 00
Crystal images							
Mask Lay-out							
FIB/ SEM							
DRSEM							

DRSEM scan was conducted at each stage of etching to verify the completion of the etching layer and to examine the sidewall profile of the etched layer. Fig. 1(a) shows the DRSEM image after the oxide hard mask etching and PR stripping. Following the SiC etching, the wafer underwent a wet clean using NE14, as depicted in Fig. 1(b). A distinct interface was observed between the oxide hard mask and the SiC etched surface, demonstrating the effectiveness of the etching process. Finally, Fig. 1(c) presents the SiC trench profile after the removal of the oxide hard mask.

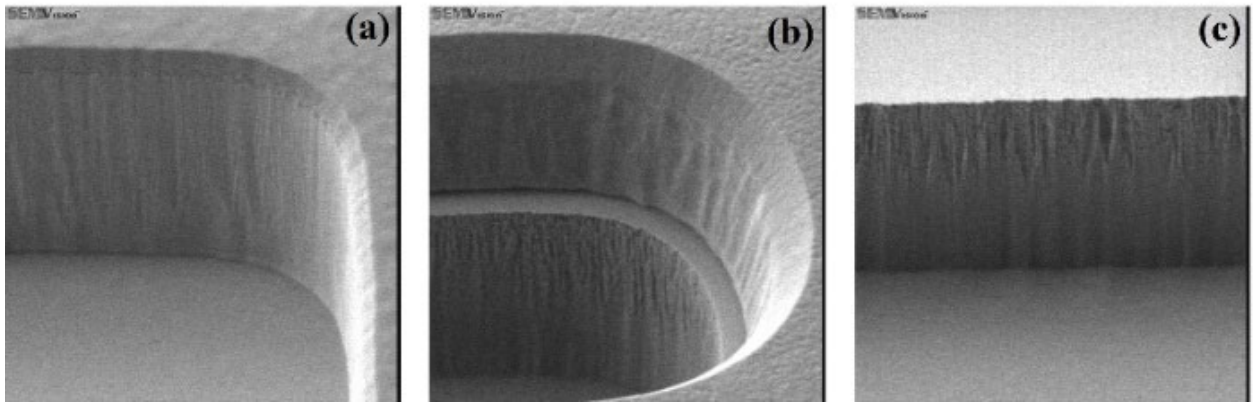


Fig. 1. DRSEM scan profile after, Oxide hard-mask etching (a), SiC trench etching (b), and post-oxide removal (c).

The sidewall profile angles were extracted from the FIB/SEM images and plotted against the crystal angles, as illustrated in Fig. 2. The reported profile angle values are the median values of 4 measurement's locations. Achieving a vertical sidewall profile angle ($87\text{-}90^\circ$) is essential for the optimal performance of Trench MOSFETs during the trench etching process. The plot shows that a vertical sidewall profile angle within the $87\text{-}90^\circ$ range was obtained across various crystal plane orientations, indicating that variations in crystal plane orientation do not impact the trench profile.

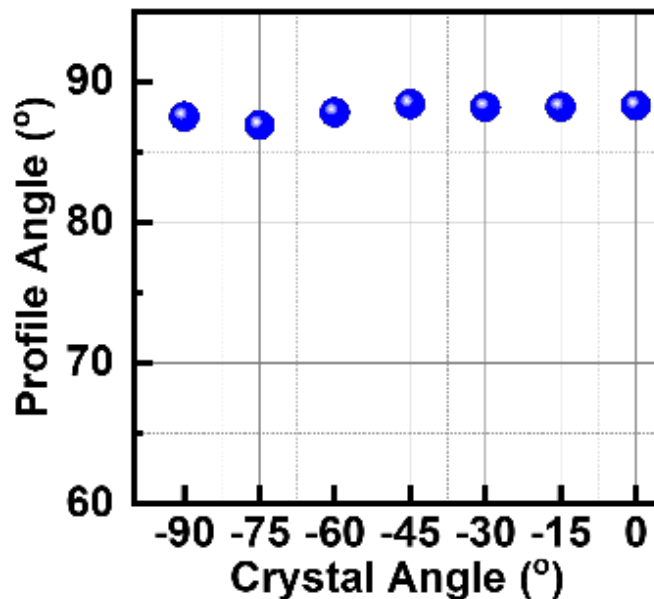


Fig. 2. Profile angle against the crystal angles.

Furthermore, it is essential to investigate the trench etching depth for different crystal planes in order to estimate the etching rate, and understand the interactions between the etching gas chemistry and the corresponding crystal atoms and orientation. The trench depth is plotted against the crystal angles, as shown in Fig. 3. It can be observed from the plot that the targeted trench etching depth of $1.9\text{ }\mu\text{m}$ was successfully achieved for various crystal planes. As expected, the trench profile and etching depth are not affected by the variation in crystal plane orientations, since the trench etching takes place in the C axis direction.

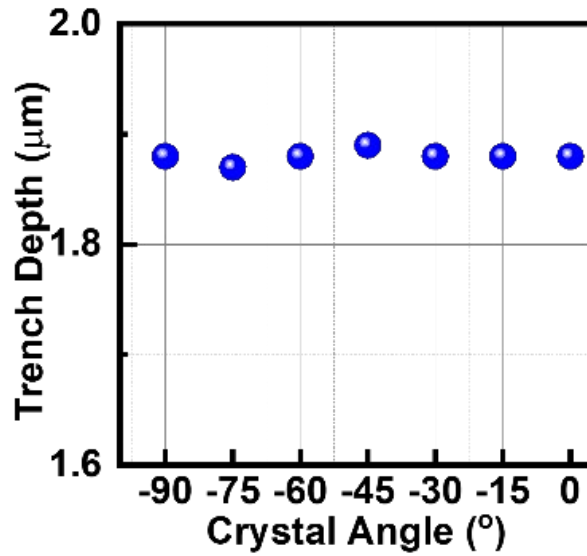


Fig. 3. Trench depth against the crystal angles.

After etching the trench, it is crucial to analyze the roughness profile of the sidewalls. A rough sidewall has adverse effects on channel mobility, gate oxide leakage, and device reliability [3, 4]. A qualitative analysis of the sidewall roughness for each crystal plane was conducted using a 3D AFM scan, as shown in Fig. 4 (a). During the scan, tip moves inside the trench, scanning 1st sidewall to bottom surface, to 2nd sidewall, and finishes scan at top of the trench. Measurement is repeated for 8 adjacent points. Measurement corresponding to these points is shown as colored line in Fig. 4 (a) (iii). Average of these 8 points is taken as final roughness value. The root mean square (RMS) roughness characteristics for different crystal plane orientations against the crystal angles are depicted in Fig. 4 (b).

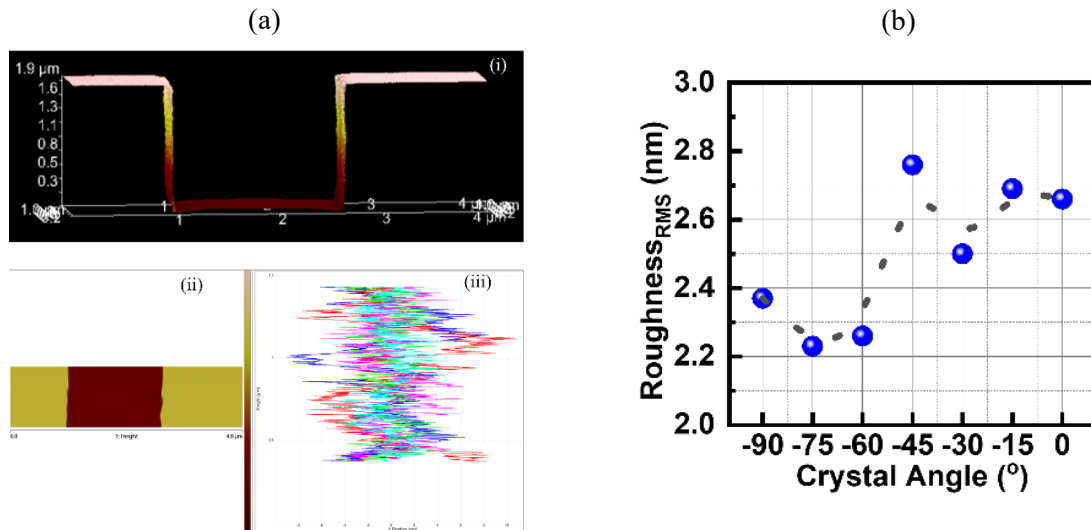


Fig. 4. 3DAFM scan profile (a), and RMS roughness against the crystal angles (b).

In the side wall images from the DRSEM scan, we observed the presence of striations on the trench sidewall, which is the main cause of surface roughness. Fig. 4 (b) illustrates that the crystal angles ranging from 0° to -45° exhibit a slightly higher roughness of 0.4 nm compared to the crystal angles of -60° to -90°. It has been previously demonstrated that dense structures are more easily smoothed by the dry etching process than loosely packed structures [7]. As depicted in the crystal images in Table 1, the crystallographic orientations of -60° and -75° are more closely packed, systematic, and homogeneous structures. This may be a possible reason for obtaining a smoother surface using plasma

etching and exhibiting lower surface roughness for these crystal angles. Further study is required to investigate this phenomenon. Additional improvement in the sidewall roughness can potentially be achieved by implementing post-trench annealing.

Conclusion

This report presents a comprehensive study, for the first time, on SiC trench etching depth, the sidewall profile angle, and sidewall surface morphology in relation to various crystal plane orientations. SiC trench profile for each crystal angle was obtained with a vertical sidewall and without micro-trenching. Vertical sidewall profile angle (within the range of 87-90°) was obtained for various crystal plane orientations, indicating that the variation in crystal plane orientation does not affect the trench profile. The targeted trench etching depth of 1.9 μm was achieved for various crystal planes. The etching depths are not affected by the variation in crystal plane orientations since the trench etching takes place in the C-axis direction. A qualitative analysis of the sidewall roughness for each crystal plane was conducted using a 3DAFM scan. The crystal angles ranging from 0° to -45° exhibit a slightly higher roughness of 0.4 nm compared to the crystal angles of -60° to -90°. Crystallographic orientations of -60° and -75° are more closely packed, systematic, and homogeneous structures, which may be a possible reason for obtaining a smoother surface using plasma etching and exhibiting lower surface roughness for these crystal angles.

Acknowledgement

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References

- [1] M. D. Pirnaci, L. Spitaleri, D. Tenaglia, F. Perricelli, M. E. Fragalà, C. Bongiorno, A. Gulino, Systematic characterization of plasma-etched trenches on 4H-SiC wafers, *ACS Omega* 6 (2021) 20667–20675.
- [2] B. Jones, J. Mitchell, J. Evans, F. Monaghan, M. Jennings, C. Bolton, K. Riddell, H. Ashraf, O. Guy, Introducing foundry-compatible SiC and GaN trench processing technologies for reliable automotive application, *Mat. Sci. Forum* 1062 (2022) 582-587.
- [3] W. Zhao, H. Ge, P. Wu, X. Bai, X. Wu and T. Zhu, Research on trench etching and photolithography process of SiC trench MOSFET, *J. Phys.: Conf. Ser.* 2083 (2021) 022093-99.
- [4] K. Kutsuki, Y. Murakami, Y. Watanabe, T. Onishi, K. Yamamoto, H. Fujiwara, T. Ito, Effect of surface roughness of trench sidewalls on electrical properties in 4H-SiC trench MOSFETs, *J. Appl. Phys.* 57 (2018) 04FR02-06.
- [5] Z. Shen, F. Zhang, X. Liu, G. Sun, Y. Zeng, Influence of H₂ treatment on the surface morphology of SiC with different wafer orientation and doping, *J. Crystal growth* 607 (2023) 127105-127112.
- [6] D. Ruixue, Y. Yintang, H. Ru, Microtrenching effect of SiC ICP etching in SF₆/O₂ plasma, *J Semicond* 30(1) (2009) 016001.
- [7] S.A.Rasgon, Thesis, Chem. Eng Dept, MIT, (2005)