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Impact of Silicon Nitride Stress on Defects Generation in 4H-SiC and the Effect of Sacrificial Oxidation on Defects Reduction

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Abstract. The impact of silicon nitride (Si_3N_4) stress on 4H-SiC has been investigated. Current-voltage (I-V) measurements on Schottky barrier diode show that Si_3N_4 films thicker than 100 nm degrade both the ideality factor and Schottky barrier height. A 45-nm sacrificial oxidation effectively reduces defects from a 100-nm-thick Si_3N_4 layer, but defects persist with films over 300 nm. Interface state density of metal oxide semiconductor capacitor with a 44-nm-thick gate oxide confirms the effectiveness of sacrificial oxidation in mitigating defects.

Introduction

Silicon nitride (Si_3N_4), renowned for its high strength, hardness, and excellent corrosion resistance, is commonly used in IC manufacturing, such as hard mask and diffusion barrier [1-2]. Previous studies have indicated that the stress induced by Si_3N_4 at high temperatures may damage the Si surface [3]. Hence, a pad SiO_2 layer is deposited before the Si_3N_4 layer to mitigate such effects, a practice also observed in SiC device fabrication [4]. However, there is scarce literature on the impact of Si_3N_4 induced stress on SiC surfaces to support the necessity of pad SiO_2 on SiC. Therefore, we fabricated Schottky barrier diode (SBD) and metal oxide semiconductor capacitor (MOSCap) to assess whether Si_3N_4 generates defects on SiC and to explore whether sacrificial oxidation can mitigate such issues.

Device Fabrication

The main process flow of SBD is shown in Fig. 1(a). Sample ID and split conditions are listed in Table 1. All samples began with nitrogen-doped 4° off-axis 4H-SiC (0001) substrate with a 5.5-μm-thick epitaxial layer. The doping concentration of the epitaxial layer was 1×10^{16} cm^{-3}. After standard RCA cleaning and a final diluted HF dip, Si_3N_4 films with various thicknesses were deposited by a LPCVD (Low Pressure Chemical Vapor Deposition) system and subsequently annealed at 1100°C in N_2 ambient to simulate the LOCOSiC (LOCal Oxidation of SiC) process [5]. Some samples underwent a sacrificial oxidation (to a thickness of 45 nm) at 1300°C in O_2 ambient after Si_3N_4 removal by hot H_3PO_4. After removing the sacrificial oxide layer, a 500-nm-thick PECVD SiO_2 layer was deposited as field oxide (FOX). Active areas were defined using photo lithography and wet etching processes. A Ti/TiN/Al stack was sputter-deposited, patterned and annealed at 500°C for 5-minutes in vacuum to form Schottky contact for SBD [6]. We also fabricated MOSCap on samples without sacrificial oxidation. To grow gate oxide, thermal oxidation was conduct at 1200°C in O_2 ambient for 140 minutes, followed by annealing at 1300°C in a NO ambient (10% NO diluted with N_2). The capacitance equivalent thickness (CET) of gate oxide is approximately 44 nm. Aluminum was deposited by thermal evaporation and patterned to form the electrode for the MOS capacitor, and all samples finished with the backside aluminum electrode and 400°C sintering in N_2 ambient.

Table 1 Sample ID and split conditions

Sample ID	Si_3N_4 Thickness (nm)	Sacrificial Oxide Thickness (nm)
Control	0	0
N36S0	36	0
N100S0	100	0
N100S45	100	45
N315S0	315	0
N315S45	315	45

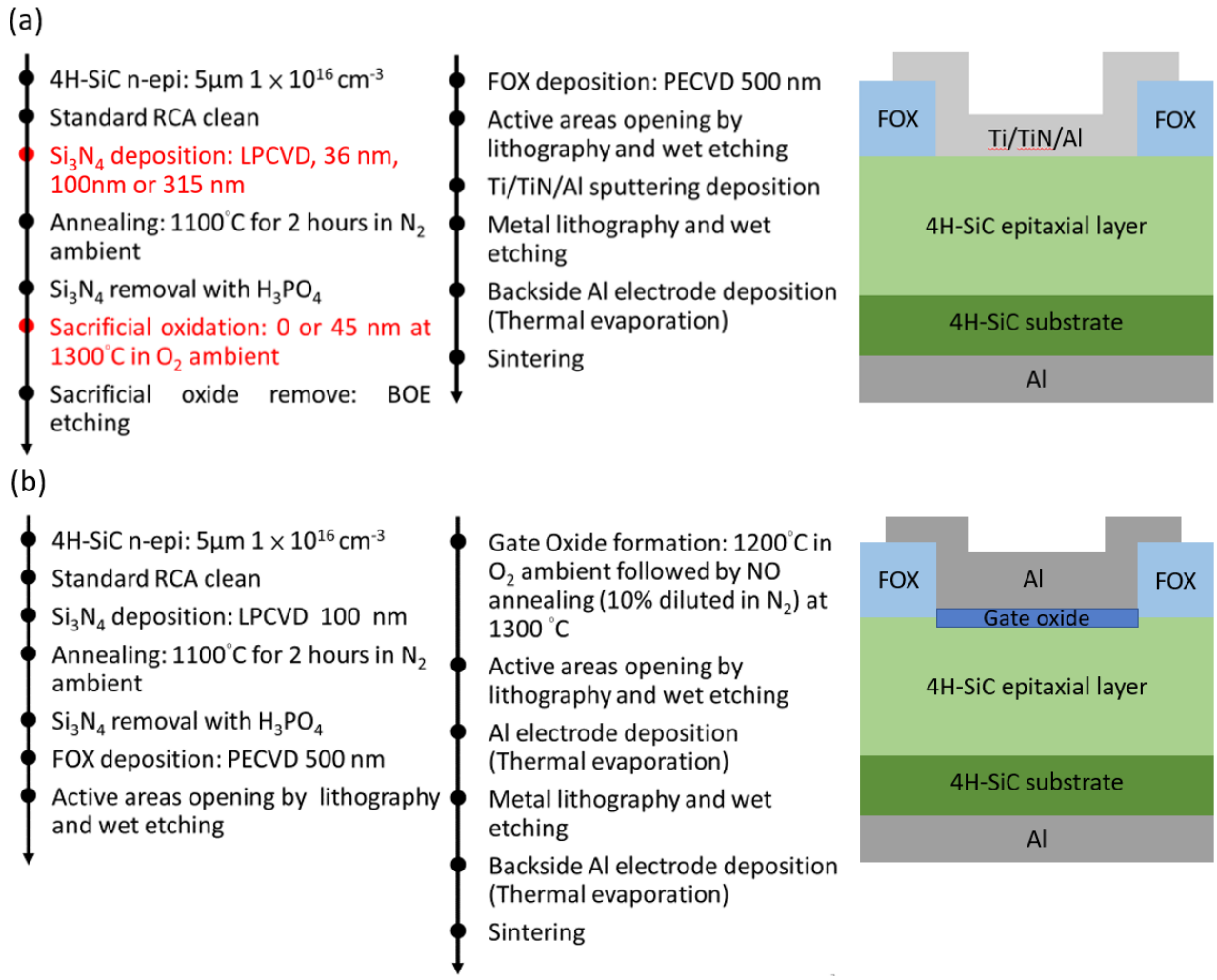

Fig. 1 Main process flow and device structure of the (a)SBD (b)MOSCap. Red letters indicate the process step with split conditions.

Experimental Results & Discussion

Fig. 2 shows the current-voltage (I-V) characteristics of the SBDs with 100-nm-thick and 315-nm-thick Si_3N_4 layer, respectively. As the Si_3N_4 layer was deposited directly on SiC substrate, thermal stress generated during the high-temperature process changed the I–V characteristics of the SBD. As shown in Fig. 2, this induced a noticeable rightward shift in the I–V curves, indicating an increase in the Schottky barrier height (Φ_b). The shift is more pronounced in the N315S0 sample compared to N100S0, suggesting that the extent of damage increases with increase of the thickness of the Si_3N_4 layer. After applying a 45-nm-thick sacrificial oxidation process, the I–V curve of the N100S45 sample shifts back and closely aligns with that of the control sample, indicating that Φ_b has returned to a level near its original value. This effective recovery indicates that the damage introduced by the

100-nm Si_3N_4 layer was shallow enough to be removed by a 45-nm-thick sacrificial oxidation process [7-8]. However, a noticeable deviation remains between the N315S45 sample and the control sample, implying that the damage caused by the 315-nm Si_3N_4 layer was more severe and deeper than the removal capability of the 45-nm sacrificial oxidation process.

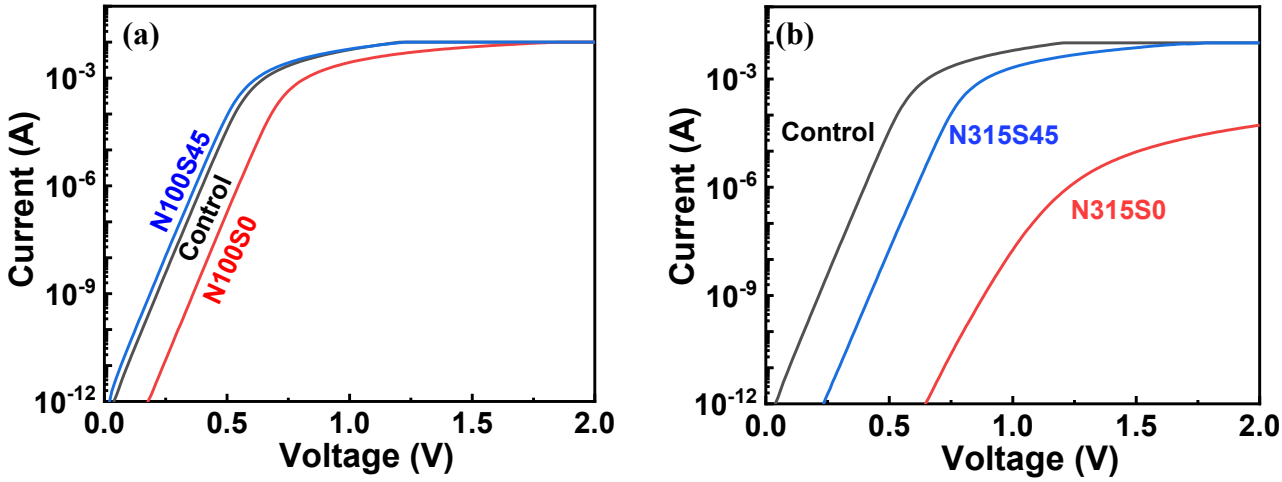

Fig. 2 Current-voltage characteristics of the (a) Control, N100S0, and N100S45 (b) Control, N315S0, and N315S45 SBDs.

To further investigate this phenomenon, the statistical distributions of the ideality factor (n-factor) and Φ_b are depicted in Fig. 3. As previously discussed, the 100-nm-thick Si_3N_4 layer leads to an increase in Φ_b, while having minimal impact on the ideality factor (n-factor). A 45-nm-thick sacrificial oxidation layer can effectively mitigate the increase in Φ_b. In contrast, the deposition of a 315-nm-thick Si_3N_4 layer without sacrificial oxidation results in poor n-factor and Φ_b values, along with a broad distribution. The significant variations in both parameters suggest non-uniform stress, likely caused by the thick Si_3N_4 layer (over 300 nm), which may crack within the layer itself, leading to uneven stress distribution [3].

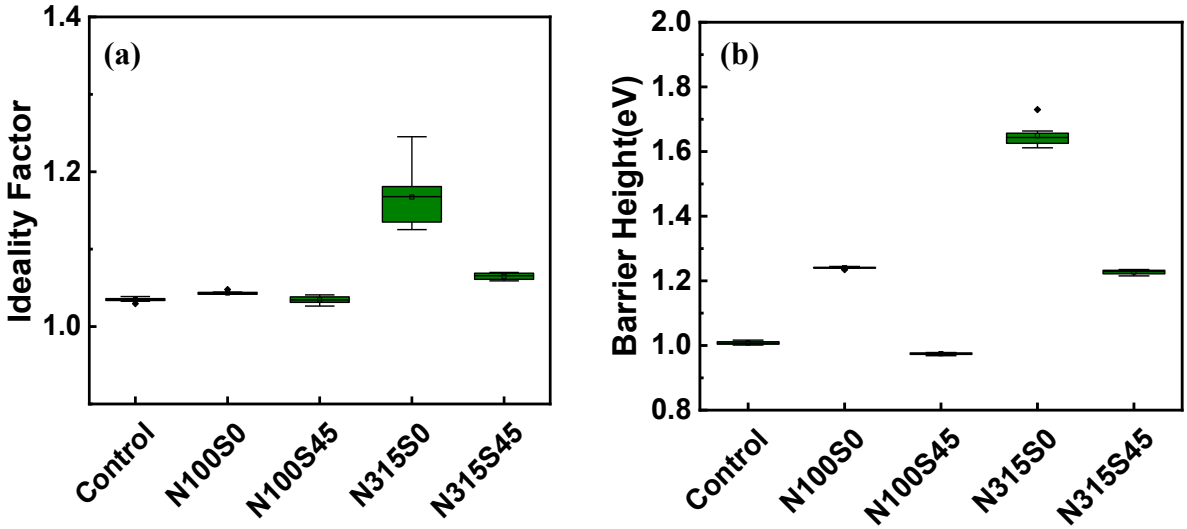

Fig. 3 Statistics of (a) ideality factor and (b) barrier height of different samples. The radius of the SBD is 100 μm. Eight SBDs were measures on each sample.

Table 2 Doping concentration and barrier height extracted from reverse C-V curve.

Sample ID	N_{sub} (cm^{-3})	Φ_b (eV)
Control	1.05×10^{16}	1.22
N36S0	1.07×10^{16}	1.22
N100S0	1.19×10^{16}	2.35
N315S0	1.19×10^{16}	4.58

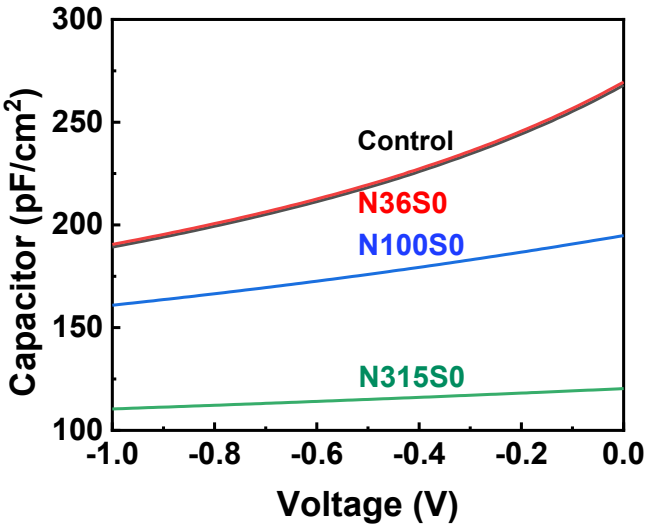

Fig. 4 Reverse-biased capacitance-voltage characteristics of Control, N36S0, N100S0, and N315S0 SBDs.

The reverse biased capacitance-voltage (C-V) characteristics measured on SBDs without sacrificial oxidation are shown Fig. 4. The measurements were performed at a frequency of 100 kHz, with the voltage sweeping from 0 V to -1 V, and the doping concentration (N_{sub}) and Φ_b calculated from the C-V curves are presented in Table 2. The C-V curves show that samples N100S0 and N315S0 exhibits significantly lower capacitance compared to the control sample. This decrease in capacitance, associated with an increased Schottky barrier height, suggests the presence of defects introduced by thermal stress. Moreover, the impact on Φ_b becomes more pronounced with increasing Si_3N_4 thickness, consistent with our earlier observations from SBD I-V measurements. It is worth noting that the Φ_b values obtained from the C-V curves are significantly higher than those derived from I-V measurements, implying that additional factors are involved, such as the presence of charge trapping and de-trapping in the defect layer within the SiC substrate. For all samples, the N_{sub} calculated from the C-V curves are close to the doping concentration of the epitaxial layer used in device fabrication, suggesting that most of the epi-layer remains unaffected. However, the Φ_b values obtained from the C-V curves are unreasonable, with the Φ_b value for the N300S0 sample even exceeding the bandgap value of 4H-SiC (3.26 eV) [9]. This indicates that a large number of traps exists in the defect layer within the SiC substrate, which are generated by the stress of the thick Si_3N_4 layer. The trapping and de-trapping of charge carriers result in a significant reduction in capacitance, leading to considerable errors in the extrapolated Φ_b. In contrast, the C-V curve for the 36-nm-thick Si_3N_4 layer (N36S0) closely overlaps with the control. The calculated Φ_b and the N_{sub} for this sample

are nearly identical to those of the control, indicating that the 36-nm-thick Si_3N_4 layer has minimal impact on the SiC.

The defect characteristics introduced by Si_3N_4 in SiC were investigated using Deep Level Transient Spectroscopy (DLTS), as shown in Fig. 5. The control group and the N36S0 group did not exhibit any significant defect signals. In contrast, the N100S0 group showed a peak around 600 K, with a defect level at E_C−1.01 eV and a trap concentration of approximately 9.8×10^{14} cm^{-3}, corresponding to the RD_3 defect previously reported to appear in SiC after He^+ implantation and radiation exposure [10-11]. The presence of this defect may lead to the slight increase in Φ_b observed in the I–V and C–V characteristics of the N100S0 group.

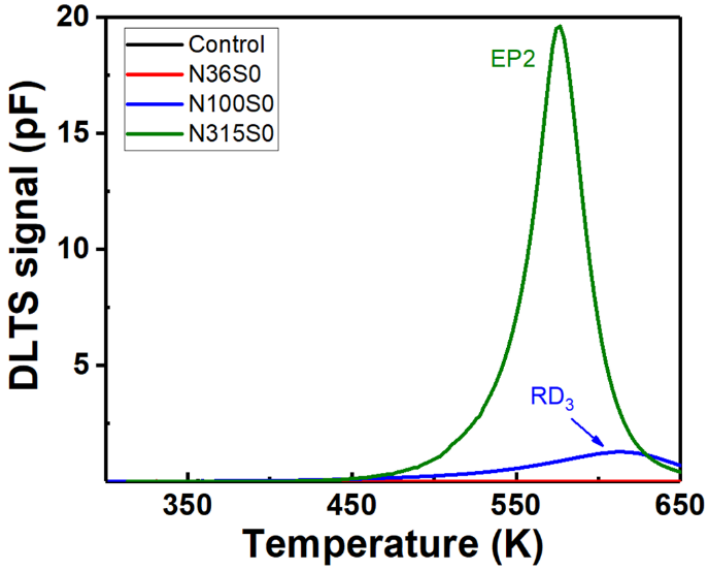

Fig. 5 DLTS spectra of Control, N36S0, N100S0, and N315S0 SBDs.

In comparison, the N315S0 group demonstrated a more pronounced peak around 560 K, corresponding to a deeper defect level at E_C−1.42 eV, associated with the well-known EP2 level, which has been suggested to be related to carbon interstitials [12]. This defect exhibited a significantly higher trap concentration of approximately 1.1×10^{16} cm^{-3}, which likely contributes to both the notable increase in Φ_b and the degradation of the n-factor in the I–V characteristics of the N315S0 group, as well as a considerable decrease in capacitance observed in the C–V measurements.

For MOSCaps, high-frequency (100 kHz) and quasi-static capacitance-voltage (C-V) measurements were conducted to calculate interface state density (D_{it}) using the high-low frequency method [9]. The capacitance equivalent thickness (CET) of MOSCap is 44 nm. The energy distribution of D_{it} is presented in Fig. 6. Both samples show that D_{it} at 0.2 eV below the conduction band edge is lower than 5×10^{11} $cm^{-2}eV^{-1}$, and they exhibit similar trends within the range of 0.2 eV to 0.6 eV below the conduction band edge. Furthermore, Time-Zero-Dielectric-Breakdown measurements on MOSCaps were conducted, and the current density-voltage (J-V) curves are depicted in Fig. 7. Both samples exhibit similar current rise trends and breakdown characteristics, showing no distinct differences.

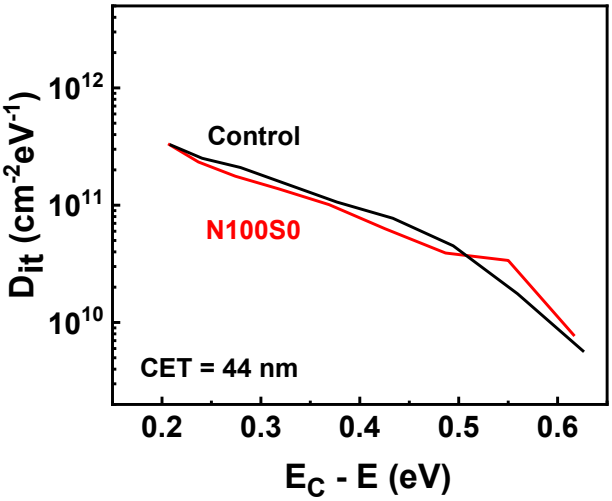

Fig. 6 Energy distribution of D_{it}, extracting by high-low frequency method on MOSCaps.

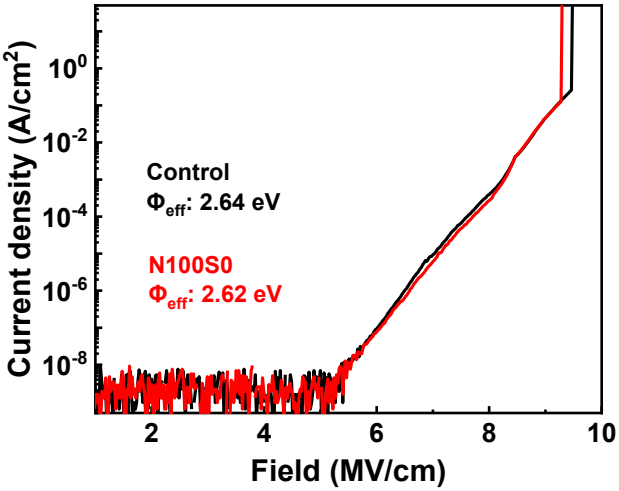

Fig. 7 Time-Zero-Dielectric-Breakdown characteristics of MOSCaps.

The rapid increase in leakage current when the electric field exceeds 6 MV/cm is attributed to Fowler-Nordheim (F-N) tunneling, which is related to the effective barrier height of the SiO_2/4H-SiC interface [13]. The effective barrier height was evaluated from the J-V curves in the 6 to 8 MV/cm range using the classical expression for F-N tunneling, which can be described as

$$J_{FN} = \frac{m_0 q^3}{16\pi^2 \hbar m^* \phi_B} \times {E_{ox}}^2 \times exp\left[\frac{-4\sqrt{2m^*}}{3q\hbar} \times (\phi_B)^{\frac{3}{2}}\right] \quad (1)$$

$$E_{ox} = \frac{V_g - V_{fb}}{T_{ox}} \quad (2)$$

where m_0 is the electron effective mass in 4H-SiC ($0.29m_e$), m^* is the electron effective mass in SiO_2 ($0.42m_e$) and m_e is the free electron effective mass. The calculated barrier heights are 2.64 eV for the control sample and 2.62 eV for the N100S0 sample, both of which are slightly lower than the theoretical value of 2.7 eV. This discrepancy can be attributed to the presence of interface traps and oxide traps [13-15]. Although no sacrificial oxidation was performed on the MOSCaps, the gate oxide thickness is similar to that of the sacrificial oxide in the SBD N100S45 sample. The defects associated with the 100-nm-thick Si_3N_4 film are nearly absent in both the D_{it} and TZDB measurements for the MOSCaps. These findings suggest that the oxidation process is effective in mitigating the impact of the Si_3N_4 layers.

Summary

A Si_3N_4 film thinner than 36 nm deposited directly on SiC generally does not impact the quality of the SiC substrate. However, a Si_3N_4 film over 100 nm thick can introduce significant stress, damaging the SiC surface layer. The presence of defects resulting from the stress can increase both the ideality factor and the Schottky barrier height. Additionally, charge trapping in the defect layer can lead to inaccurate capacitance measurements and incorrect Φ_b calculations. The extent of damage is related to the thickness of the Si_3N_4 layer—a 45-nm-thick sacrificial dry oxidation was able to mitigate the effect from the 100 nm Si_3N_4 layer but failed to eliminate defects generated from the Si_3N_4 layer over 300 nm. Therefore, similar to Si process, it is recommended to insert a pad SiO_2 layer between Si_3N_4 film and SiC.

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