Materials Science Forum
ISSN: 1662-9752, Vol. 1159, pp 15-20
doi:10.4028/p-omYG0i

Submitted: 2024-09-20
Revised: 2025-08-07
Accepted: 2025-08-08
Online: 2025-09-09

Indium-Tin-Oxide (ITO) Interlayer-Assisted Ohmic Contacts on n-Type 4H-SiC with Low Specific Contact Resistance

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Keywords: Ohmic contacts, n-type SiC, ITO interlayer, barrier height, metal-SiC interface

Abstract. This study investigates the role of ultra-thin conductive Indium-Tin-Oxide (ITO) as an interlayer at the Metal-SiC (MS) junction to lower the overall specific contact resistance (SCR) for source drain metallization applications on n-type 4H-SiC substrates.
In this work, we demonstrate an improvement in SCR by about 1 order of magnitude from ~10^{-6} Ω·cm^2 to 10^{-7} Ω·cm^2 through the integration of an ultra-thin ITO interlayer. Barrier height (Φ_B) lowering by ~ 0.1 eV was observed at the MS interface as deposited which could have assisted in the reduction of the SCR. Titanium-based Ohmic contacts were subsequently formed at 950 °C. Various thicknesses of ITO were examined to assess their influence on the formation of ohmic contacts to n-type SiC. An SCR (ρ_c) of 6.9×10^{-7} Ω·cm^2 was achieved through integration of an ultra-thin conductive ITO interlayer at the MS interface.

Introduction

The specific on-resistance (R_{ON}) in SiC devices consists of various components: n^+ contact, channel, JFET, drift, and substrate resistances. In 4H-SiC power JBSFETs, the n^+ contact resistance accounts for roughly ~ 50 % of the total resistance, given a contact width of 1 μm [1]. Therefore, minimizing the SCR becomes crucial for reducing overall R_{ON} as devices scale. The Specific Contact Resistance (SCR) in 7 nm CMOS node is much lower in comparison to SiC metal contacts due to the ease of silicide formation [2]. Hence, more studies are still needed to further improve the contact resistance to N-type SiC. The aim of this work was to minimize carbon at the Metal- SiC (MS) interface to achieve a lower SCR.

Indium Tin Oxide (ITO) is a widely used transparent conductive oxide known for its electrical conductivity. Through optimized deposition techniques, a high carrier concentration in the ITO can be obtained with low resistivity making it an ideal candidate for electrode applications. Furthermore, ITO is a CMOS compatible material which has been widely used in the industry [3].

In this study, a conductive Indium Tin Oxide (ITO) was proposed and employed to facilitate the reduction of carbon during post metal deposition annealing (PMDA). Additionally, conductive ITO enables efficient charge transport across interfaces, acting as an effective passivation layer that can reduce surface states and enhance device performance [3]. This paper further investigates the role of ITO as a conductive interlayer at the MS interface for SCR reduction and its effects as a contact material to n-type SiC.

Results and Discussion

In this study, 4° off-cut n-type 4H-SiC substrates (0001), with a doping concentration of 5×10^{18} cm^{-3}, were cleaned by standard Sulfuric-Peroxide Mix (SPM) and Buffered Oxide Etchant (BOE) (7:1) chemistries as per previous work prior to fabrication [4]. This step is crucial to ensure a clean surface prior to fabrication of the test structures to prevent defects from remaining at the MS interface. Schottky barrier diodes (SBDs) were fabricated, as shown in Fig. 1 (a), with different ITO interlayer thicknesses followed by formation of Ti/Al Schottky contacts with similar thicknesses for comparison. Ni ohmic contacts were formed on the backside of the substrate after 950 °C post-metal deposition annealing (PMDA). It is noteworthy that the backside contacts were formed prior to Schottky contacts on the front-side. Subsequently, circular transmission line method (CTLM) structures (top-to-top) for contact resistance measurement and extraction were also fabricated using a Ti-based metal stack (Ti/TiN) as shown in Fig. 1 (b) with several splits with the incorporation of various ITO interlayer thicknesses.

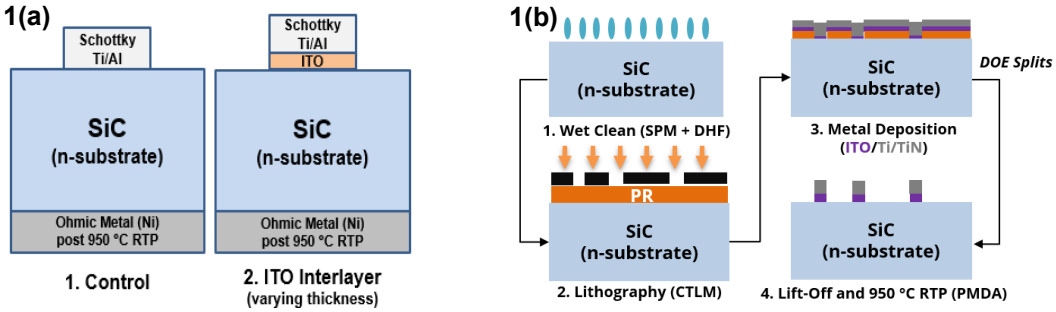


Fig. 1. Cross section of (a) SBD with Ti/Al Schottky contact (b) CTLM structures for SCR extraction.

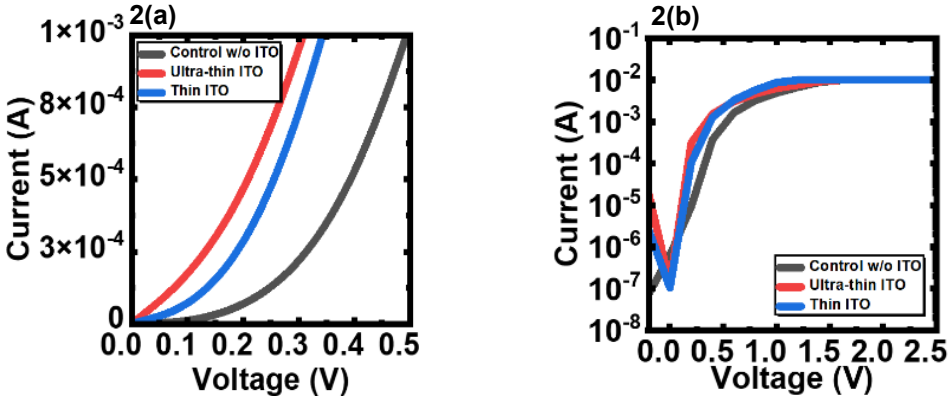


Fig. 2. I-V of SBDs with different ITO interlayer thickness as deposited in the (a) linear scale and (b) log-scale.

In Fig. 2 (a-b), I-V measurements on the SBD samples indicate a reduction in barrier height (Φ_B) by ~ 0.1 eV with the incorporation of an ITO interlayer as deposited. It was observed that the samples with ITO interlayer displayed a lower V_{knee} as compared to the control sample, without any ITO. This supported the finding of the extracted Φ_B to be lower with the incorporation of ITO interlayer. However, the I_{ON} was not changed with the incorporation of the interlayer which was expected. Following the subsequent PMDA at 950 °C, it was interesting to observe that only the ultra-thin ITO sample exhibited ohmic behaviour, as depicted in Fig. 3 (a) below. In thicker samples, a rectifying behaviour instead was observed. This rectifying behaviour was further pronounced with thicker ITO interlayer thickness as shown in Fig. 3 (a) below. This implies that a much thicker ITO interlayer could have hindered the intermetallic diffusion of the Ti-based metal stack into the SiC lattice which may have resulted in the undesired rectifying behaviour. Hence, careful optimization was needed to ensure a suitable thickness for desirable low SCR ohmic contacts.

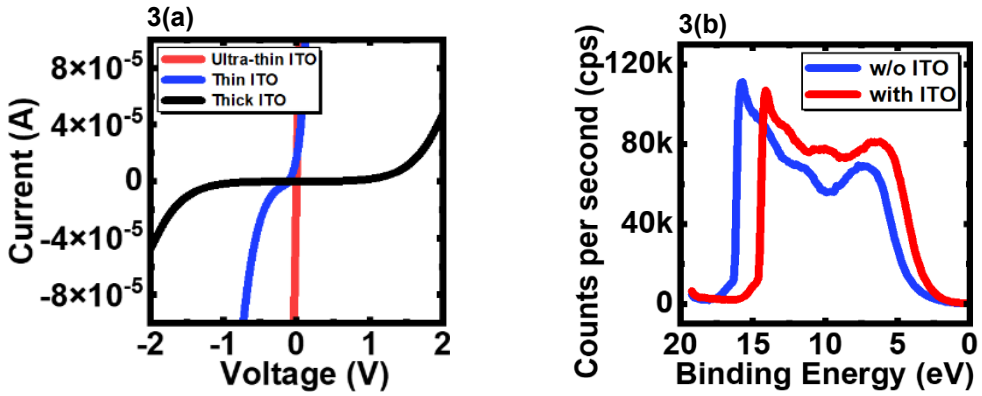


Fig. 3. (a) I-V of SBDs with different ITO thicknesses after PMDA at 950 °C (b) UPS Spectra of samples with and without ITO after PMDA at 950 °C.

The deposited thickness of ITO had a notable impact on the ohmic behaviour of the sample. This could be due to the conductive nature of the ITO interlayer which was deposited prior to metallization. Another reason could be that the ITO interlayer was responsible in passivating the interface and surface states which could have lowered Φ_B at the MS interface as deposited [3]. This would have a significant correlation to the overall extracted SCR [5]. Results from ultraviolet photoelectron spectroscopy (UPS) analysis indicated a slight decrease in the work function of the silicide, as shown in Fig. 3 (b) above. This further supports the role of the ITO interlayer in lowering the Φ_B as deposited since the work function of the metal Φ_M is closely related to the Φ_B [4].

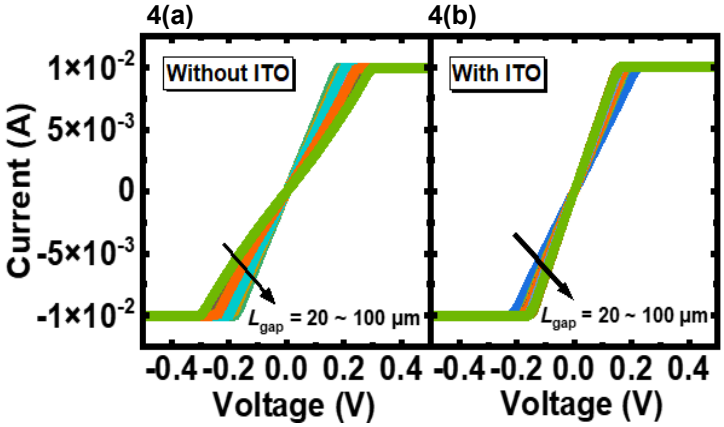
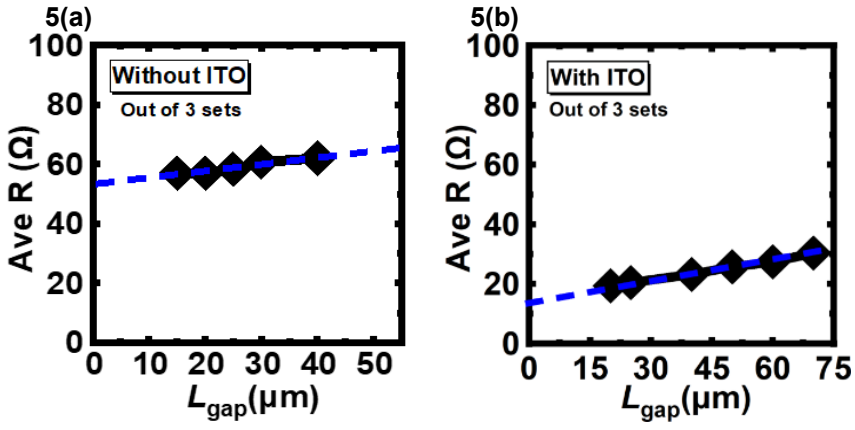


Fig. 4. I-V Measurements of CTLM structures with 20 – 100 μm gap spacings (a) without ITO interlayer and (b) with ITO interlayer.



ρ_c 2.5 × 10^{-6} Ω·cm^2 ρ_c 6.9 × 10^{-7} Ω·cm^2

Fig. 5. Ave R vs Gap out of 3 sets of CTLM structures (a) without ITO interlayer and (b) with ITO interlayer.

Electrical measurements (I-V) on the CTLM structures (top-to-top) with varying gap spacings of 20-100 µm were measured as shown in Fig. 4 (a-b). There was an observable decrease in the steepness of the I-V curve which correlates to a reduced contact resistance with the incorporation of the ITO interlayer. The results extracted out of 3 CTLM sets revealed a ρ_c of ~ 10^{-7} Ω·cm^2 with the ITO interlayer, leading to a significant reduction by almost one order of magnitude as compared to samples without ITO [Fig. 5 (a-b)]. The conductive nature of the deposited ITO interlayer could have also provided additional carriers which would have helped improve carrier injection across the MS interface. Additional carriers to present at the MS interface could enhance tunnelling across the interface. Another contributing factor could be the passivating nature of ITO. The passivating nature of the film could have reduced surface states and minimized fermi-level pinning. This would then lower charge trapping and could improve carrier injection and reduce contact resistance [3]. However, more studies on the role of ITO can be further investigated in future work. Combining the beneficial physical and electrical properties of the conductive ITO interlayer incorporated had assisted in the formation of better low SCR contacts to SiC.

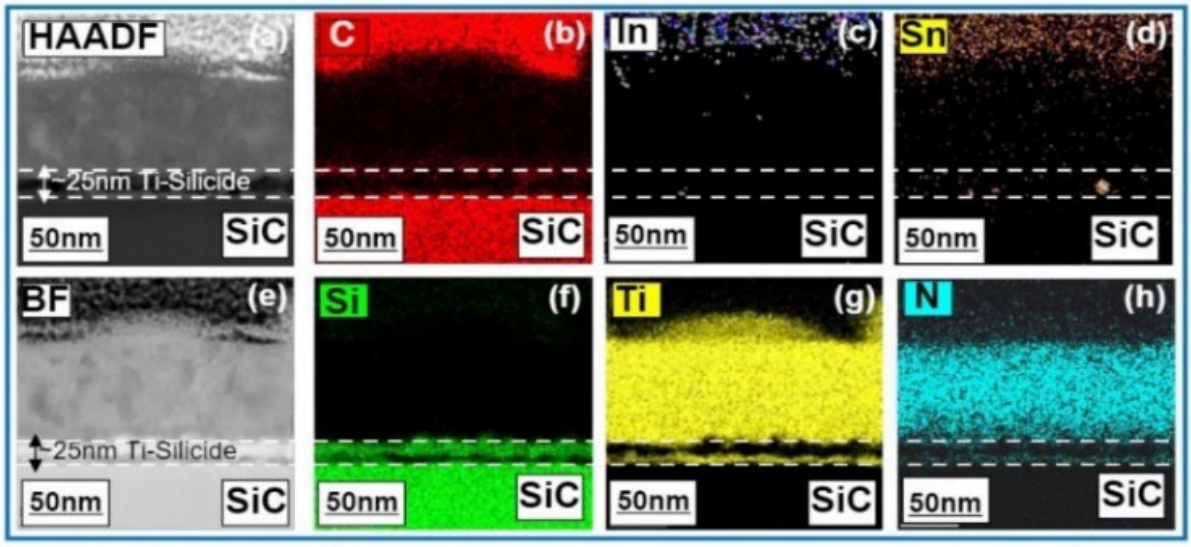


Fig. 6. (a-h) TEM-EDX with colour mapping of MS interface after 950 °C PMDA.

Intermetallic diffusion and silicide formation at the MS interface after 950 °C PMDA was investigated with Transmission Electron Microscopy (TEM-EDX) colour mapping as illustrated in Fig. 6 (a-h). The silicide layer was measured to be ~ 25 nm after PMDA due to the annealing conditions used. We observed the clear formation of $TiSi_2$ phase in the sample which predominantly forms the ohmic contact to the n-type SiC. An absence and clear out diffusion of carbon atoms from the silicide layer was also observed. This out diffusion could have been further promoted by positively charged indium atoms from the ITO interlayer. Previous studies have found that Indium may form complexes with carbon which could have increased the rate of carbon out diffusion [10]. These carbon vacancies which are formed after PMDA can serve as electron donors, potentially contributing to the improvement in ohmic contact formation, thereby achieving a lower SCR value. This reported value indicates a relatively low SCR as benchmarked in Fig. 7 [6-9].

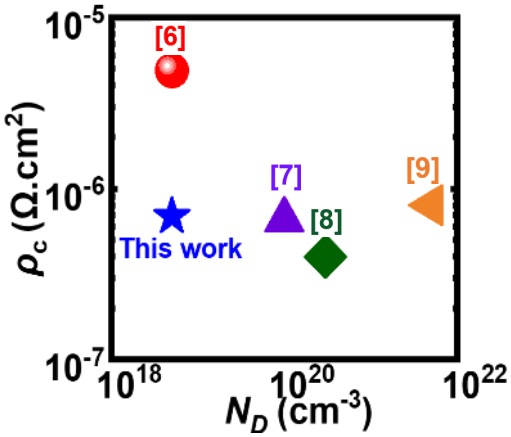


Fig. 7. Benchmarking of this work with previous studies on highly doped n-type regions.

Conclusion

In this work, an ITO interlayer for ohmic contact enhancement was studied to n-type SiC. We have demonstrated that the incorporation of ultra-thin conductive ITO at the MS interface as an interlayer material, had reduced the SCR by almost 1 order of magnitude to ρ_c of ~ 6.9×10^{-7} Ω·cm^2 on n-type SiC. Careful selection and optimization of the interlayer was critical to achieve favourable ohmic contacts. This was achieved through the reduction of Φ_B as deposited. In addition, carrier injection was promoted through the incorporation of a conductive interlayer at the MS junction. Furthermore, a low SCR was also achieved through the controlled promotion of carbon out diffusion by the ITO interlayer.

Acknowledgement

This work was supported by A*STAR (Agency for Science, Technology and Research Singapore), under Grant No. A20H9A0242.

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