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Trench Etch Processing for SiC Superjunction Schottky Diodes

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Abstract. This study focuses on the trench etching process for the fabrication of SiC Superjunction Schottky diodes, utilizing an ICP-RIE technique. Through a series of experiments, we optimized the etching parameters, including ICP power, RF power, and SF_6 gas flow rates, to achieve etching rates ranging from 157 nm/min to 372.1 nm/min. Additionally, the study identified the performance of the hard mask as a critical issue during the etching process, which was improved by reducing the RF power below 80 w. The deepest trench achieved reached a depth of 21 μm at 75 w RF power, 1000 w ICP power and 40 sccm SF_6, confirming the feasibility of this approach for fabricating high-performance SiC superjunction devices.

Introduction

Silicon carbide (SiC) has increasingly replaced silicon devices in power semiconductor applications due to its superior physical and chemical properties [1]. SiC unipolar devices, such as SiC Schottky diodes and metal-oxide-semiconductor field-effect transistors (MOSFETs), exhibit faster switching speeds and lower switching losses compared to their bipolar silicon (Si) counterparts within the current commercialized range of 400V to 3300V [2], [3]. However, at voltages above 3300V, the on-state voltage drop of a SiC unipolar device is high compared to Si bipolar devices of equivalent blocking voltage, due to the absence of conductivity modulation and the high resistance in the thick drift region [4]. Superjunction (SJ) MOSFETs that comprise of alternating, charge-balanced p-type and n-type columns, offer lower device resistance at a given breakdown voltage in exchange for higher output capacitance and hence slower switching. However, the common multi-epitaxial growth method [5] used in Si SJ fabrication is impractical in SiC due to limited implantation depths. Therefore, SiC superjunction MOSFETs [6] and Schottky diodes [7] have been produced using a trench etch and refill process, which overcomes these limitations by trench etching and ion implantation along the trench walls, effectively increasing the implantation depth. These trenches then need to be refilled with dielectrics, such as silicon dioxide (SiO_2), finely tuned so additional charge states don't interfere negatively with the charge balancing principle.

In this study, we show that, because of changes in air flow in the chamber, the etch rate significantly decreases when the trench width is reduced to less than 10 μm. This trend highlights the importance of refining trench etching techniques for narrow and deep trench fabrication, as precise trench quality directly impacts the performance of superjunction devices. The challenge of maintaining high etch rates while ensuring trench depth uniformity and sidewall smoothness remains a key area of research, as these factors directly affect the electrical characteristics of the device, such as charge balance and breakdown voltage.

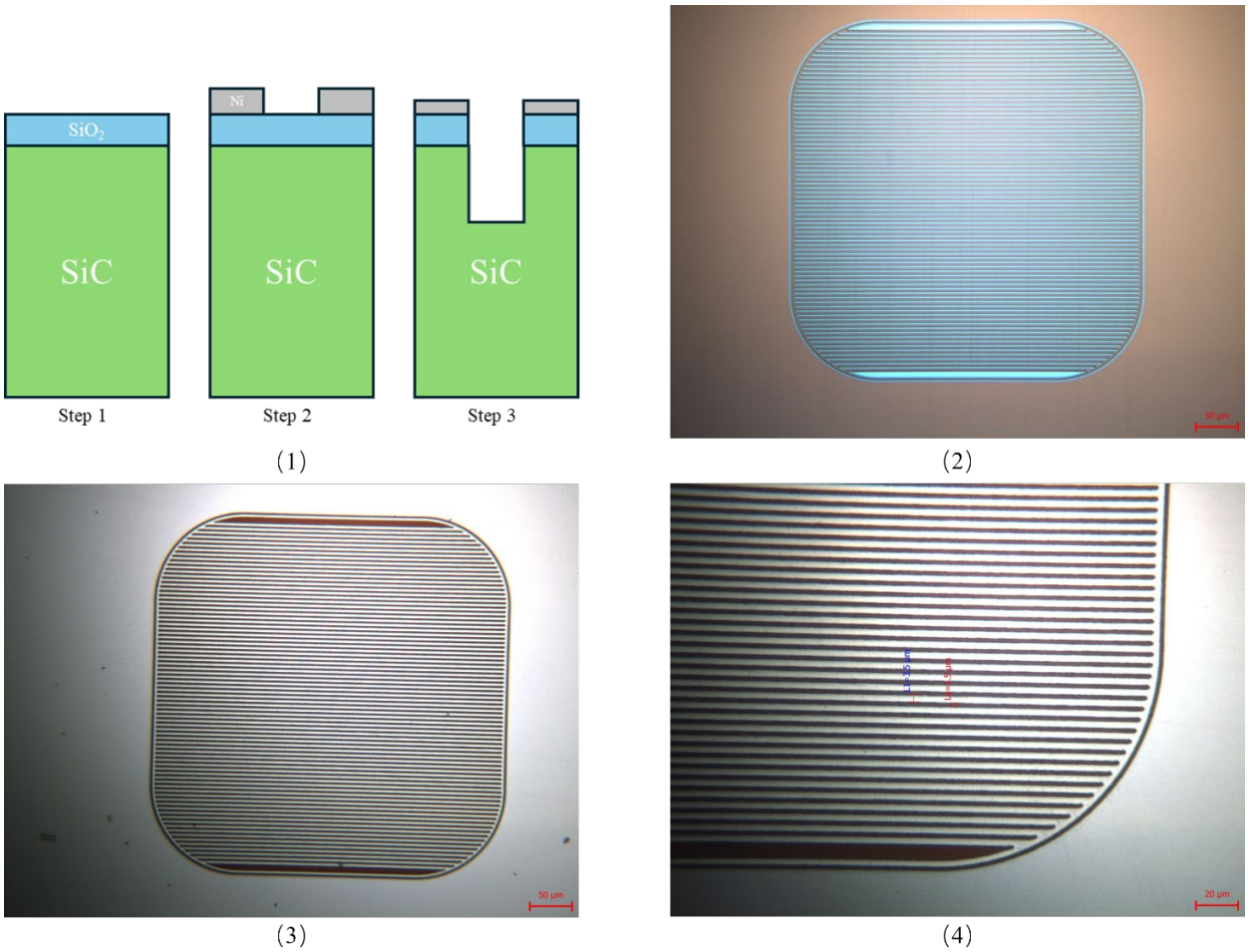


Fig. 1. (1): Flow chart for trench etching using a Ni + SiO_2 hard mask; (2) microscope image of Schottky diode active region after photolithography, amber color represents sample surface and light blue represents photo resist; (3) & (4) overlook and conner microscope image after metal lift off, white represents Ni and dark brown represents sample surface.

Methodology

Samples were fabricated on 1.5×1.5 µm square 4H-SiC chips that had a 100 µm thick, lightly n-type doped epilayer grown on top of it, with the process flow illustrated in Fig. 1.1. After completing a full RCA cleaning sequence (HF(1:10), SC-1, HF (1:10) and SC-2), a 250 nm thick blanket layer of silicon dioxide (SiO_2) was deposited on the sample surface. Photolithography was then performed as shown in Fig. 1.2, followed by sputter deposition of 700 nm of nickel (Ni). Dimethyl sulfoxide (DMSO) and acetone were used for metal lift-off to form the metal mask on the sample surface (shown in Fig. 1.3 & 1.4). The use of this composite mask of SiO_2 and Ni was primarily to prevent nickel from directly penetrating the SiC surface during sputtering, thereby avoiding metal contamination. Additionally, the nickel mask prevents high-energy fluorine ions from penetrating the SiO_2 film and diffusing to the SiC surface during dry etching [8]. In the manufacture of Schottky diodes, the remaining mask also serves as a mask for ion implantation, thus eliminating errors associated with repeated alignment in subsequent processes.

A Corial 210IL ICP-RIE etcherwas used, with the chiller temperature fixed at 0°C. In SiC, there are strong covalent bonds between silicon and carbon. The mainstream approach for ICP-RIE dry etching employs a fluorine-based plasma, in this experiment is sulphur hexafluoride (SF_6) consisting of a mix of oxygen (O_2) and argon (Ar) gases [9]. The main chemical reaction involved during etching process are [10]:

$$Si + xF \rightarrow SiF_x, \qquad x = 1 - 4$$

$$C + xF \rightarrow CF_x$$

The addition of oxygen not only promotes the other way of volatilization of carbon atoms, forming CO, CO_2, and COF_2, which enhances the etching rate [11]; but also leads to the formation of an SiF_xO_y layer on the trench sidewalls due to reactions between O ions and the F ions with Si atoms in SiC [12]. This SiF_xO_y layer, being more ion-attractive than SiC, results in uneven chemical reaction rates at the trench corners, an effect which has been shown to create micro-trenches [13]. These micro-trenches increase the electrical field on super junction structure during voltage blocking and affect the charge balance and the complexity of ion implantation into the sidewalls [14]. Consequently, we discontinued the etching approach using O_2. While Ar, as a stable inert carrier gas, which also contributes to enhancing the smoothness of the etched surface [15] and He which effectively reduces the heat generated during etching and serves as an excellent medium for SF_6 ionization [16] are used in recipe.

The first experiment investigates the relationship between trench width and etch rate. Four different etching recipes were applied to the samples, with specific parameters detailed in Table 1. he second experiment focuses on optimizing deep trench etches for openings less than 5 μm, which are representative of the dimensions expected in the final SJ device structure (around 3.5 μm). After etching, the cross-sections of the samples were captured using a Zeiss Gemini scanning electron microscope (SEM), and the depth, width and sidewall angles of the trenches were recorded.

Table I. Parameters for Each Etching Recipe.

Sample No.	ICP Power [w]	RF Power [w]	Pressure [mT]	SF6 [sccm]	Ar [sccm]	He [sccm]	Time [s]
1	1000	60	10	10	85	20	1800
2	1000	100	10	10	85	20	900
3	800	100	10	10	85	20	900
4	800	100	10	10	85	20	1800

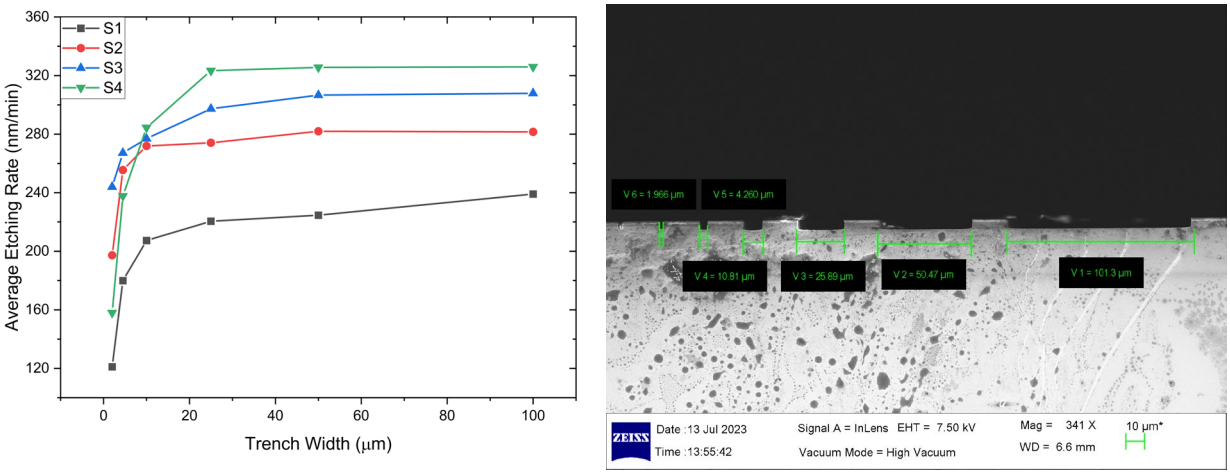


Fig. 2. Left: Calculated average etching rate of Sample 1-4 against various trench widths; right: example SEM image of Sample 3 after etching.

Results and Discussion

Fig. 2 shows the SEM image of the trench cross-section for Sample 3 (see Table I) after etching, along with the average etching rate calculated from the measured trench depth. It is evident that, when the trench width decreases below 10 µm, the etching rate significantly drops. This indicates that, in a real power SiC SJ device, batch etching is necessary when there are trenches with large width variations in the device. We selected the etching recipe used for Sample 4 to fabricate the Superjunction active region [3]. In this experiment, the observed region comprises trenches with a width of 3 µm and mesas with a width of 2 µm, as shown in Fig. 1.2 to 1.4. Ideally, the trenches in the active region should have smooth walls and rounded corners, and each trench should be as uniform as possible to facilitate particle implantation and ensure uniform electric field distribution under reverse bias. Considering the anisotropy present during trench etching, the etching process should not excessively reduce the width of the mesas, as they play a crucial role in current transport. The cross-section of the resulting trench is shown in Fig. 3, with an etch rate of 178.3 nm/min. Notably, one important issue observed was the darkening of the metal mask on the sample surface after etching, as shown in Fig. 4.1. Even after a 6-hour wet etching in hydrofluoric acid (HF) and non-dilute aqua regia ($HNO_3 + 3\,HCl \rightarrow NOCl + Cl_2 + 2H_2O$), some black residue remained on the sample (see Fig. 4.2). To investigate this residue, Energy-dispersive X-ray (EDX) elemental spectral analysis was conducted on the post-etched surface (point a in Fig. 4.3) and the acid-cleaned sample (points b, c, d in Fig. 4.4). According to the elemental composition displayed in Fig. 4.5, points a and b appear to be the same substance which is the rest Ni mask and trace amounts of nickel fluoride (NiF_2). Point d is the sample surface of silicon carbide, while point c consists mainly of nickel and silicon, suggesting the formation of nickel silicide due to temperature increases during etching with the following reaction [17]:

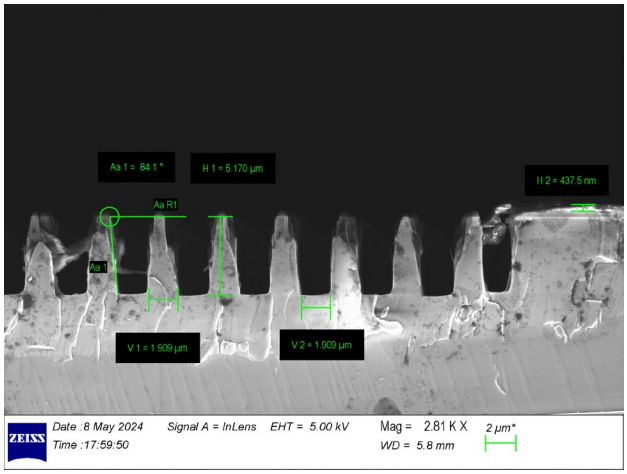


Fig. 3. Cross section of trench after 30 min etching under recipe 4.

$$SiC + Ni \xrightarrow{high\ temperature} NiSi + C$$

Nickel silicide (NiSi), being highly stable, makes the residues difficult to completely remove, leading to metal contamination in subsequent device production. During the etching process, contact between silicon and nickel is unavoidable. To address this issue, reducing the sample temperature is crucial. One of the main sources of heat leading to increased sample temperature is ion bombardment from plasma [18]. In the ICP-RIE system, reactive ions (fluorine ions from SF_6 in this experiment) are accelerated towards the sample surface by the electric field in the reactor. The kinetic energy of these ions, especially under the influence of a bias voltage, transfers to the substrate upon impact, resulting in heating. However, under purely thermal conditions, the formation of NiSi typically requires temperatures in the range of 500–600 °C. In this experiment, we were unable to directly measure the surface temperature during etching, though it is likely that the wafer did not reach such high values. We hypothesize that the combined effect of high-energy ion bombardment and the presence of chemically active species in the plasma may facilitate a plasma-enhanced reaction pathway, enabling the formation of NiSi at lower effective temperatures. Based on this hypothesis and consistent experimental observations, we chose to reduce the RF power to lower the ion energy, thereby controlling the thermal load during etching and effectively minimizing NiSi formation. Fig. 5.1 shows the surface of the sample etched for 30 minutes under an ICP power of 800 W, an RF power of 60 W, and an SF6 flow rate of 10 sccm. No significant discoloration was observed on the surface, but due to the reduced RF power, the etching rate decreased to 157 nm/min, as shown in

Fig. 5.2. To enhance the etching rate, we kept the RF power and increased the ICP power to 1000 W and adjusted the SF_6 flow to 20 sccm and 40 sccm, which resulted in increased etching rates of 163.5 nm/min and 178.2 nm/min, respectively. Based on these rates, we performed a 45-minute etch with an SF6 flow rate of 40 sccm, aiming for a trench depth exceeding 7 μm. However, the average etching rate dropped sharply to 133.6 nm/min. We hypothesize that this is due to the relatively low RF power, which is insufficient to effectively etch deeper trenches. Therefore, we gradually increased the RF power. Fig. 6.1 shows a trench with a depth of approximately 10 μm after 30 minutes of etching at an RF power of 75 W, with an average etching rate of 372.1 nm/min.

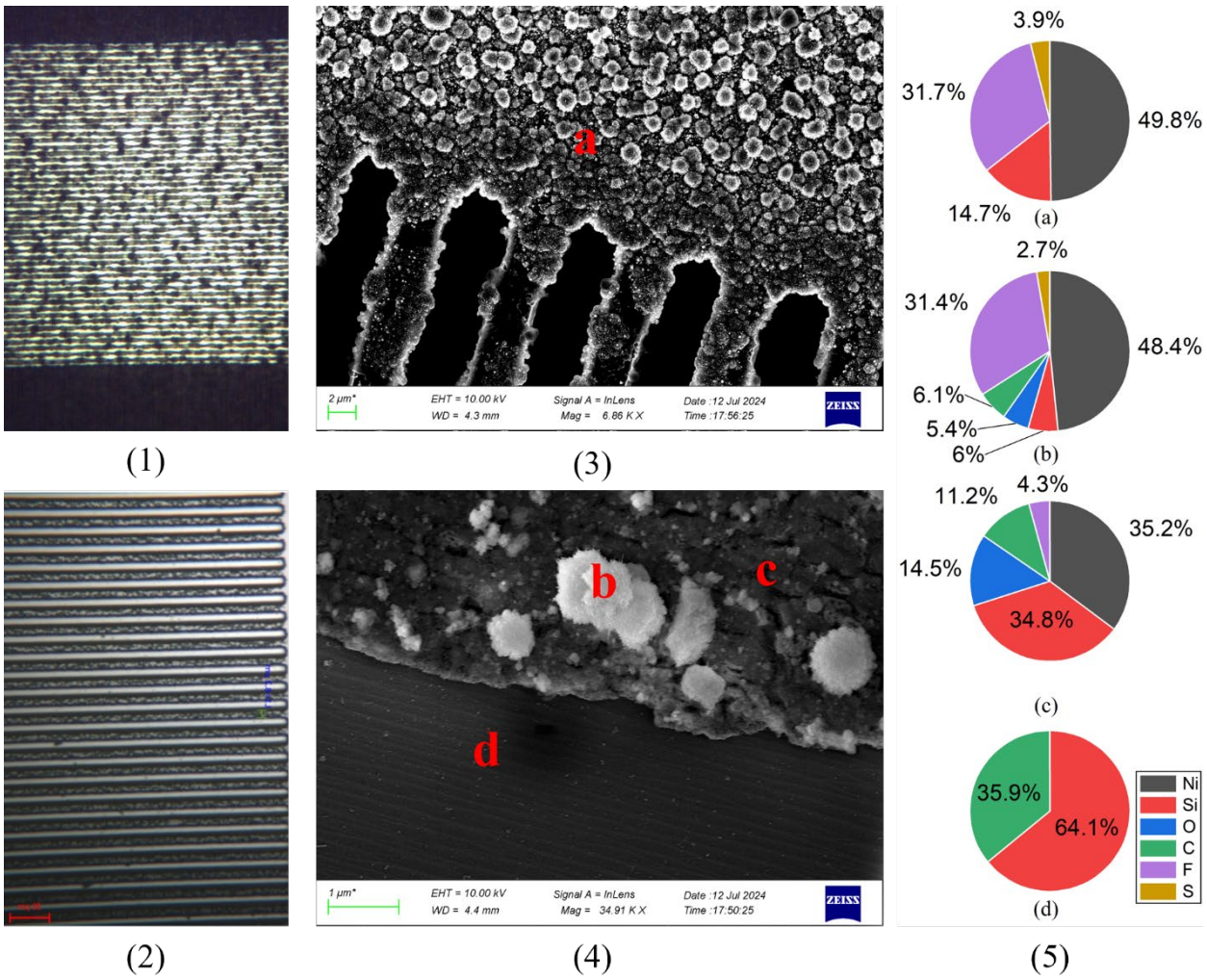
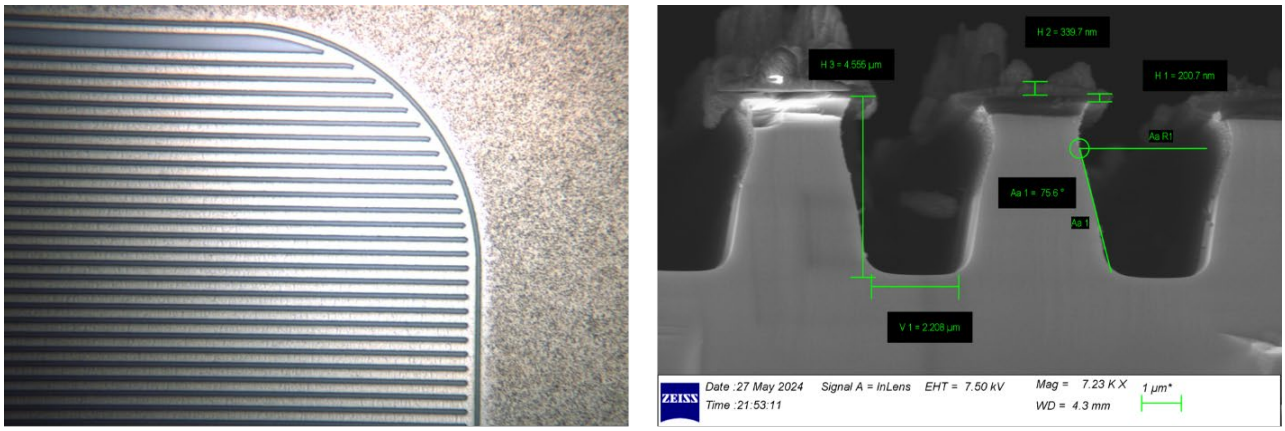


Fig. 4. (1) & (2) shows sample (in Fig. 3) surface outlook under microscope before and after wet etching by acid; (3) & (4) shows the sample surface under SEM respectively; (5) shows the element composition of points from point a to d by EDX.



(1) (2)

Fig. 5. The Sample after 30 min etching under ICP Power = 800 W, RF Power = 60 W, SF6 = 10 sccm. (1) sample surface by microscope; (2) sample cross section by SEM.

To test the controllability of this etching recipe, we performed a 21-minute etch, aiming to fabricate a 7 μm deep trench. The result, as shown in Fig. 6.3, indicates a trench depth of 6.913 μm, confirming process repeatability. At the same time, we observed curvature at the upper part of the trench, likely due to under-cutting caused by SF_6 on the high-resistance mask (such as the nickel used in this experiment). One feasible method to reduce the impact of under-cutting on the structure is to increase the thickness of the mask. As shown in Fig. 6.4, by significantly increasing the thickness of SiO_2, the trench depth remained 7 μm after etching, but the curvature at the trench opening was noticeably reduced. Finally, we conducted a longer etching process, and the deepest trench achieved reached a depth of 21 μm with the average etching rate 350nm/min.

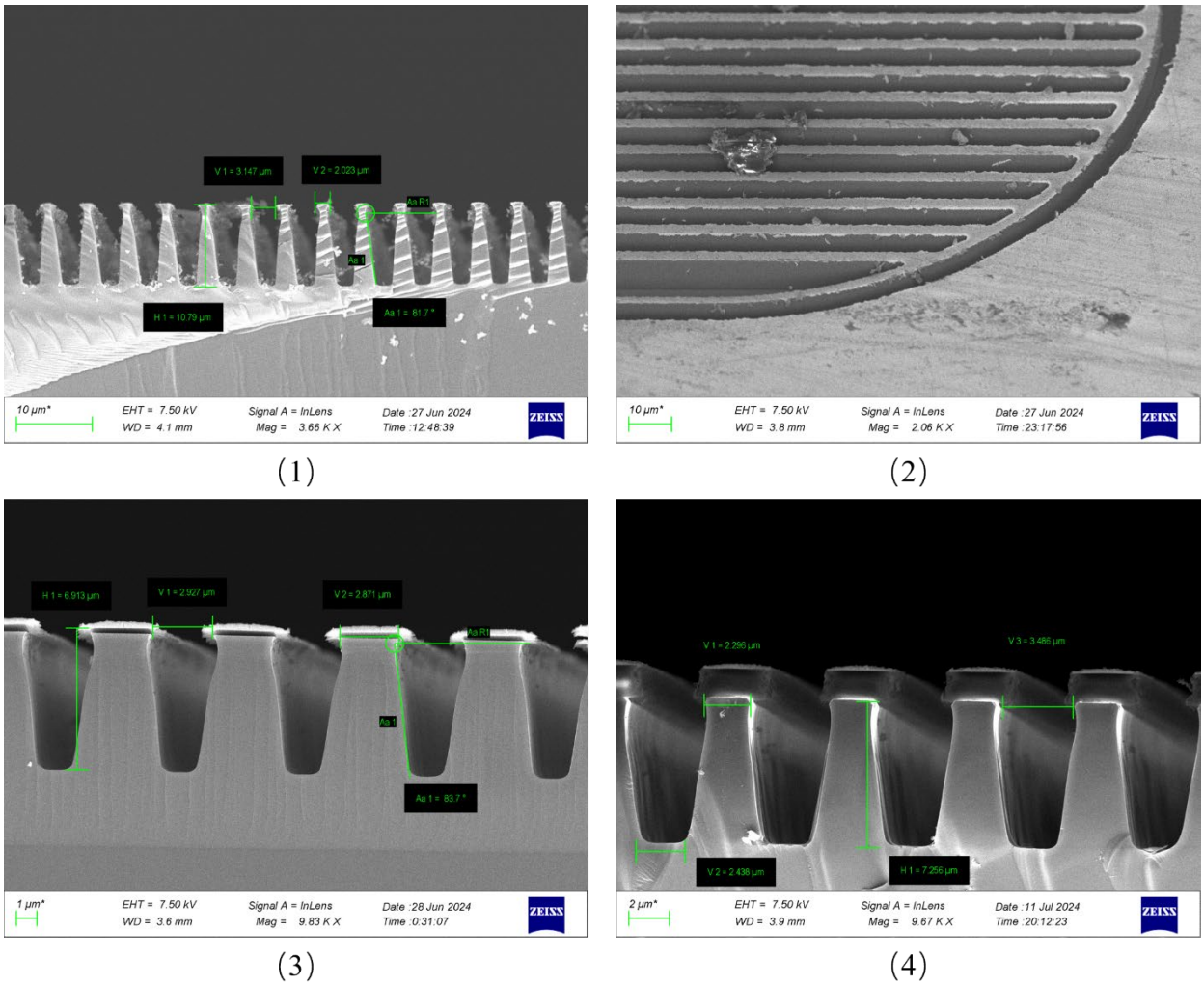


Fig. 6. SEM image: (1) Cross section of trench after 30 min etching under ICP Power = 1000W, RF Power = 75W, SF_6 = 40 sccm. (2) The sample surface of sample in Fig.6.1. from 45° angle. (3) Cross section of trench with same recipe after 21 min etching. (4) Cross section of trench with same recipe and thicker SiO_2 mask.

Summary

In this paper, we successfully demonstrated the fabrication of deep trenches in 4H-SiC wafer for Superjunction Schottky diodes using ICP-RIE etching techniques. By optimizing the etching parameters, particularly the ICP and RF power levels and SF_6 flow rates, we achieved a maximum etching rate of 372.1 nm/min and trench depths of up to 21 µm. The experiments revealed that trench width significantly influences the etching rate, with a notable decrease when the width is below 10 µm. Furthermore, the formation of nickel silicide during the etching process was addressed by controlling the RF power, preventing excessive heating. These findings offer a robust foundation for further improving the fabrication of SiC super junction devices. Future work will focus on refining the trench profile and addressing the remaining challenges associated with under-cutting and sidewall roughness.

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