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Gate Oxide Performance and Reliability on SmartSiC™ Wafers and the Influence of RTA Processing on Gate Oxide Lifetime

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Abstract. In this work, a comparison of standard bulk 4H-SiC epi wafers and Soitec's SmartSiC™ wafers as well as the influence of RTA processing was conducted. For this, MOS capacitors were processed using thermal gate oxide paired with a polycrystalline gate electrode. Subsequent high temperature steps were avoided until an RTA process was performed on some of these wafers. To investigate the oxide quality on all wafer and process splits, CV-, time-zero dielectric breakdown and constant-current stress time-dependent dielectric breakdown measurements were carried out. For the examination of bulk wafers and SmartSiC™, no relevant differences in terms of yield, oxide quality, interface state density and reliability were found. In contrast, RTA processes seem to create a shift in flat band voltage and also lead to a reduction in oxide lifetime. The V_{FB} shift could partially, but not completely, be explained by addition activation of dopants in the polysilicon electrode. The influence on the oxide reliability, however, is still unclear.

Introduction

With silicon carbide (SiC) power devices becoming more and more relevant in the electrification of the automotive sector as well as for renewable energies, a demand for more cost-efficient ways to manufacture these devices, in addition to a fabrication yield increase will be necessary. For this purpose, Soitec introduced its SmartSiC™ technology (see Fig. 1), which combines low resistivity polycrystalline SiC substrates with high-quality monocrystalline 4H-SiC top-layers, to minimize devices on-resistance and cost of ownership [1]. In this paper we evaluate the compatibility of this SiC engineered substrate with gate oxide fabrication in terms of capacitor yield, D_{it} and reliability. We also investigate the impact of including, or not, an RTA step in the capacitor fabrication process, for comparability to full MOS-transistor processes, where this step is necessary. The annealing step required on standard bulk SiC substrates to ensure good backside metal contact can be skipped on SmartSiC™ wafers [2] but the resulting lower dopant activation in the polycrystalline silicon gate electrode adversely impacts the gate oxide evaluation. For structured ohmic contacts with low resistivity on the epitaxial surface, RTA is still necessary.

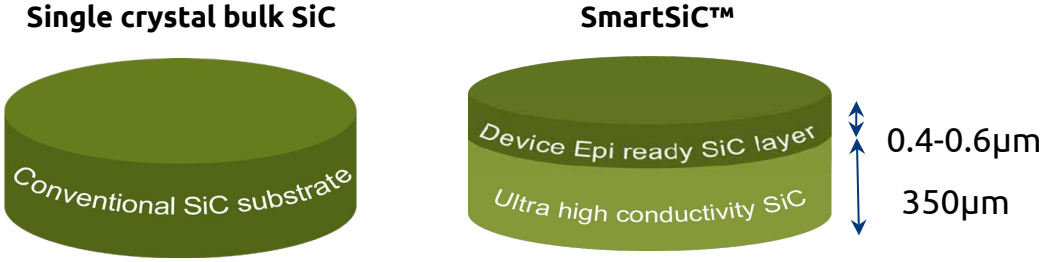

Fig. 1. Wafer types used for this study are standard 20 mΩcm single crystal bulk 4H-SiC (left) and SmartSiC™ engineered substrates composed of a layer of high quality monocrystalline 4H SiC on an ultra-high conductivity (> 5 mΩcm) polycrystalline SiC substrate. [3]

Sample Preparation

To be able to evaluate the performance and reliability of gate oxides on engineered SiC substrate (SmartSiC™) wafers in comparison to standard (bulk) 4H-SiC wafers and investigate the influence of RTA processing, a design of experiment with four major splits was implemented (see table 1).

The 150 mm wafers used had an epitaxial n-doped layer stack of a 1.0 µm, 10^{18} cm^{-3} buffer and a 10.5 µm, $9.5 \cdot 10^{15}$ cm^{-3} drift layer. The 52 nm gate oxide was thermally grown at 1300 °C and a 500 nm in-situ phosphorous-doped polycrystalline silicon layer was deposited at 570 °C as the gate electrode. To avoid high temperature steps other than the RTA after gate oxidation for selected wafers, a 600 nm thick field oxide was deposited using a plasma enhanced CVD process at about 250 - 300 °C. After the opening of the field oxide above the polycrystalline gate electrode via dry etching, the wafers A and C were processed in an RTA tool for 2 minutes at 980 °C in Argon atmosphere in order to establish comparability to full SiC MOS-transistor processes. To complete the front side process, a power metallization consisting of a Ti/Al/Ti stack was sputtered and structured above the vias in the field oxide. On the wafer backside, NiAl was deposited and an ohmic contact was created by laser annealing of all standard bulk 4H-SiC wafers (not needed on engineered SiC substrate [2]. A thick aluminum layer was then deposited on all wafers on the backside and a forming gas tempering for 30 minutes at 450 °C was performed.

Table 1. Wafer type and process split.

#	*Wafer type*	*RTA*
A	Standard bulk SiC	yes
B	Standard bulk SiC	no
C	Engineered SiC substrate	yes
D	Engineered SiC substrate	no

In parallel to these SiC MOS-Cap wafers, four Silicon dummy wafers with a 100 nm oxide layer underneath a 500 nm doped polycrystalline silicon layer were processed and characterized with regards to the sheet resistance R_{sh} of the polycrystalline layers before and after being processed in the RTA, via a four-point probe measurement.

Electrical Characterization

After the manufacturing of these MOS-Caps, several electrical characterization methods were used to determine the flat band voltage, breakdown properties and reliability on forty devices per parameter investigated.

On the largest capacitors with areas of 1.0 mm^2, 0.5 mm^2 and 0.316 mm^2 CV-measurements were conducted from +10 V to -20 V to determine the impact of the RTA. Fig. 2 (left) shows exemplary CV-curves at 100 kHz on wafer A. The tight distribution obtained on all capacitor sizes and on all wafers (not shown here) allows significant comparison between the various wafer flavors, using typical curves. Fig. 2 (right) shows typical quasi-static (QS), 100 kHz and 1 MHz back-and-forth CV-curves. The lack of hysteresis demonstrates the absence of slow traps. The only impact of frequency is the small shift between QS and higher frequencies (typical for the expected D_{it}) observed close to flat band capacitance.

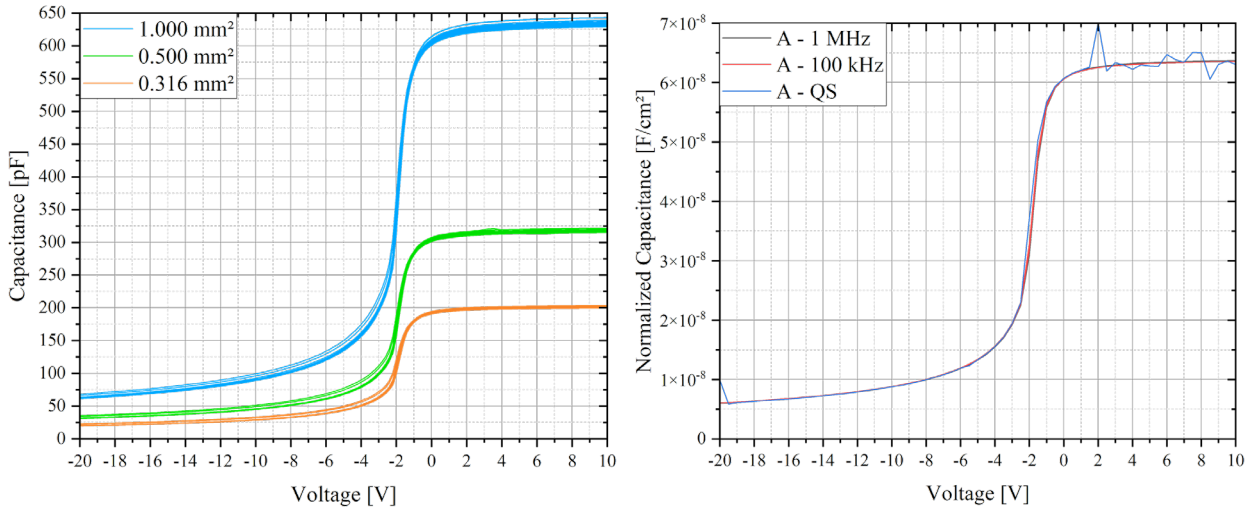

Fig. 2. 100 kHz CV measurement for three different capacitor sizes (left), and QS, 100 kHz and 1 MHz back-and-forth measurements (right) on wafer A.

The comparison of the capacitance characteristic of all tested wafers (see Fig. 3) makes obvious that the V_{FB} shift is linked to the thermal budget the gate stack (oxide and polysilicon electrode) was exposed to during processing, while there was no difference of substrate type used.

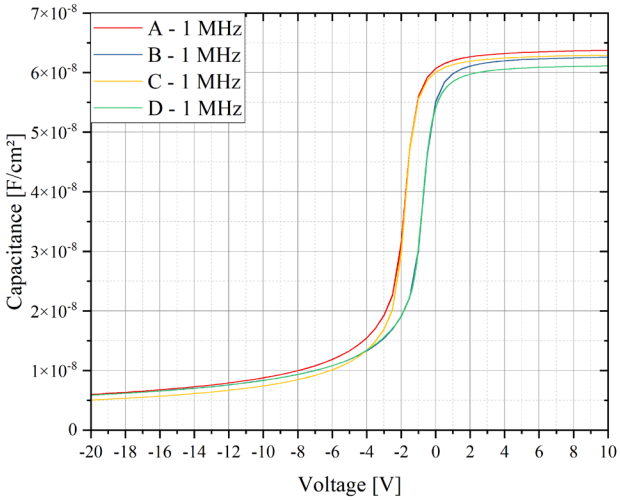

Fig. 3. Typical CV measurements at 1 MHz for all studied wafers, depicting a clear shift between wafer subjected to RTA and not.

We suspect that the dopant activation in the polycrystalline silicon electrode is not complete after Poly-Si deposition [4]. During the short RTA the active doping is estimated to be roughly doubled, partially leading to the observed V_{FB} shift of about 1.1 V. To support this theory, R_{sh} measurements were done after deposition of the doped polysilicon layer on the SiC process wafers and silicon dummy wafers via four-point probe measurement. The R_{sh} values extracted were about 25.5 Ω/sq. The silicon dummy wafers were again measured after RTA processing, producing an R_{sh} of about 13.5 Ω/sq. The same R_{sh} values were also calculated after electrical measurements of polysilicon meander structures on fully processed SiC wafers both with and without RTA. The entire origin of this large V_{FB} shift is still unclear.

The density of interface states/traps was extracted by both the Terman [5] (left) and high-low [6] (right) method for all four wafer and process splits, as shown in Fig. 4 and table 2.

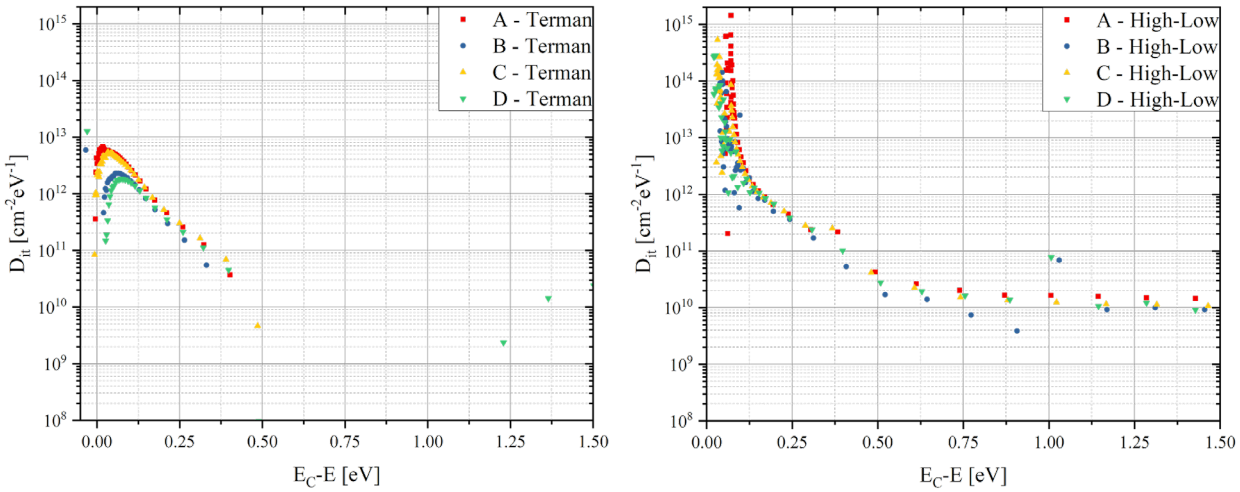

Fig 4. Interface trap density from the 4H-SiC conduction band (E_C) to 1.5 eV deep into the gap, evaluated with the Terman- (left) and High-Low- (right) method for both wafer types with and without exposure to RTA processing.

0.2 eV is suggested to be the limit of reliable D_{it} value extraction this close to the conduction band edge E_C [7]. For this reason, table 2 displays D_{it} values extracted from Fig. 4 at 0.25 eV (near E_C) and 1.5 eV (near mid-gap) to compare concentrations at the same energy level for all wafers. Extracted D_{it} values for both Terman and high-low method lie in a narrow range for wafers A-D. It is noticeable that neither the wafer type (bulk and engineered SiC substrate) nor the RTA process has any significant influence on the density of interface states or traps.

Table 2. D_{it} value comparison of both wafer types, with and without RTA, near the band gap E_C (0.25 eV) and near the mid-gap (1.5 eV).

D_{it} [1/cm²/eV]	Band energy depth from conduction band (E_C - E) [eV]			
	0.25 (near E_C)		1.5 (near mid-gap)	
	Terman	QS/HF	Terman	QS/HF
A	$2.90 \cdot 10^{11}$	$4.04 \cdot 10^{11}$	-	*noise (~ $1.0 \cdot 10^{10}$)*
B	$1.85 \cdot 10^{11}$	$3.33 \cdot 10^{11}$	-	*noise (~ $1.0 \cdot 10^{10}$)*
C	$3.00 \cdot 10^{11}$	$4.04 \cdot 10^{11}$	-	*noise (~ $1.0 \cdot 10^{10}$)*
D	$2.35 \cdot 10^{11}$	$3.64 \cdot 10^{11}$	-	*noise (~ $1.0 \cdot 10^{10}$)*

To determine the yield and breakdown voltage, TZDB (time-zero dielectric breakdown) measurements up to a current compliance of 10 mA were performed at different temperatures. Fig. 5 depicts the current density over electric field for forty 0.01 mm² devices each of the wafers A (left) and C (right) at room temperature (RT), 100 °C, 150 °C and 175 °C, with the different V_{FB} values taken into account by the calculation of the electric field.

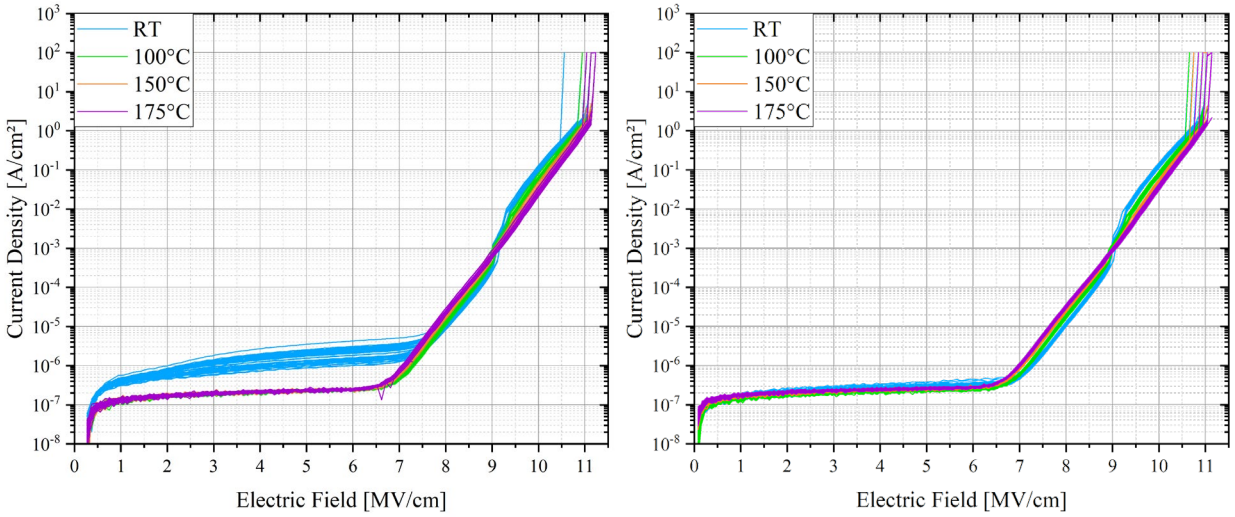

Fig. 5. Current density over electric field in the oxide layer from TZDB-measurements for both wafer A (left) and C (right) on 0.01 mm² capacitors.

Above 6.25 MV/cm the Fowler-Nordheim tunneling dominates the charge transport through the oxide and at about 8.75 - 9.00 MV/cm the kinks in the curve at RT and 100 °C suggest the beginning of impact ionization due to hole injection at the gate electrode [8, 9]. At 150 °C and 175 °C this effect gets pushed to higher fields, not reached here, due to lattice vibrations [10]. When comparing exemplary curves of different wafer types as well as with and without RTA processing in Fig. 6, no noticeable differences can be noticed in the current density over electric field performance for RT nor for 175 °C.

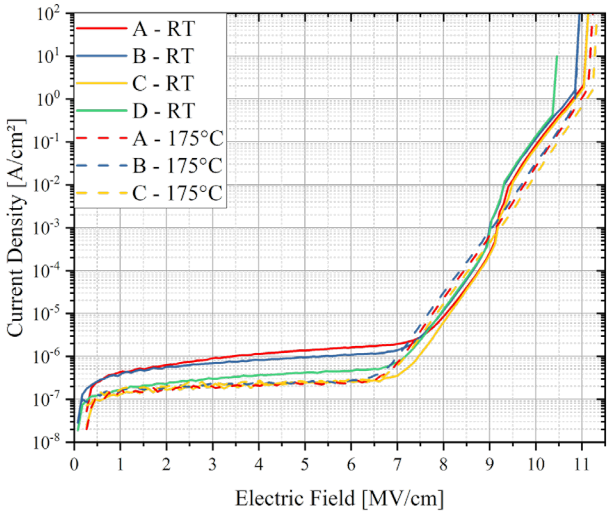

Fig. 6. Current density over electric field comparison of wafers A, B, C, and D. The plot shows no significant diversions in behavior for the three wafers at the same temperature, proposing that neither the influence of the RTA, nor the wafer type affects the breakdown properties seen in TZDB measurements.

Due to constraints in time and resource availability, high temperature TZDB and CCS-TDDB measurements on wafer D could not be conducted in the scope of this work. In terms of capacitor yield, no notable difference is seen between standard bulk wafer A and engineered SiC substrate wafer C. Wafer B, which has not seen the RTA process shows a significant B-mode (intermediate breakdown mode) failure rate, as shown in Fig. 7.

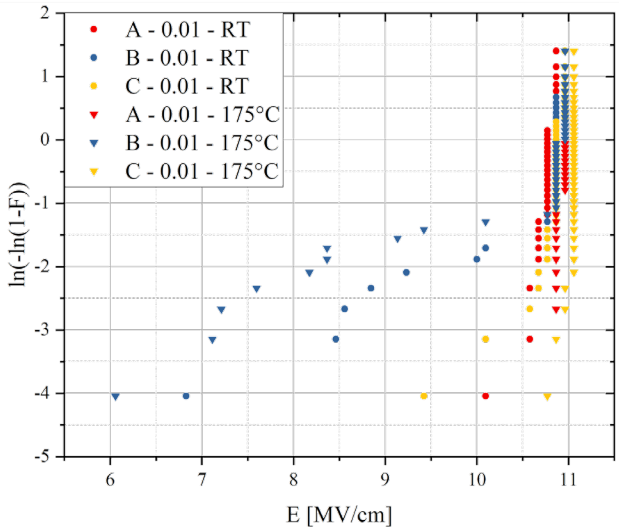

Fig. 7. Weibull plot depicting the yield according to maximum electrical field reached during TZDB measurements on wafers A, B, and C on 0.01 mm² capacitors. There seem to be a few earlier failures for wafer B, but no noticeable difference between A and C.

For most sizes on all three wafers, over 10 MV/cm were reached during the TZDB measurement of 40 devices per size and wafer (Table 3). The failures on wafer B occur on the 0.01 mm² devices at RT and on both 0.01 mm² and 0.00316 mm² capacitors at 175 °C. This trend does not correlate with expectations relating a lower yield with larger device sizes induced by randomly distributed defects (such as crystal defects in the SiC) and could stem from processing issues or edge effects.

Table 3. Yield values for the test-pass-condition of over 10 MV/cm before reaching the current compliance for wafers A, B, and C on three device sizes each.

Capacitor Size [mm²]	E > 10 MV/cm at RT			E > 10 MV/cm at 175 °C		
	A	B	C	A	B	C
0.0316	100 %	100 %	100 %	100 %	100 %	100 %
0.01	100 %	83 %	98 %	100 %	85 %	100 %
0.00316	100 %	100 %	100 %	100 %	68 %	100 %

When comparing the quality of gate oxides, not only TZDB, but also reliability focused measurement methods like time-dependent dielectric-breakdown (TDDB) are of great interest. To be able to confidently calculate the charges to breakdown (Q_{BD}) for these wafers, the constant-current stress (CCS) TDDB was chosen. The CCS-TDDB was performed at RT and 175 °C on three different capacitor sizes (0.0316 mm², 0.01 mm², and 0.00316 mm²) and four different current densities (50 mA/cm², 100 mA/cm², 200 mA/cm², and 300 mA/cm²). Fig. 8 displays the Weibull plots of wafers A and B (left) and wafers A and C (right) for the three capacitor sizes each, measured at RT with an injected current density of 100 mA/cm². A clear shift in oxide lifetime is noticeable between A and B (the standard bulk wafers with and without RTA respectively). This significant reduction in reliability could be explained by the above-mentioned, but not fully understood, influence of the RTA and partially by its effect on the concentration of activated phosphorous ions inside the polycrystalline silicon gate electrode, by influencing the electric field at the gate/oxide interface and the carrier injection mechanism. The comparison of wafers A and C, the standard SiC wafer and engineered SiC substrate, on the left of Fig. 8 shows an overlapping of the intrinsic population for all device sizes independent on the wafer type. This leads to the conclusion, that there is no difference in oxide quality and reliability between these two wafers. The origin of the significantly better yield on wafer C (much lower extrinsic failure rate) is not identified yet.

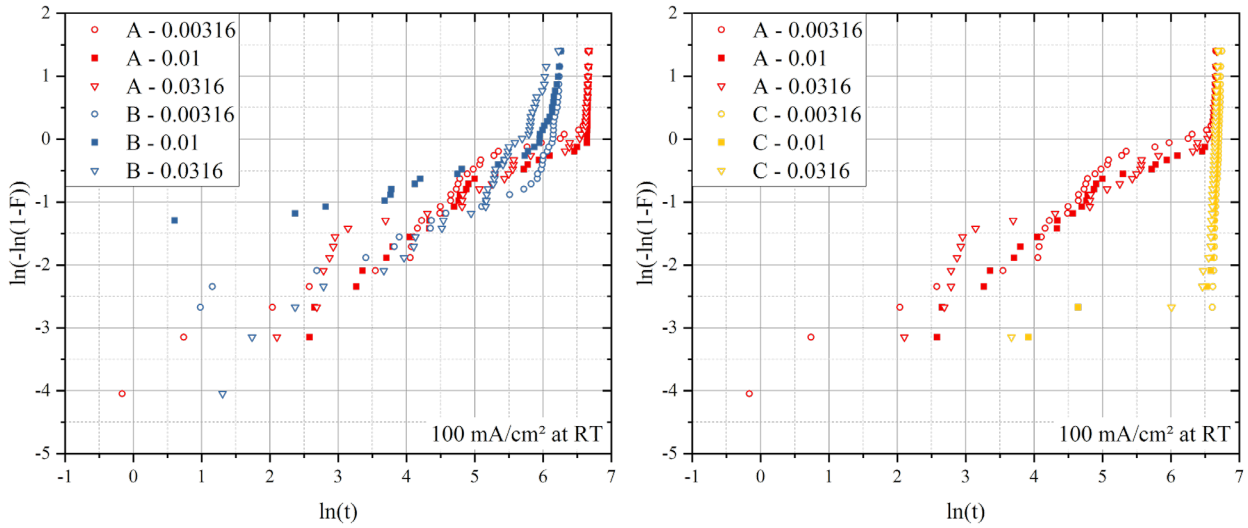

Fig. 8. Weibull plots of gate oxide lifetime after CCS-TDDB at RT with a current density of 100 mA/cm² for wafers A and B (left) as well as wafers A and C, to investigate the influence of RTA processing and wafer type on the MOS reliability.

To validate the conclusions of the RT measurements above, Fig. 9 present results from CCS-TDDB with the same injected current density of 100 mA/cm² but at 175 °C. Consistent results are obtained, with a significant reduction of both the lifetime and the B-mode failures compared to RT.

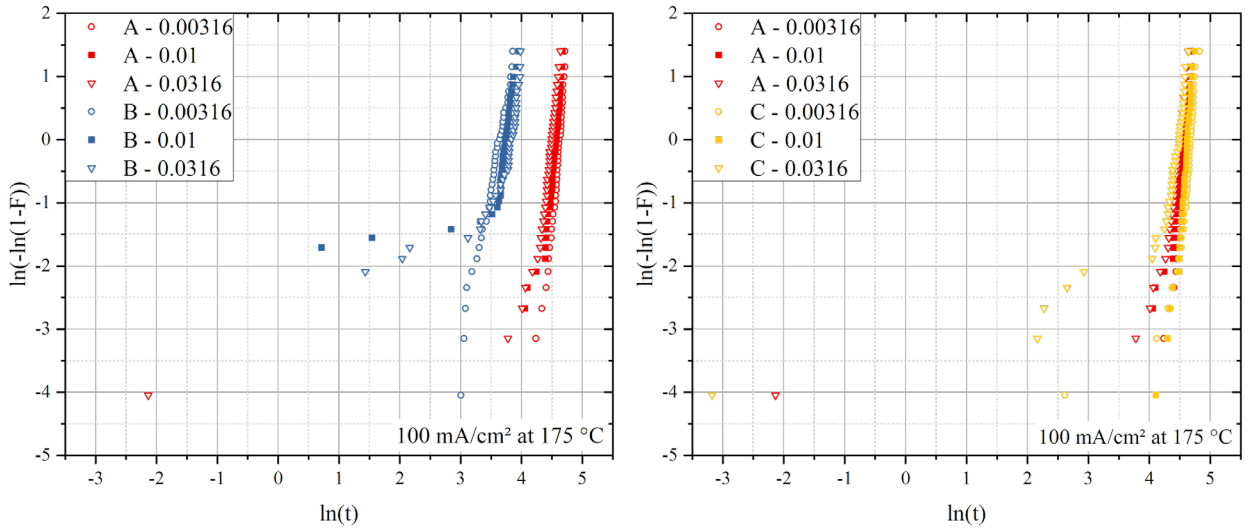

Fig. 9. Weibull plots of gate oxide lifetime after CCS-TDDB at 175 °C at an injected current density of 100 mA/cm² for wafers A and B (left) as well as wafers A and C (right).

To evaluate the oxide lifetime of wafers A, B, and C, an assessment of Q_{BD} for each measurement condition is shown for the 0.01 mm² capacitors at a failure rate of 63 %. Fig. 10 displays Q_{BD} over current density for both RT (left) and 175 °C (right) and it can be noticed that the shift to shorter lifetimes in the Weibull plot for wafer B in comparison to A and C translated to a major reduction in Q_{BD} of 35 % to 75 %, depending on temperature and injected current density.

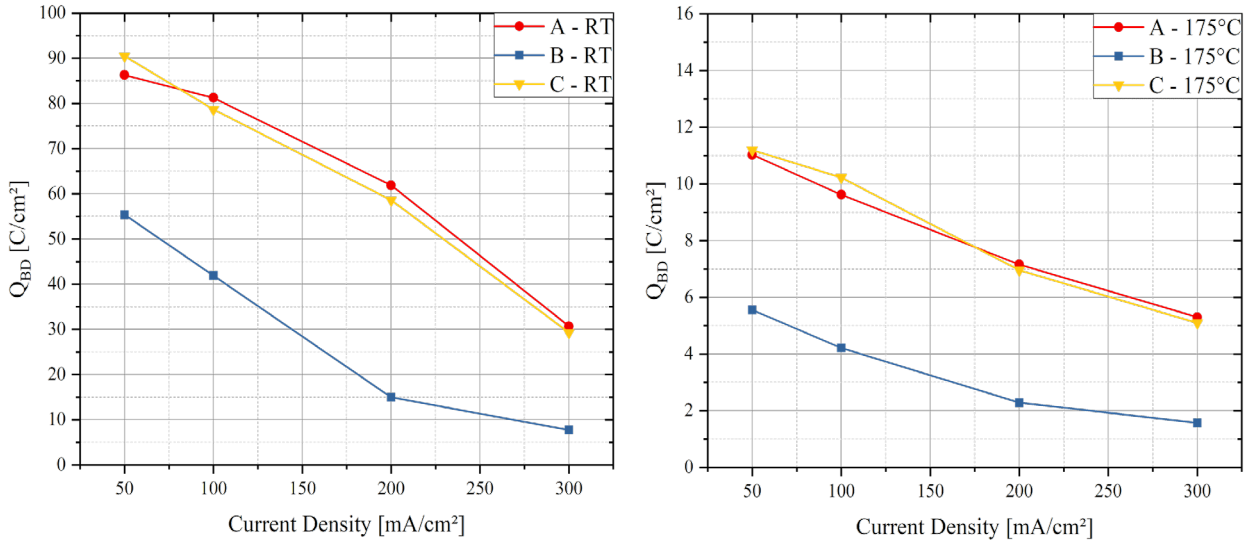

Fig. 10. Q_{BD} over injected current density at both RT and 175 °C displayed for 0.01 mm² devices for wafers A, B, and C.

Conclusions

We conducted a thorough investigation of thermally grown gate oxide quality in terms of flat band voltage, interface states density, breakdown behavior and yield, as well as oxide reliability on both standard bulk 4H-SiC and SmartSiC™ wafers. We concomitantly evaluated the impact of including, or not, an RTA step in the test capacitors fabrication process. Our results non-ambiguously lead to the following conclusions: (i) Gate oxides grown on standard bulk 4H-SiC and SmartSiC wafers exhibit the same V_{FB}, D_{it}, failure rate, breakdown field and Q_{BD}, whatever the injected current density or stress temperature. (ii) Skipping the RTA step in the test capacitors fabrication process induces a shift in flat-band voltage of over 1 V towards more positive voltages and a strong reduction in oxide lifetime as presented by CCS-TDDB measurements and Q_{BD} analysis. This could be partially attributed to degradation of an incomplete dopant activation in the polycrystalline silicon gate but needs further investigating due to its importance for MOS-transistor processing. No impact was observed on the D_{it}. The origin of the lower TZDB yield when skipping the RTA step or the lower extrinsic failure rate on SmartSiC™ Q_{BD} at RT are not identified and could be process related.

Acknowledgments

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