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Fabrication of the Planar SiC Gate-all-Around JFET with Channel Dose Modulation

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Abstract. Currently, silicon carbide (SiC) is widely recognized as a wide bandgap semiconductor, with expanding applications in harsh environments, such as high temperature and radiation exposure. In this study, we fabricated a planar structure 4H-SiC gate-all-around junction field-effect transistor (JFET), wherein the channel region is formed through ion implantation at varying doses. We successfully produced both normally-on and normally-off JFETs. Moreover, we constructed a JFET common source amplifier. The amplifiers achieved a maximum gain of -226.7 (47.1 dB) at a supply voltage of $V_{DD} = 30$ V.

Introduction

At present, siliocon carbide (SiC) is known as a leading wide bandgap semiconductor material because of its high tolerance to harsh environments, such as high temperature and radiation [1]. Realizing SiC integrated circuits (ICs), such as operational amplifiers, will enable devices based on SiC ICs to operate in harsh environments. Currently, four types of SiC transistors are mainly studied: bipolar junction transistors (BJTs), junction field-effect transistors (JFETs), metal-oxide-semiconductor field-effect transistors (MOSFETs), and metal-semiconductor field-effect transistors (MESFETs) [2–10]. The advantage of SiC JFETs is that they have no gate oxide layer. It has been reported that gate oxide layers can be easily degraded by radiation [11]; therefore, SiC JFETs are preferable to SiC MOSFETs in radiation environments. Meanwhile, SiC MESFETs have an inadequate interface contact between the N-channel and P-type buried back gate layer, which causes backgating [10]. For these reasons, SiC JFETs are likely the prime choice for SiC ICs operating in harsh environments. Recently, not only n-type but also p-type SiC JFETs have been demonstrated [12].

Increasing channel density is beneficial for enhancing device performance [13]. However, it raises the pinch-off voltage, leading to higher power consumption in ICs due to the need for elevated supply voltages. Therefore, to fabricate the gate region, double-gate and gate-all-around (GAA) structures are preferable to single-gate structures because a lower pinch-off voltage is suitable for the same channel density. Recently, we developed a SiC JFET featuring a GAA design, which theoretically optimizes transconductance [14]. In the design, fabricating the p+ bottom layer required extremely high-energy ion implantation, such as 3 MeV, and oblique ion implantation after gate trench etching, making unconventional processes significantly challenging.

To overcome these challenges, we propose and evaluate the characteristics of a 4H-SiC JFET with a new planar GAA structure. In this design, the gate region is fabricated by ion implantation at varying doses without the need for such high-energy implantation. In addition, two types of JFETs, normally- on and normally-off JFETs, can be customized by varying the dose amount. Further, we

constructed a common-source amplifier as a simple electronic circuit using the JFETs and assessed the maximum voltage gain.

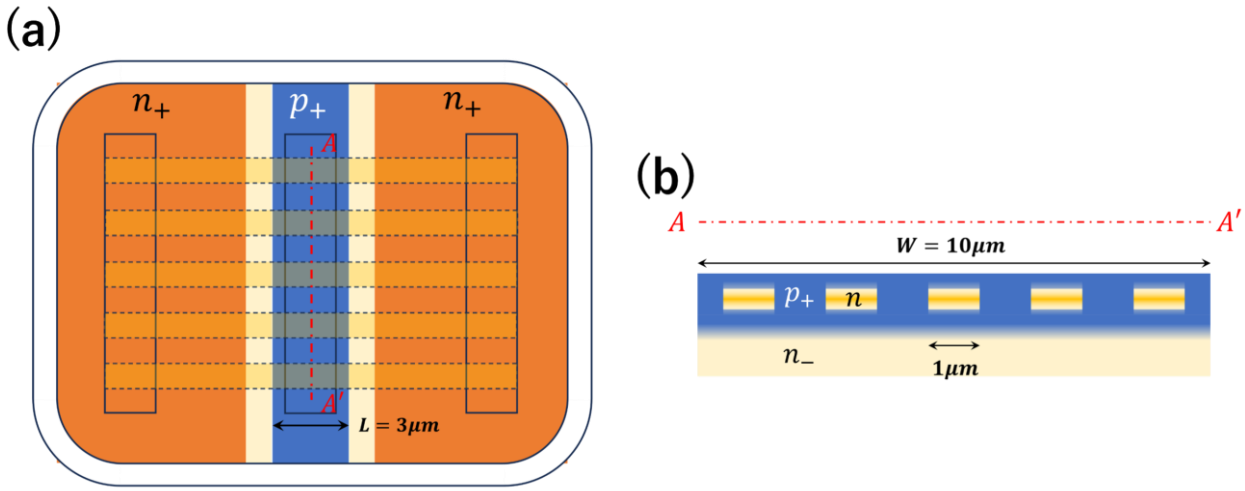

Fig. 1. (a) Top and (b) cross-sectional schematics of the planar n-type SiC GAA JFET. Five n-type channel stripes (orange) are embedded beneath the n_+ source/drain (dark orange) and p_+ gate top (blue) regions in the n_- epitaxial layer (light yellow). The p_+ gate length and width are L = 3 and W = 10μm, respectively. The device is isolated by trenches around it.

Device Fabrication

Fig.1(a) and (b) show the top and cross-sectional schematics of the proposed JFET, respectively. Five n-type channel stripes are embedded beneath the n_+ source/drain and p_+ gate top regions in the n_- epitaxial layer. The n-type channels (width: 1μm) are separated by the p_+ gate side region (1μm). The p_+ gate length and width are L=3 and W=10μm, respectively. The margin between the p_+ gate and n_+ source/drain regions is 1μm, and the width of the contact holes is 2μm. The device is isolated by trenches (width: 0.8μm, depth: 1.87μm) around it.

First, the p_+ gate bottom region is firstly formed by Al-ion implantation into the entire n_- epitaxial layer (3×10^{16}cm^{-3}, 5μm) grown on a n_{++} 4H-SiC wafer. The n-type channels, n_+ source/drain, p_+ gate side, p_+ gate top regions are then formed. We use six channel doses (0.8, 1.0, 1.2, 1.4, 1.6, and 1.8×10^{13} cm^{-2}) to control the gate threshold voltage. When the channel dose is 1.8×10^{13} cm^{-2}, the target channel density is approximately 10^{18} cm^{-3}.

After device isolation by SiC trench etching, we performed activation annealing (1650℃, 10min.). Ni contact metal is deposited on both sides of the wafer and sintered at 500. The device fabrication is completed by attaching a 1.6μm thick Al electrode on the surface side while the back side is covered with Ti, Ni, and Au layers.

IV-Characteristics of JFET

We fabricated two types of JFETs: normally-on and normally-off JFETs, by varying the channel dose amount. These are fabricated on two wafers, named 10SY and 11SY. For 10SY, three channel doses 0.8×10^{14} cm^{-2}, 1.0×10^{14} cm^{-2}, and 1.2×10^{14} cm^{-2}, were selected to achieve normally-off operation; meanwhile, for 11SY, 1.4×10^{14} cm^{-2}, 1.6×10^{14} cm^{-2}, and 1.8×10^{14} cm^{-2} were chosen to achieve normally-on operation. The device characteristics were measured with Semiconductor Parameter Analyzer Agilent 4156C. Fig. 2 shows an optical microscope image of an actual GAA JFET being measured using a manual prober. The substrate is connected to GND. The transfer and output characteristics were measured for the six doses. For the transfer characteristics, V_{DS} was set to 10 V and V_{GS} was swept from −7.5 to 2.5 while measuring I_D. For the output characteristics, for each dose, V_{GS} was varied from 0 to 2 V for normally-off and from −3 to 2 V for normally-on in steps of 1 V while V_{DS} was swept from 0 to 20 to measure I_D.

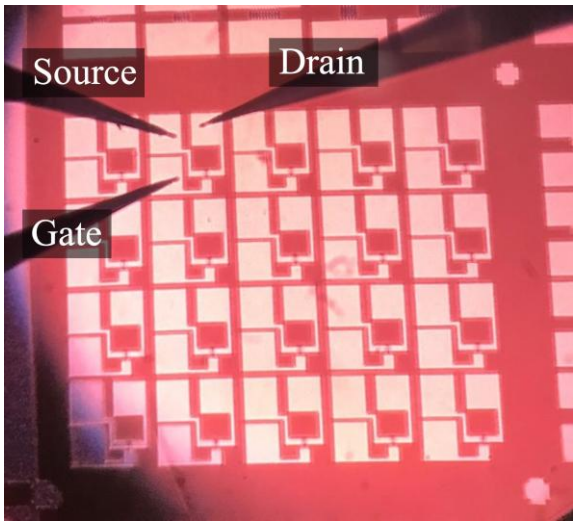

Fig. 2. Optical microscope of actual SiC GAA JFETs.

Fig. 3 illustrates the characteristics of JFETs. Fig. 3 (a) shows the transfer characteristics of JFETs with different channel doses, indicating a shift in the gate-threshold voltage V_T from 2.11 to - 3.76 V as the channel dose increases from 8.0×10^{12} to 1.8×10^{13}cm^{-2}, and Fig. 3 (b) shows the logarithmic plot of the transfer characteristics of JFETs with different channel doses. As the channel dose amounts increases, the threshold voltage shifts toward negative values.

Figs. 3 (c) and (d) display the output characteristics of the normally-off JFET with a channel dose of 1.2×10^{13}cm^{-2} and the normally-on JFET with a channel dose of 1.8×10^{13}cm^{-2}, where the drain current I_D in the saturation region remains nearly constant across the drain-source voltage V_{DS}. The device parameters are listed in Table 1. The drain current I_D was measured for the normally-off and normally-on JFETs when $V_{GS} = 2$ V and $V_{GS} = 0$ V, respectively. r_0 and g_m are calculated when $V_{DS} = 10$ V and $V_{GS} = 0$ V

Large-Signal Behaviors of JFET Common-Source Amplifier and Source Follower

To test the fabricated JFETs, simple circuits - a common-source amplifier and a source-follower amplifier - were constructed and tested. The circuit diagrams are shown in Fig. 4 (a) and Fig. 5 (a). Fig. 4 (a) is a common-source amplifier and Fig. 5 (a) is a source-follower circuit. This measurement is also conducted using Semiconductor Parameter Analyzer Agilent 4156C. In the measurement of the common-source amplifier, V_{DD} was set to 10, 20, and 30 V with V_{in} swept from -2 to 2 V while the corresponding output was measured. Similarly, for the source-follower amplifier, V_{in} was swept from -2 V to the maximum V_{DD} under the same V_{DD} settings while the output was recorded.

Fig. 4 (b) shows the output voltage V_{OUT} of the common-source amplifier under large-signal analysis. As verified in the figure, V_{OUT} turns off when V_{IN} reaches 0 V, as expected. The maximum gain of the amplifier around $V_{IN} = 0$ V was calculated, resulting in values of -17.1 (24.6 dB), -112.6 (41.0 dB), and -226.7 (47.1 dB) for $V_{DD} = 10$, 20, and 30 V, respectively. The gain can be determined using $A_v = \frac{V_{out}}{V_{in}}$, calculated from the slope of the I/O characteristics. In Fig. 5 (b), the output voltage V_{OUT} of the source-follower amplifier is shown. The circuit's correct operation is confirmed by the manner the output rises in response to the input, effectively following it.

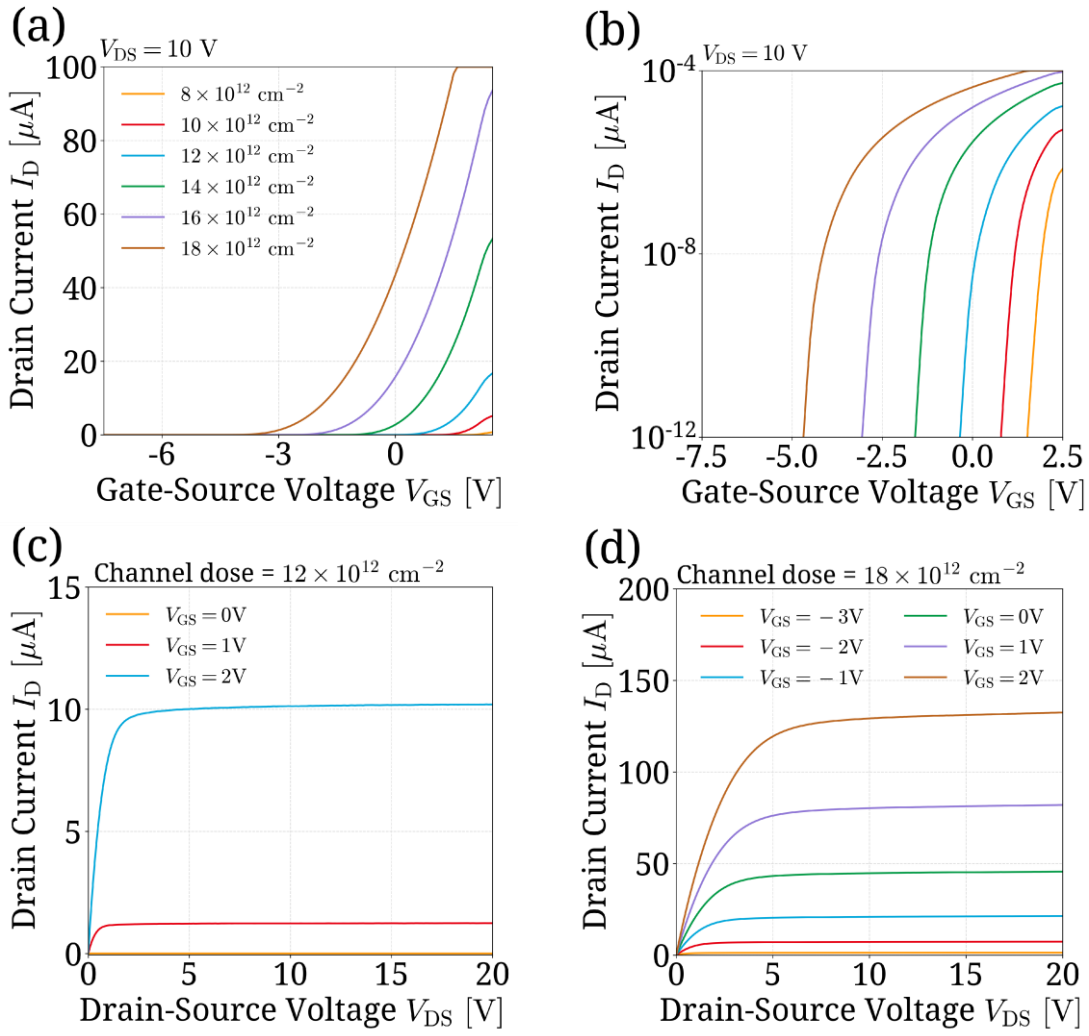

Fig. 3. (a) Transfer characteristics of normally-on and normally-off JFETs per channel dose when $V_{DS} = 10$V. (b) Logarithmic plot of transfer characteristics of normally-on and normally-off JFETs per channel dose amounts when $V_{DS} = 10$V. The color legend is the same as in (a). (c) Output characteristics of normally-off JFET for gate-source voltages (V_{GS}) of 0, 1, and 2 V. The channel dose is 1.2×10^{13} cm^{-2}. (d) Output characteristics of normally-on JFET for gate-source voltage (V_{GS}) steps from -3 V to 2 V in increments of 1 V. The channel dose is 1.8×10^{13} cm^{-2}.

Summary

In this study, normally-on and normally-off JFETs with a planar GAA structure were fabricated and demonstrated. By varying the channel dose, we successfully produced both types of JFETs. Their characteristics were measured using the Semiconductor Parameter Analyzer Agilent 4156C. In addition, simple electronic circuits, including a common-source amplifier and a source-follower amplifier, were constructed and tested using the JFETs. The maximum gains of the amplifiers near $V_{IN} = 0$ V was found to be -17.1 (24.6 dB), -112.6 (41.0 dB), and -226.7 (47.1 dB) for $V_{DD} = 10$ V, 20 V, and 30 V, respectively.

Table 1. Device parameters per varied dose.

Dose [cm^{-2}]	I_D [μA]	r_0 [MΩ]	g_m [μS]	$A_v = r_0 g_m$
1.0×10^{13}	1.98	110	6.10	671
1.2×10^{13}	10.0	23.8	14.8	352
1.4×10^{13}	2.78	192	6.06	1164
1.6×10^{13}	16.1	22.5	17.1	385
1.8×10^{13}	45.0	6.79	29.6	201

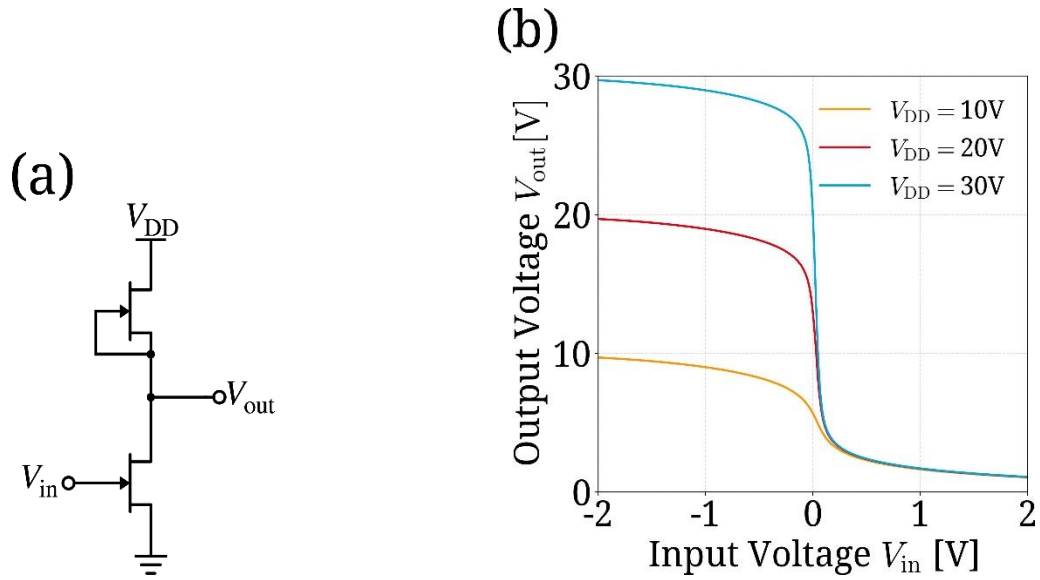

Fig. 4. (a) Common-source amplifier circuit diagram and (b) transfer characteristics of the common source amplifier. In the circuits, normally-on JFET devices are used, where the typical resistor is replaced by shorting the JFET's source and gate. The maximum gain around $V_{IN} = 0$ V was observed at V_{DD} = 10, 20, and 30 V.

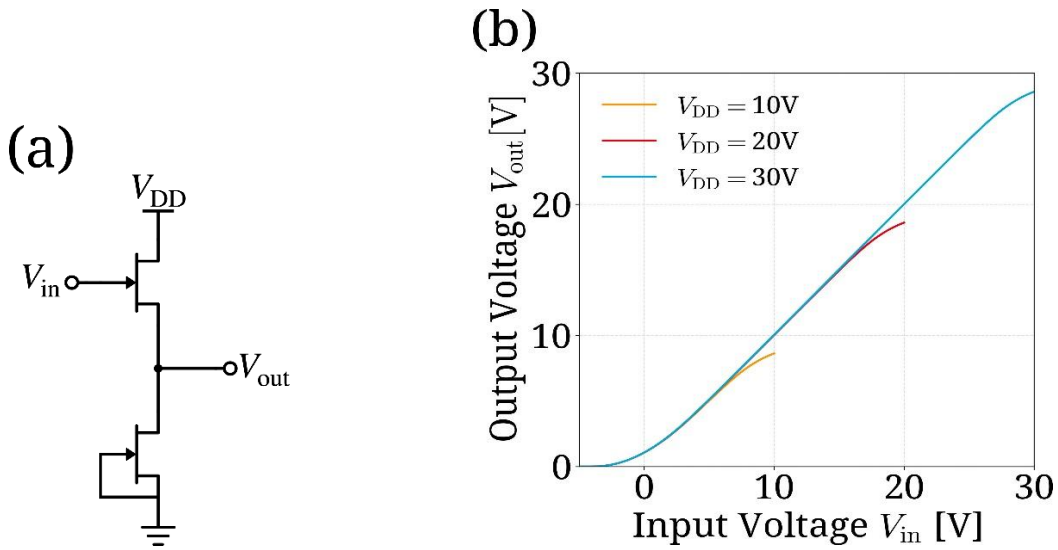

Fig. 5. (a) Source-follower amplifier diagram and (b) transfer charactristics of the source-follower amplifier circuit.

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