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Investigation of Poly-Si Gated, Al_2O_3-Based High-*k* Dielectrics on 4H-SiC

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Abstract. In this paper, we investigate the electrical and structural characteristics of Al_2O_3-based high-*k* gate dielectrics, which were integrated into a gate-first, high-temperature manufacturing process having comparable thermal budget as needed in 4H-SiC metal-oxide-semiconductor field-effect transistor (MOSFET) production. MOS capacitors were chosen as test devices to examine the electrical performance in terms of current-voltage (*I*-*V*) and capacitance-voltage (*C*-*V*) behavior. Remarkably, even after processing temperatures of up to 1,000 °C for ohmic contact formation, the Al_2O_3 layers revealed highly uniform breakdown characteristics, low *C*-*V* hysteresis and a flat-band voltage (V_{FB}) that closely aligns with the theoretical value. Time-dependent dielectric breakdown (TDDB) measurements of the Al_2O_3 MOS capacitors, however, showed a clear reliability disadvantage concerning the intrinsic dielectric lifetime when comparing with the SiO_2 counterpart from commercial SiC production. Finally, to better understand the electrical behavior, transmission electron microscopy (TEM) analysis was conducted, pointing out that high-temperature processing causes the Al_2O_3 films to transition from an amorphous state to an ordered, polycrystalline structure.

Introduction

Even though the SiC power MOSFET is an established product by now, there is still plenty of room for improving the transistor's performance. To exploit the full potential of the superior material properties of SiC, namely the low drift zone resistance due to the high breakdown field strength, other series resistance contributions, such as the channel resistance, must be kept as small as possible. Despite the continuous progress in improving the SiO_2/4H-SiC interface and therefore the channel mobility, the channel contribution to the overall on-state resistance ($R_{DS,on}$) remains considerable for most of the SiC power MOSFET products [1].

An innovative approach to minimize the channel contribution is to utilize high-*k* insulators as gate dielectric material. Due to their higher dielectric constant, the induced inversion charge is increased for the same applied voltage, leading to a reduced channel resistance. Furthermore, most of the high-*k* dielectrics are deposited by using an atomic layer deposition (ALD) process, which is known for precise thickness control, high uniformity, conformality and reproducibility and offers unique possibilities for in-situ interfacial engineering.

However, there are still major challenges, which complicate the integration of these dielectrics into commercially available SiC power MOSFETs. One of them is the relatively low thermal stability of the commonly used high-*k* materials. During typical SiC power MOSFET production, temperatures up to 1,000 °C are needed for ohmic contact formation. Moreover, compatibility with poly-Si gate electrode formation must be ensured. According to literature, these processes often lead

to crystallization of the high-*k* layers, hampering their usage as gate dielectric due to inacceptable leakage currents and reliability issues [2].

In this work, we study the influence of the typical high-temperature processes on the electrical characteristics of poly-Si gated, Al_2O_3-based MOS capacitors. We have chosen Al_2O_3 as the main gate dielectric material due to the relatively high thermal stability as well as the large conduction and valence band-offsets to 4H-SiC. We modified the interfacial properties by using gate dielectric stacks, consisting of thin interfacial layers (SiO_2 and AlN), followed by subsequent Al_2O_3 deposition.

Experimental Details

Device Fabrication. The MOS capacitors characterized in this work were fabricated on epitaxial n-type layers, grown on conventional 4°-off axis (0001) 4H-SiC 6" substrates. The fabrication, except the gate dielectric depositions, took place in the corporate research cleanroom of the Robert Bosch GmbH. A schematic cross-section of the devices as well as the processing sequence including the applied thermal budget is shown in Fig. 1.

Prior to the gate dielectric deposition, the SiC wafers were cleaned and subsequently etched in a diluted HF acid solution to remove any oxidized surface species. Right after, the Al_2O_3-based gate dielectric layers and stacks were deposited according to the wafer overview in Fig. 1 using ALD technology from Beneq TFS 200 R&D. For selected wafers, the interfacial properties were modified by depositing a 5 nm layer of either plasma-enhanced ALD (PEALD) SiO_2 or PEALD AlN prior to the Al_2O_3 deposition. The Al_2O_3 films of all samples were grown by means of thermal ALD using trimethylaluminium (TMA) and H_2O as precursors. For PEALD AlN, TMA and a plasma mixture of NH_3 and N_2 was utilized. In the case of SiO_2 growth, Bis(diethylamino)silane and O_2 plasma were employed as precursors. The process temperature for all depositions was maintained at 300 °C to ensure the production of high-purity films.

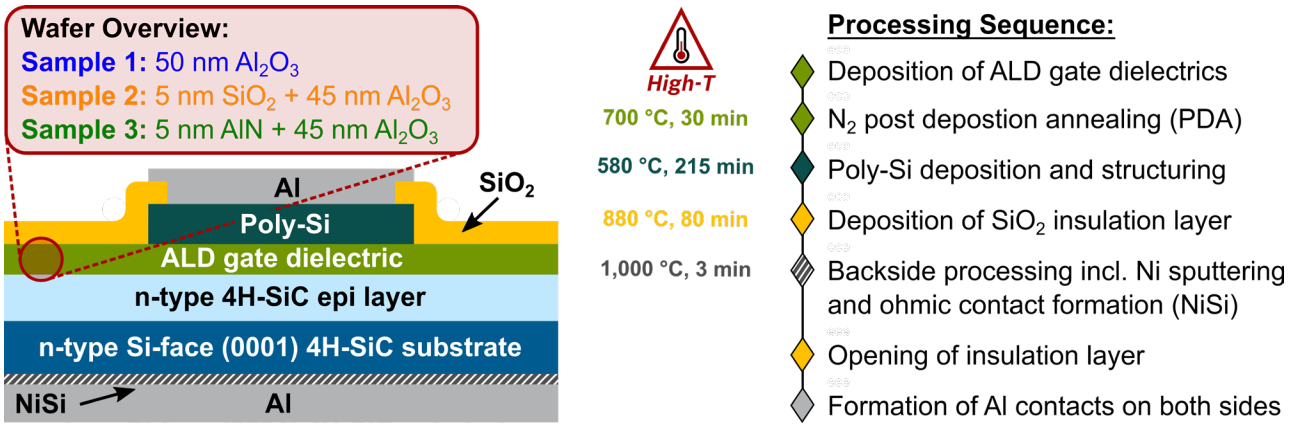

Fig. 1. Process flow including the corresponding thermal budget, cross-section and wafer overview of the fabricated Al_2O_3-based MOS capacitors.

Except for the ALD process, all three wafers underwent exactly the same fabrication process. After post deposition annealing (PDA) in N_2 ambient at 700 °C for 30 min, in-situ P-doped poly-Si was deposited by means of low-pressure chemical vapor deposition (LPCVD) to form the gate electrode layer. Subsequently, a reactive ion etching (RIE) process was used to structure the poly-Si layer, followed by encapsulating the MOS stack in a high-temperature oxide (HTO), deposited via LPCVD at elevated temperature to enhance the deposition rate. This additional SiO_2 layer was primarily applied to attenuate the electric field strength at the edges of the poly-Si pads to make the MOS capacitor devices suitable for reliable TDDB measurements.

Forming the backside ohmic contact consists of sputter deposition of a thin Ni layer, combined with a rapid thermal annealing (RTA) process at 1,000 °C for 3 min afterwards. Finally, the Al pads were formed on the frontside and backside to contact the MOS capacitor devices during electrical characterization. As the overall applied thermal budget is comparable to SiC MOSFET fabrication, the obtained electrical results are expected to be transferable to transistor devices.

Electrical Characterization. The fabricated MOS capacitor devices were electrically characterized in a Cascade Microtech probe station equipped with different measurement instruments. For *I-V* breakdown characteristics as well as constant voltage TDDB measurements, a Keithley 2636 sourcemeter was connected to the MOS devices. Quasi-static *C-V* measurements were conducted by using a measurement setup consisting of a Keithley 6517 electrometer and a Keithley 2010 multimeter. In this configuration, the electrometer was used to measure the charge on the gate electrode while the applied, stairs-like voltage profile was traced with the additional multimeter.

Structural Characterization. To investigate the atomic structure of the gate dielectrics after high-temperature processing, TEM analysis was carried out in a Thermo Fisher Scientific Talos F200X equipment. All inspections were performed using an acceleration voltage of 200 kV. Electron diffraction patterns of the SiC crystal were taken to align the samples accordingly.

Results and Discussion

For precise evaluation of the device parameters, the final thickness of the gate dielectric layer after the fabrication process is needed. Therefore, we made TEM images of the samples, as shown in Fig. 2 a)-c). For all three samples, the ALD gate dielectrics got densified during MOS capacitor device fabrication, leading to an overall thickness decrease of approximately 10 %. Similar behavior was already observed previously when annealing Al_2O_3 layers under high temperatures [3].

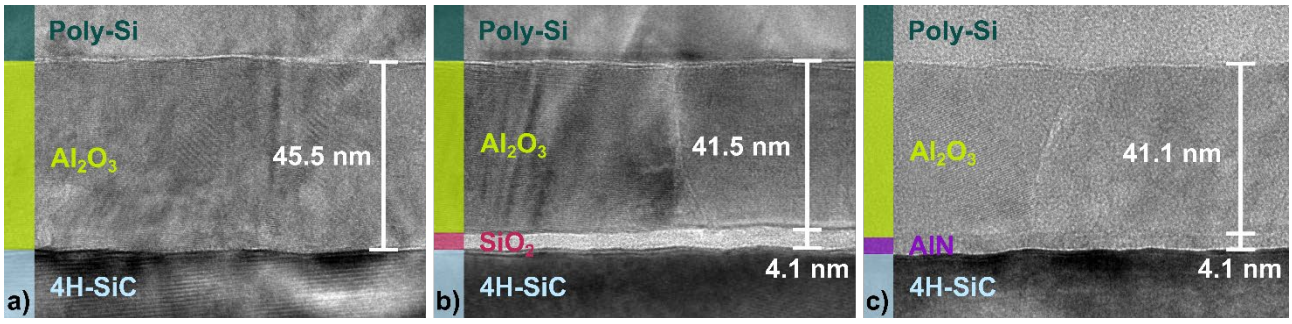

Fig. 2. TEM overview images of a) sample 1 (Al_2O_3/4H-SiC), b) sample 2 (Al_2O_3/SiO_2/4H-SiC) and c) sample 3 (Al_2O_3/AlN/4H-SiC). The shown thickness values are averaged by using several measurements at different positions of one MOS capacitor from the middle of each wafer.

Electrical Results. Fig. 3 a) shows the *I-V* breakdown measurements, which were conducted for numerous MOS capacitor devices per sample in a cross-shape over the whole wafer. Interestingly, samples 1 and 3 show a high uniformity and a Fowler-Nordheim-shaped current increase with an average breakdown field strength E_{BD} of around 7 MV/cm, whereas sample 2 depicts a much higher spread including premature breakdowns. Comparing all three samples, the only notable difference is the interfacial material in direct contact to the underlying SiC. Accordingly, the results indicate that this interfacial layer is crucial, impacting not only the interface trap density, but also the current blocking capability of the Al_2O_3 layer.

Besides the *I-V* analysis, quasi-static *C-V* measurements were performed. The corresponding results are shown in Fig. 3 b) for five different devices per wafer. The gate voltage was swept between +7 V and -7 V to stay below the dielectric breakdown of sample 2. Especially in terms of accumulation capacitance, flat-band voltage V_{FB} and hysteresis ΔV_{FB}, a clear difference between the samples is observed. Sample 1 exhibits the highest accumulation capacitance, whereas the value gradually decreases from sample 3 to sample 2 owing to the lower dielectric constant ε_r of the interfacial AlN and SiO_2 layer with respect to the Al_2O_3. Together with the thickness data of Fig. 2 a), measuring the accumulation capacitance of sample 1 allows the ε_r extraction of the Al_2O_3 layer. The resulting value of $\varepsilon_r = 10.2$ is comparably high and may be attributed to a crystallization of the Al_2O_3 layer during the high-temperature processes of the fabrication sequence [4].

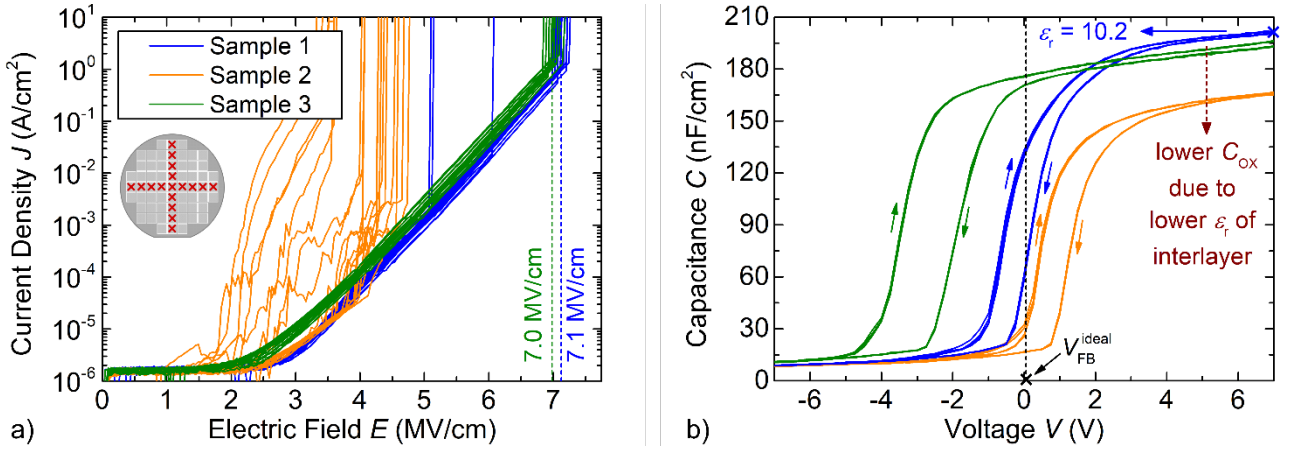

Fig. 3. a) *I-V* breakdown measurements for MOS capacitors distributed in a cross-shape over the whole wafer, b) quasi-static *C-V* measurements for five devices per wafer in up- and down-sweep direction.

Nevertheless, especially sample 1 without an intentionally modified interface reveals promising *C-V* characteristics with low hysteresis and a V_{FB} value that closely approximates the theoretical value of a poly-Si gated dielectric on SiC. All extracted parameters from Fig. 3 a) and b) are summarized in Table 1. Compared to published analysis on Al_2O_3 gate dielectrics on SiC [5], the results are notably promising, especially when taking the high thermal load into account, which the devices experienced during the fabrication process. Processing at such high thermal budgets typically leads to crystallization of the Al_2O_3 layers, accompanied by deteriorated electrical characteristics, such as high leakage currents [6] and/or a large shift in V_{FB} [7].

Table 1. Summary of the sample parameters breakdown field strength E_{BD}, flat-band voltage in both sweep directions $V_{FB,low}$ and $V_{FB,high}$ and hysteresis ΔV_{FB} at the flat-band capacitance. Values are averaged and given with the respective standard deviation. E_{BD} for sample 2 is not listed due to the high spread of values across the wafer.

	Sample 1	**Sample 2**	**Sample 3**
E_{BD} (MV/cm)	7.13 ± 0.08	-	6.97 ± 0.08
$V_{FB,low}$ (V)	-0.36 ± 0.03	0.64 ± 0.02	-3.32 ± 0.01
$V_{FB,high}$ (V)	0.34 ± 0.01	1.46 ± 0.01	-1.72 ± 0.01
$\Delta V_{FB} = V_{FB,high} - V_{FB,low}$ (V)	0.71 ± 0.03	0.82 ± 0.02	1.60 ± 0.01

Due to the excellent uniformity of the *I-V* results, constant voltage TDDB measurements at three different temperatures were carried out for MOS capacitors of sample 1. The corresponding results are shown in Fig. 4. In Fig. 4 a), measurements of different devices at stress voltages between 12 V and 17 V and a temperature of 175 °C are plotted in a double-logarithmic Weibull plot. As the time to dielectric breakdown t_{BD} increases exponentially with lowering the applied gate voltage, we showed only for one voltage (13 V), that stressing of 62 instead of nine devices ends up in the same Weibull slope of the intrinsic failure branch. Therefore, we conclude that a lower statistic is sufficient to obtain a reliable lifetime estimation.

To get a prognosis of the intrinsic Al_2O_3 lifetime at typical operation conditions, the t_{BD} values, at which 63 % of the devices broke ($t_{63\%}$ lifetime), were extracted out of Fig. 4 a) and used for the lifetime extrapolation shown in Fig. 4 b). When comparing the lifetime of different gate dielectrics, it is mandatory to consider variations in the oxide thickness d_{ox} as well as the ε_r value. Therefore, the $t_{63\%}$ lifetime is plotted over the electric displacement field strength D, which can be calculated by using the following expression.

$$D = \varepsilon_0 \varepsilon_r E = \varepsilon_0 \varepsilon_r \frac{V}{d_{ox}}. \quad (1)$$

The *D*-field value thereby describes the charge carrier density at the oxide semiconductor interface and allows for a fair comparison between the Al_2O_3 gate dielectric of sample 1 and the SiO_2 counterpart, used in commercial SiC production. The extracted $t_{63\%}$ values at different stress voltages and temperatures are extrapolated to a *D*-field of 1 µC/cm^2, which represents a typical on-state condition when assuming a SiO_2 gate dielectric in SiC MOSFET technology. The estimated intrinsic Al_2O_3 lifetime at 1 µC/cm^2 and a stressing temperature of 140 °C yields values in the range of 10-100 years, which is orders of magnitude below the SiO_2 counterpart [8]. Nevertheless, the conducted measurements are highly consistent and scale perfectly with temperature, as shown in the inset of Fig. 4 b).

Especially due to the large number of extrinsic defects in SiC technology, the $t_{63\%}$ lifetime should lie well above the typical operation lifetime to ensure the reliability requirements for automotive applications [8]. The typical operation lifetime in on-state is represented by the red star in Fig. 4 b). The comparably lower projected lifetime of the Al_2O_3, therefore, leads to a reduced "safety margin" with respect to a typical operation lifetime of a SiC MOSFET.

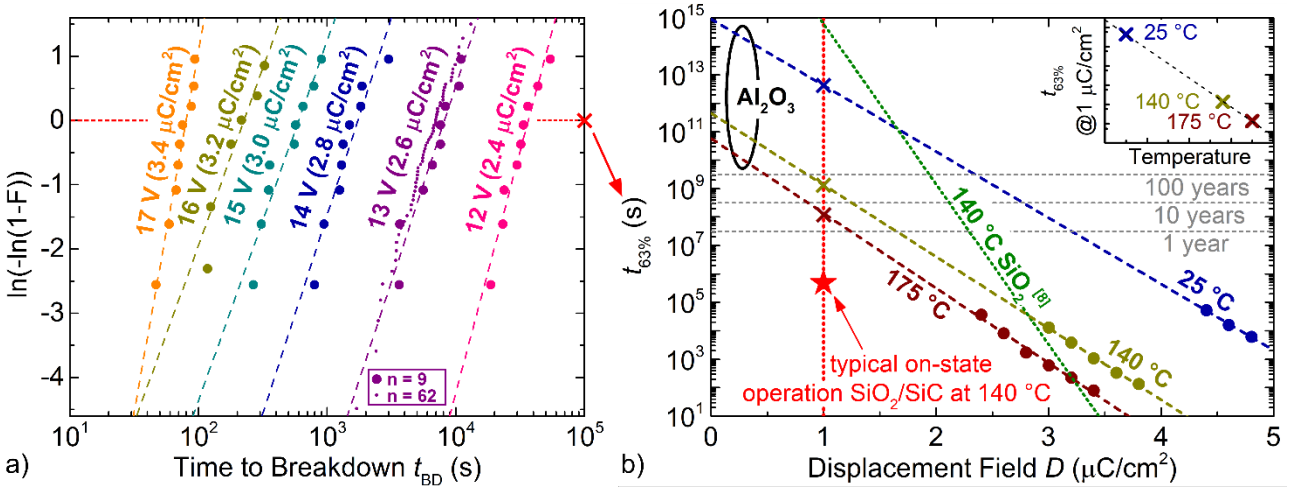

Fig. 4. a) Weibull plot for constant voltage TDDB measurements of sample 1 at 175 °C, b) extracted and extrapolated $t_{63\%}$ lifetime over *D*-field strength for sample 1 as well as a comparison with the published values of a SiO_2 gate oxide on planar 4H-SiC [8].

The integration of Al_2O_3-based high-*k* dielectrics into SiC MOSFETs, used for automotive application, would require additional effort to improve the TDDB behavior of these layers. Therefore, it is crucial to understand the reason behind the above-mentioned lifetime issue. Previously, the effect of the PDA temperature on the reliability of Al_2O_3 dielectrics on GaN was investigated [9]. The published results show that the transition from an amorphous to a crystalline structure by high-temperature annealing comes along with a decrease in reliability. To check whether a similar phenomenon could explain our results, we performed TEM analysis for all three samples.

Structural Results. Exemplary high-resolution TEM images of sample 1 with different magnification are shown in Fig. 5. The atomic arrangement within the Al_2O_3 layer clearly points out that crystallization happened during the MOS capacitor fabrication process. The fast Fourier transformation (FFT) pattern, represented in the inset of Fig. 5 c), supports this observation. Besides the contributions of the SiC substrate, the FFT pattern contains extra reflections, which are attributed to the crystallized Al_2O_3 film. Furthermore, polycrystalline grains and defects are visible. These non-idealities potentially promote the formation of leakage paths, that lead to a comparably low lifetime of the Al_2O_3 gate dielectrics.

As a result of the crystallization process, the atoms inside the Al_2O_3 film rearrange, causing mechanical stress on the underlying SiC substrate. The effect of the stress potentially shows up in the strain fields, which are observed in Fig. 5 a) at the Al_2O_3/SiC interface inside the semiconductor.

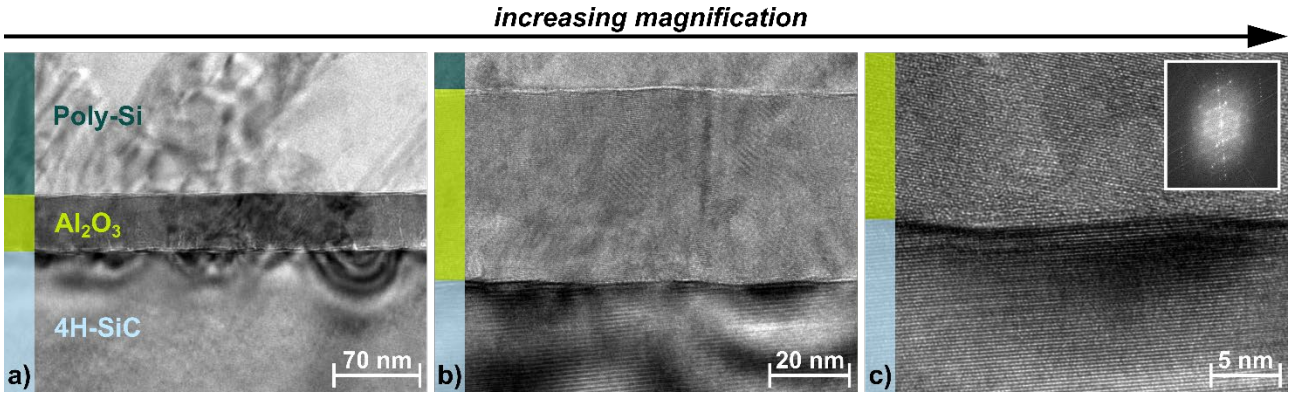

Fig. 5. High-resolution TEM images of sample 1 with increasing magnification from a) to c).

Comparing the thermal budget of the fabrication process used in this work with published results regarding the annealing of Al_2O_3 layers on SiC, it is not surprising that crystallization happened during processing. Typically, the crystallization temperature of Al_2O_3 is reported to lie around 800-900 °C [10]. Especially the ohmic contact annealing and the insulation layer deposition process clearly exceeded this temperature (comp. Fig. 1). Additionally, several studies revealed an unintentional formation of a thin SiO_2 layer at the boundary between Al_2O_3 and SiC due to an interfacial reaction during high-temperature annealing [11,12]. Such an interfacial SiO_2, however, could not be observed in our studies.

The TEM investigations of samples 2 and 3 showed similar observations in terms of crystallization and strain fields. Therefore, only TEM images at higher magnification are shown in Fig. 6. As expected, the SiO_2 interlayer of sample 2 in Fig. 6 a) is still amorphous, whereas the AlN interlayer of sample 3 in Fig. 6 b) shows areas that seem to have a crystalline atomic arrangement. Accordingly, the Al_2O_3 film is only for sample 2 in vicinity of an amorphous layer. This might possibly change the onset of the crystallization transition, leading to different grain size, more leakage paths and therefore worse breakdown results (comp. Fig. 3 a)).

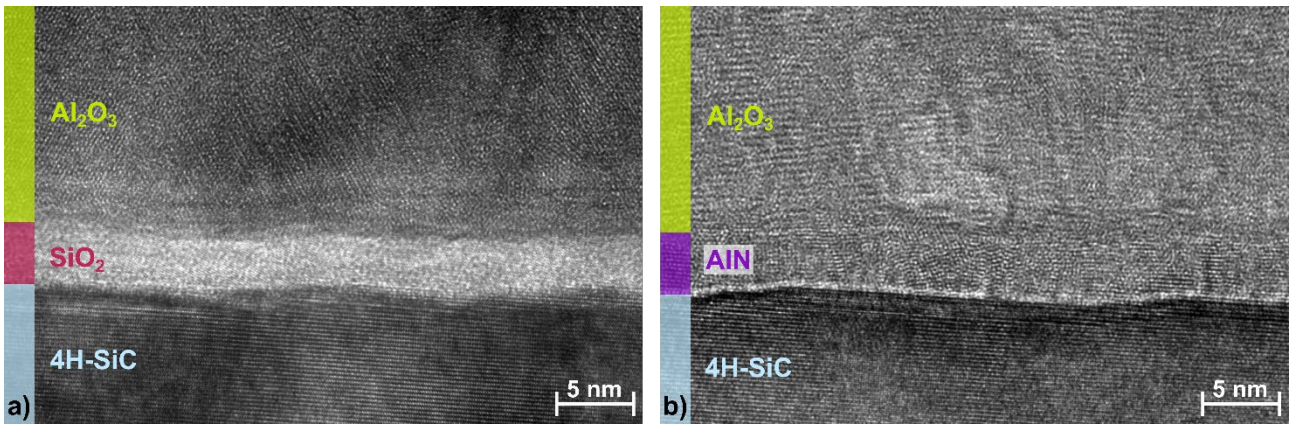

Fig. 6. High-resolution TEM images showing the interfacial arrangement of a) sample 2 (Al_2O_3/SiO_2/4H-SiC) and b) sample 3 (Al_2O_3/AlN/4H-SiC).

Summary

In this work, the influence of a typical, high-temperature SiC fabrication process on the electrical and structural properties of Al_2O_3-based high-*k* dielectrics was investigated. Gate-first MOS capacitors with poly-Si gate electrode and NiSi backside contact were chosen as test vehicles. Especially for Al_2O_3 dielectrics without an interfacial layer, we showed promising electrical results, consisting of highly uniform breakdown characteristics, high dielectric constant, low *C-V* hysteresis and a nearly ideal flat-band voltage. Nevertheless, TDDB measurements revealed a rather low intrinsic lifetime at typical operation conditions when comparing with a SiO_2 gate dielectric from commercial SiC production. A possible root cause for the comparably low lifetime was found by performing high-

resolution TEM analysis, where all Al_2O_3 layers turned out to be polycrystalline. Furthermore, our work underlined the crucial role of carefully designing the gate dielectric-semiconductor-interface, not only in terms of interface defects, but also for tailoring the crystallization behavior of high-*k* dielectrics.

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