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SiC Plasma Dicing for Future High Yield Die Singulation

B. Jones[1,a*], A. Croot[2,b], J. Mitchell[2,c], S. Kazemi[2,d], C. Bolton[2,e], H. Ashraf[2,f], M. Jennings[1,g], O. J. Guy[1,h]

[1]Swansea University, Singleton Park, SA2 8PP, Swansea, UK

[2]KLA Corporation (SPTS Division), Ringland Way, NP18 2TA, Newport, UK

[a]828129@swansea.ac.uk, [b]alex.croot@kla.com, [c]jacob.mitchell@kla.com, [d]samira.kazemi@kla.com, [e]chris.bolton@kla.com, [f]huma.ashraf@kla.com, [g]m.r.jennings@swansea.ac.uk, [h]o.j.guy@swansea.ac.uk

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Abstract. Silicon Carbide is an exceptionally hard and challenging to process semiconductor material. Effective device singulation retaining 100% die yield is hard to achieve with conventional saw dicing. Chips, microcracks and machining abrasions lead to reduced die strength and increased scrap. With rapid advancements in SiC device processing, resolving many fabrication issues, dicing yield losses are becoming an area of industrial concern. Plasma dicing has a proven track record in silicon and presents a potential solution to low yields during SiC dicing. Smooth vertical sidewalls with no machining damage, with etch rates approaching 5 μm/min, position SiC plasma dicing as a viable alternative ready for industrial uptake. Plasma etch processes development using Ni and Cu etch masks, with full singulation have been demonstrated, resulting in improved die strength compared to saw diced samples.

Introduction

Silicon carbide power MOSFETs with blocking voltage ratings between 650 V and 1200 V are increasingly being used for applications in electric vehicles, while SiC is also utilized as a substrate for high frequency GaN RF devices. Effective singulation of SiC die, with reduced dicing lane widths and subsequent increase in die per wafer is an important technological development for device production. Conventional saw dicing is known to introduce chips and abrasions which serve as sites for crack propagation, significantly weakening the individual SiC die with a detrimental impact on yield by 9% on average across the industry [1]. Given the rapid advancements in SiC device processing and a focus on reducing defects for automotive applications [2], SiC die singulation yield losses stand to become a focal area of improvement in the future.

Laser-based die singulation technologies such as stealth dicing show promise but can introduce localized heating and stress to the wafer in the form of increased dislocation density around the diced region [3]. Plasma dicing of SiC offers an alternative avoiding edge chipping, surface particle damage, tooling losses related to saw dicing [4] and thermal stresses and particulates associated with laser dicing. Assuming a dicing lane width reduction to 30 μm from 100 μm (saw dicing), and a die size of 5 × 5 mm translates to a 5% yield increase across a 150 mm wafer. This predicted yield improvement is compounded by the established 9% yield loss typical of saw dicing, suggesting an overall yield improvement of up to 14% if plasma dicing was utilized over saw dicing. This is depicted graphically in **Fig. 1.** Additionally, the projected plasma dicing yield improvements willenefit from economies of scale when industry adopts larger wafer sizes and reduced wafer thickness, while the throughput will also increase compared to saw dicing as lanes will not need to be diced individually. The ability to singulate SiC die with maximised die yield, minimal defects and at a cost-effective throughput is an industry priority.

This work presents SiC dicing etch optimisation building on previously reported results [5] while demonstrating use of Cu etch masking and providing insight into on-wafer processing temperatures. The capabilities of plasma dicing technology are outlined with a goal of providing an industry-ready solution to the issues associated with current wafer dicing processes.

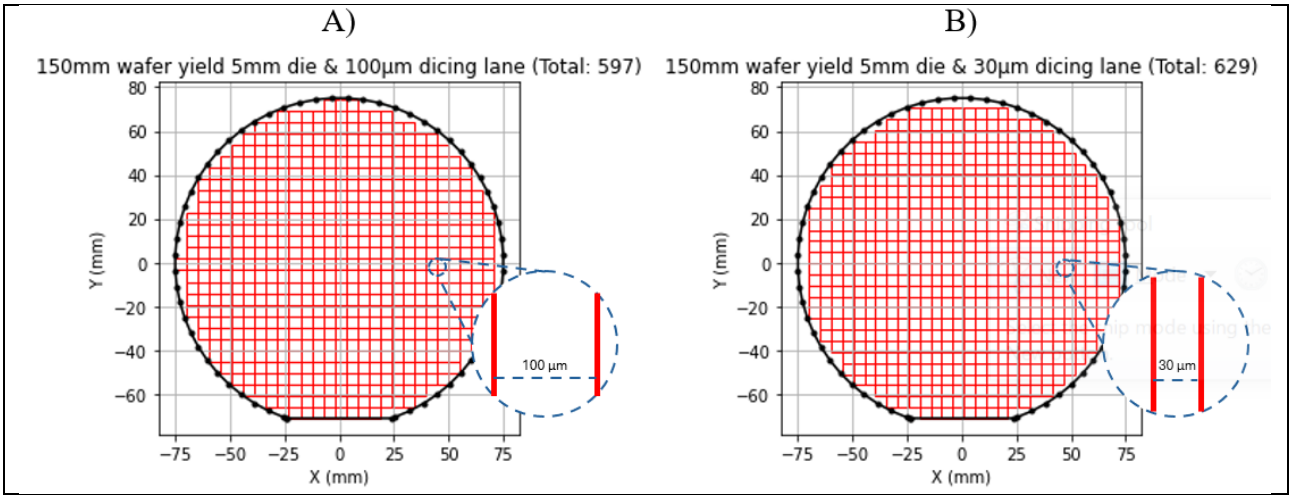

Fig. 1. Plotted 150mm die yield comparison between A) saw dicing and B) plasma dicing, if die size is 5 × 5 mm and lane width for saw dicing is 100 µm, while plasma dicing lanes are 30 µm wide. This results in a theoretical 5% yield increase for the plasma diced wafer.

Methods

For this study 350 µm bulk and 100 µm thinned 150 mm SiC wafers with Cu etch masks were used, with examples of Ni etch masks also used for comparison. A dicing lane width of 30 µm was used to singulate 5 × 10 mm die, and to perform etch process trend development work on 10 ×10 mm die. All development work was performed using bulk SiC pieces on Cu-coated Si carrier wafers, bonded with an adhesive stable up to 300°C. An SPTS SynapsEtch™ module was used for the RIE processing, capable of maximum 2.5 kW source and 1.5 kW bias powers. This process module facilitates a high-density plasma, with a readily changeable wafer-source distance to maximise high energy ions interacting with the wafer. SF_6 and O_2 etch chemistry was used for this backside etch. SEM imaging was used to obtain etch rate, profile angle and etch rate uniformity data while bias power, SF_6 flow and process pressure were varied over the course of this study.

On-wafer process temperature data was acquired using an FLIR T530 thermal camera with temperature range set to 0 – 650 °C. The process module top view port was fitted with a ZnSe window to allow emission of infrared spectra. The Cu coated SiC pieces used for the temperature study were mounted alongside an IR emissive material (Cu has an IR emissivity of ~ 0.05) to obtain accurate temperature readings.

For the die strength testing a Mecmesin MultiTest-dV 2.5 force tester fitted with an AFG gauge was used. The strength test criteria was a 3 point break test, performed flat, lengthways on the 5 × 10 mm singulated SiC die.

Results and Discussion

SiC dicing etch process tests were performed to optimise etch rate and examine profile angle and etch uniformity. Etch process trends shown in **Fig. 2. A)** show the SiC etch characteristics of Cu and Ni masks with respect to varied bias power, with maximum source power. The etch rate for the Cu-masked samples is almost double that of the Ni-masked samples, while the profile angle and uniformity are also improved on average. For efficient whole wafer singulation, low percentage etch rate uniformity is highly desirable, as the processing time will be limited to the slowest etch rate (typically at the wafer edges).

The improved etch rate and profile angle of the Cu-masked samples could be explained by the difference in metal sputtering and re-deposition behaviour during processing – effectively reducing masking by re-deposited metal. From previous work [5] it is understood that the Cu redeposition is less than that of the Ni. The reduction in sidewall redeposition results in an etch profile angle closer to 90°. Cu sputter yield is typically higher than that of Ni, so the reduced Cu redeposition could be

caused by the fact it is more easily removed by the ongoing etch [6]. This could also explain the increased etch rate of the Cu masked sample – sputtered Cu at the base of the trench being more easily removed by the ongoing etch, compared to the Ni counterpart.

Given the improvements offered by the Cu mask, all subsequent process development was performed on Cu-masked SiC. **Fig. 2. B)** shows the effects of altering SF_6 flow. The depicted trend presents an etch rate plateau at 84% of total applied SF_6 flow, while the uniformity continues to improve at maximum applied SF_6 flow. Increased SF_6 flow improving the etch uniformity is likely due to an increase in fluorine ions available to interact with the SiC. The influence of process pressure on etch outputs is shown in **Fig. 2. C)**. A marked improvement in etch rate at higher process pressures is seen, likely owing to increased etchant density at the trench base. However, etch uniformity suffers with increasing process pressure.

Based on the results in **Fig. 2.** it was presumed that a cumulative benefit could be attained by combining increased SF_6 flow and raising process pressure. **Fig. 3. A)** shows the etch trends when high process pressure is maintained and SF_6 flow is varied, while **Fig. 3. B)** shows changing process pressure with maintained high SF_6 flow. Contrary to the assumption that combined increases in process pressure and SF_6 flow should improve the etch rate, **Fig. 3.** shows that the etch rate and uniformity decrease at this process regime.

Table 1 summarises a proposed hypothetical etch mechanism for the differences in results found at the range of applied process conditions. At high SF_6 flow the Cu mask undergoes more aggressive chemical etching which promotes increased Cu sputtering and redeposition in the trench, as the byproduct is not significantly volatile. At lower process pressures we propose that the removal rate of redeposited material increases, owing to the greater ability of ions to reach the base of the trench. When both SF_6 flow and process pressure are high, Cu sputtering into the trench is high but its removal is hindered by the high process pressure (short mean free path for ions), perhaps explaining the reduced etch rates seen in **Fig. 3.** Requiring validation by further tests, this explanation suggests that the etch mechanism of the Cu mask in fluorine is predominantly chemical, which is plausible as Cu readily forms bonds with fluorine in solution.

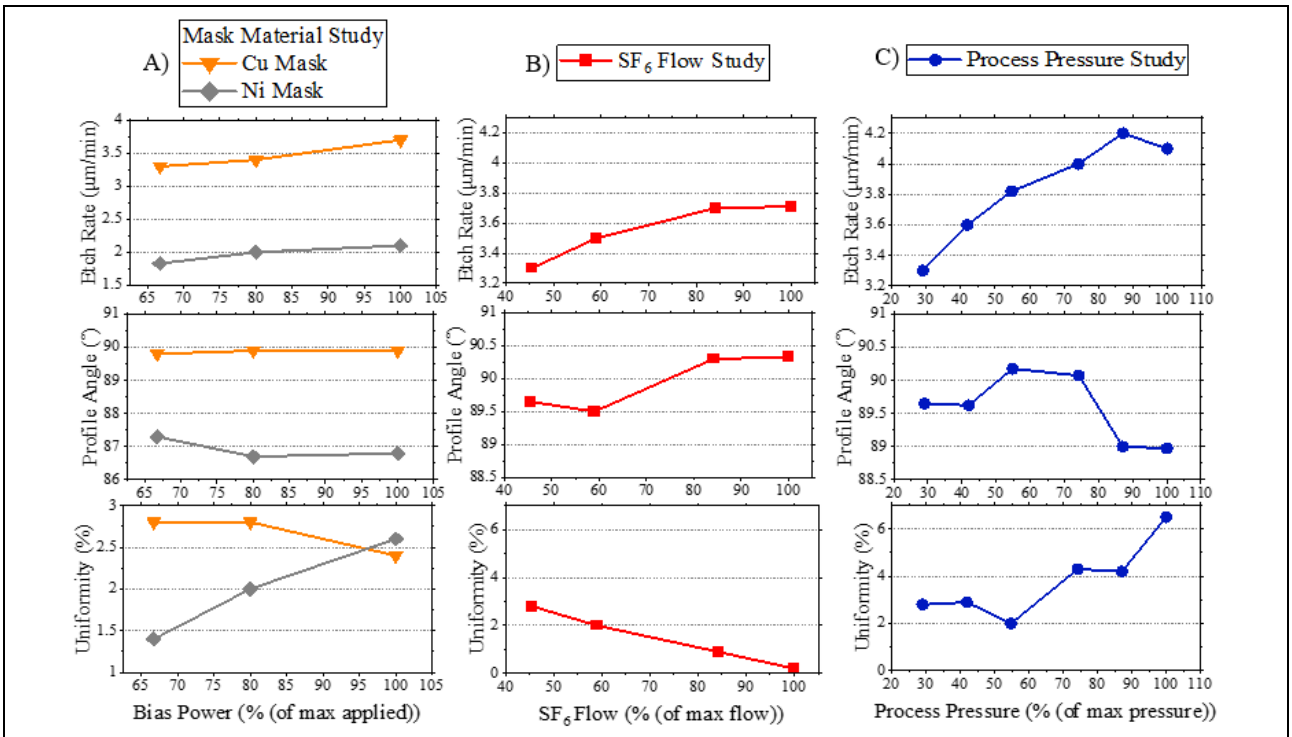

Fig. 2. Etch trend data for etch rate, sidewall profile angle and depth uniformity. **A)** Baseline data for Cu and Ni masked SiC depicted for varying bias power while source power is kept constant, with low process pressure and SF_6 flow. **B)** Cu masked samples etch data, varying SF_6 flow at constant source and bias powers with low process pressure. **C)** Cu masked samples etch data, varying process pressure at constant source and bias powers with low SF_6 flow.

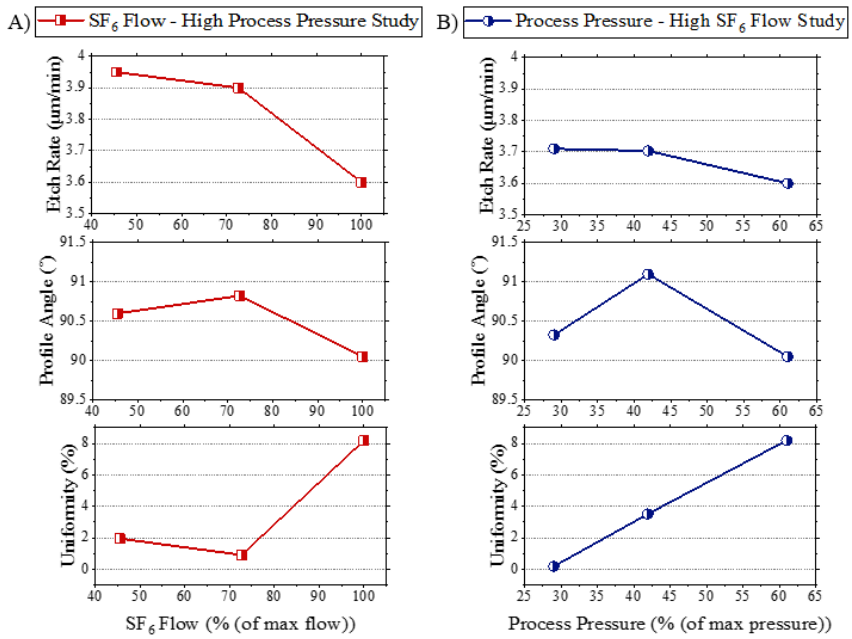

Fig. 3. Etch trend data for etch rate, sidewall profile angle and depth uniformity. **A)** Cu masked sample data for variable SF_6 flow with process pressure held at 60% of max and constant source and bias powers. **B)** Cu-masked sample data for variable process pressure with SF_6 held at 100% of max and constant source and bias powers.

Table 1. Process conditions influence on SiC etch rate.

Process Condition	*Low SF_6 Flow*	*High SF_6 Flow*
Low Process Pressure	➢ Low fluorine density in trench. ➢ Low mask resputtering. ➢ High trench redeposition removal. ❖ Low SiC etch rate.	➢ High fluorine density in trench. ➢ High mask resputtering. ➢ High trench redeposition removal. ❖ High SiC etch rate.
High Process Pressure	➢ High fluorine density in trench. ➢ Low mask resputtering. ➢ Low trench redeposition removal. ❖ High SiC etch rate.	➢ High fluorine density in trench. ➢ High mask resputtering. ➢ Low trench redeposition removal. ❖ Low SiC etch rate.

On-wafer temperature data obtained during etch processing using a thermal camera is shown in **Fig. 4.** with the temperature increasing with applied bias power. Between points **A)** and **B)** the temperature increase is minimal, but when the bias power is set to max (point **C**), the wafer temperature jumps dramatically. For SiC devices, certain metallizations such as Schottky contacts are temperature sensitive, depending on the metal, so understanding the relative temperature changes with etch parameters is valuable for a process intended to be performed post device fabrication. The impact of processing temperature on the fabricated devices is still proposed to be minimal due to the dicing etch being a backside process.

Additionally, measurements were taken of the Cu coated carrier wafer temperature (**D**, **E** and **F** on **Fig 4**). The slight temperature decrease of the carrier compared to the mounted pieces implies that on the pieces the underlying Cu mask layer, the bulk thickness of the mounted piece and the bonding agent are acting as insulating layers, slightly reducing the effect of the chuck cooling (set to -15°C). In production, mounted, thinned and masked SiC device wafers are expected to etch at a temperature somewhere between that of the carrier and piece as presented here.

Fig. 5. shows the result of an optimised SiC dicing etch prior to sidewall passivation removal using nitric acid. An etch rate of 4.2 μm/min was achieved at a process pressure of 87% of max, while maintaining low SF_6 flow and 67% bias. For an industry viable dicing process an etch rate of

5 µm/min is desirable to compete with saw dicing throughput, while maintaining effectively low process temperatures. However, given the imminent industry scale up of SiC to 200 mm substrates and the associated increase in yield, plasma dicing could realise a throughput advantage over conventional saw dicing. This is largely due to the requirement of saw dicing to individually dice each lane on the substrate.

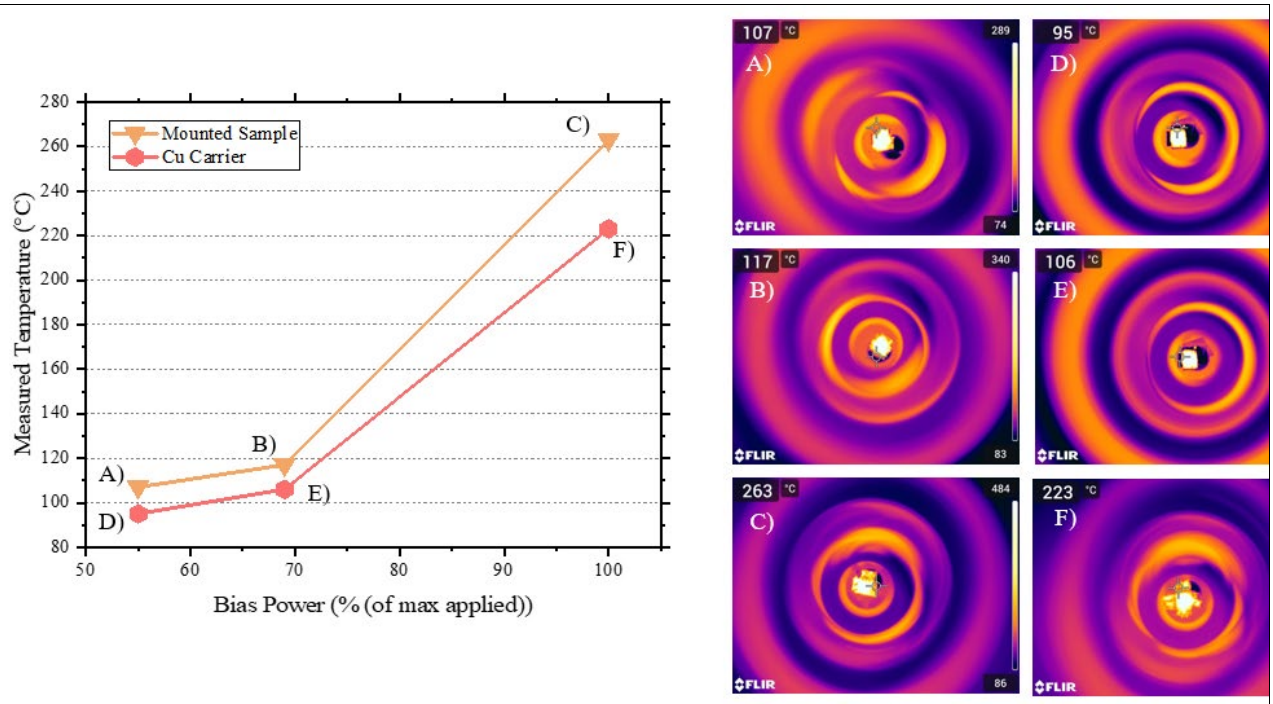

Fig. 4. Measured temperature data for Cu-masked bonded SiC samples and Cu carrier wafers using infrared imaging mid-process, for varying bias power. Infrared images shown inset with marker to the plot.

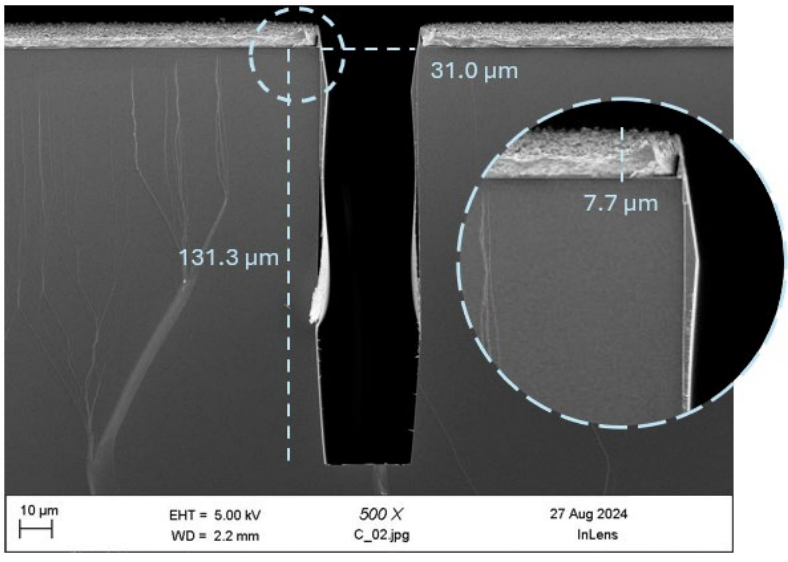

Fig. 5. SEM cross section of optimised SiC dicing etch, exhibiting an average etch rate of 4.2 µm/min, and 4.2% cross wafer uniformity while the Cu mask etch rate was ~0.15 µm/min.

SiC die were singulated using the etch process outlined in **Fig. 5.** The individual die can be seen in **Fig. 6. A)** prior to debonding from the Si carrier wafer. An example of a de-bonded, singulated die is depicted in **Fig. 6. B)** following mask and passivation removal.

More detailed sidewall topography can be seen in **Fig. 7. A)**, which compares die edge surfaces of saw-diced and plasma-diced samples. The evident machining damage and chipping on saw-diced

sample is understood to be typical of saw-diced SiC, and likely has a detrimental effect on the die strength. By contrast, the surface of the plasma-diced sample has very little evident surface damage.

Fig. 7. B) demonstrates the die strength improvement afforded by plasma dicing compared to saw dicing. The microcracks and abrasions caused by saw dicing likely act as sites of crack propagation, weakening the die. The improved die strength afforded to plasma dicing should translate to improved wafer-die yield were this processing method adopted by the industry.

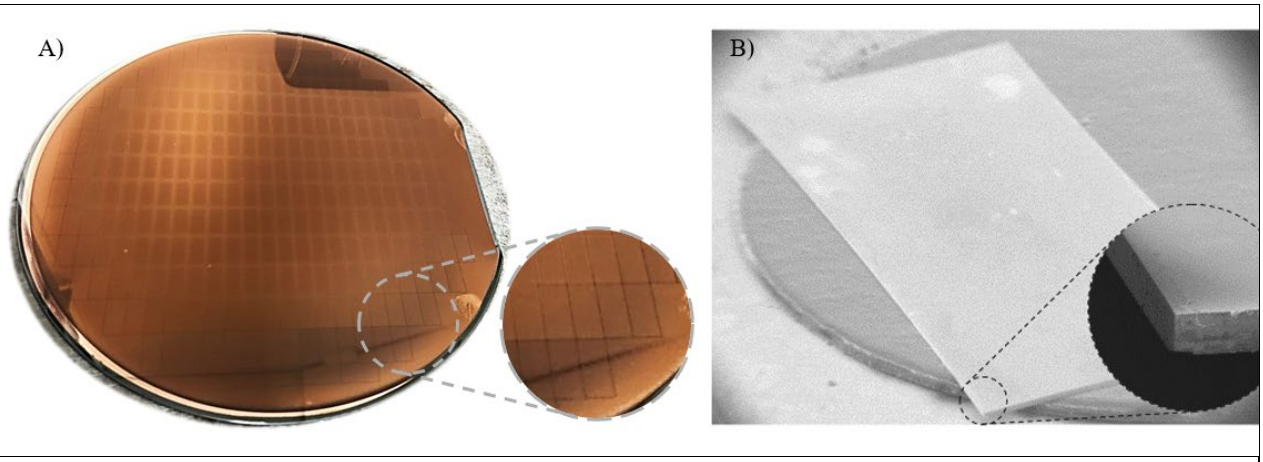

Fig. 6. A) Complete 150 mm Cu masked 100 µm thinned SiC wafer, bonded to a 350 µm Si carrier wafer, post singulation etch. The individual 5 × 10 mm die are visible, along with the 30 µm dicing lanes. **B)** SEM image of individual die, post etch following mask removal and passivation removal in nitric acid.

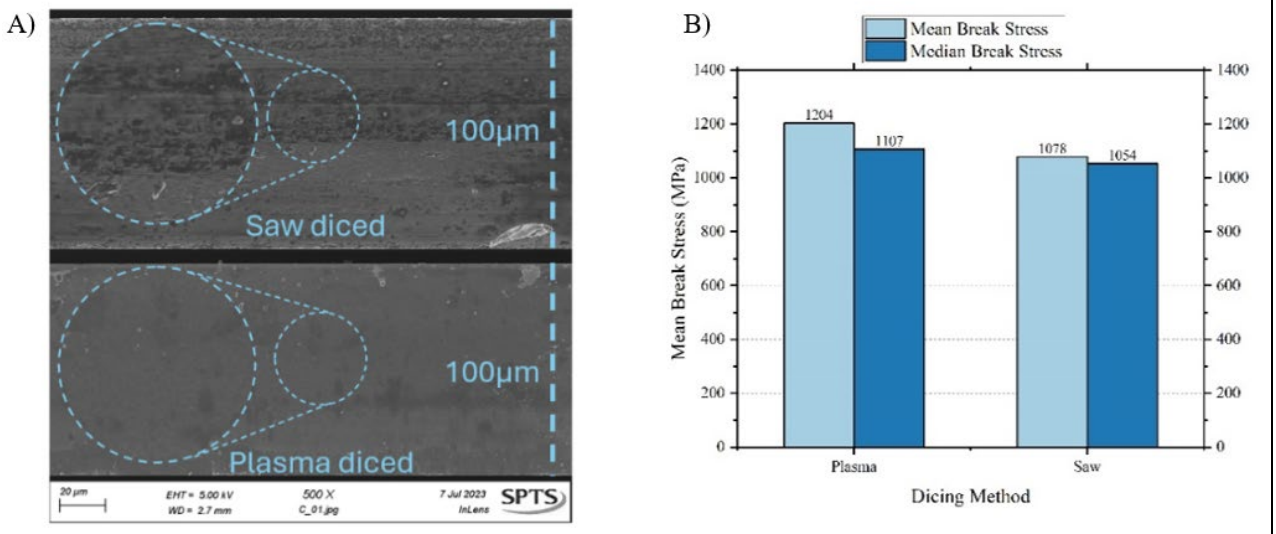

Fig. 7. A) SEM image side-view of saw-diced (top) & plasma-diced (bottom) SiC die. While handling debris is visible on both, there is also evident saw damage on the saw-diced sample. **B)** Plot comparing die break stress for plasma- and saw-diced samples. The plasma-diced die exhibited greater overall strength than their saw-diced counterparts.

Conclusion

The rapid advancements in SiC device processing, particularly for the power electronics sector mean that as issues are solved, new problems quickly become a focal point for industry. Efficient singulation of SiC devices is a targeted area for development, with projected yield improvements associated with plasma dicing, compared to saw dicing, as high as 14%. In this paper, a backside dicing process with an etch rate of 4.2 µm/min has been demonstrated. Processing temperature considerations have also been investigated – particularly the relationship between applied bias power

and on-wafer process temperature. Finally, the relative die strengths have been compared for saw- and plasma- singulated die. In this instance, we suggest that the vastly improved die edge surface smoothness is the defining factor in the improved die strength following plasma dicing.

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