

C-Face Epitaxy for Enhanced SiC Device Performance: Insights from Schottky Barrier Diodes

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Abstract. This study focuses on analyzing the electrical performance and characteristics of Schottky Barrier Diodes (SBDs) on the carbon face (C-face) epitaxial layer. The C-face epitaxial layer is grown on monocrystalline 4H-SiC and has a thickness of $\sim 11 \mu\text{m}$. It displayed minimal surface roughness, with an R_q of $\sim 0.3 \text{ nm}$. The C-face termination epitaxy was examined using grazing-angle X-ray photoelectron spectroscopy (XPS) analysis. SBDs were fabricated using a Ti/Al metal stack. Schottky Barrier Height (Φ_B) of about 1.2 eV was extracted from I - V measurements. Temperature-dependent I - V measurements demonstrated a forward voltage decrease as the temperature rises when the forward current is $< 1 \mu\text{A}$. However, for forward currents $> 1 \mu\text{A}$, the forward voltage increases with temperature. This rise in forward voltage could lead to a reduction in reverse recovery time and thus enhancing the switching speed. Additionally, the diode exhibits remarkable immunity to reverse leakage current up to 200°C , surpassing the performance of the 6.5 kV JBS diode on Si-face 4H-SiC [1].

Introduction

Wide-band gap (WBG) semiconductors are widely regarded as the building blocks for the future of power electronics devices. Among all WBG materials, 4H-SiC stands out as the most promising for power devices. Various types of devices fabricated on the Si-face of 4H-SiC have achieved a high level of technological maturity. However, the carbon-face (000 $\bar{1}$) crystallographic orientation offers significant advantages over the conventional Si-face, particularly in terms of enhanced thermal stability and carrier mobility [2]. The C-face of SiC exhibits fewer surface defects than Si-face.

Despite these advantages, device fabrication on C-face epitaxy has not been thoroughly explored to fully exploit the high electron mobility, superior switching characteristics, power efficiency, and expanded operational frequencies. Several factors play a part in the lack of motivation for development of C-face SiC devices such as the difficulty to achieve a reliable gate oxide layer with standard gate oxidation processes on C-face SiC due to the high oxidation rate. A poor gate oxide interface would compromise the device quality and negatively impact the performance of SiC devices. Among the different types of devices, Schottky diodes have shown remarkable performance as power diodes for fast switching applications, with minimal power loss. The overall performance of a Schottky diode is influenced by various conditions, including the semiconductor surface

characteristics, the metal work function used, and the metal-semiconductor interface [3,4]. The objective of this study is to investigate the electrical characteristics of a C-face epitaxially grown 4H-SiC using a Ti-based Schottky diode.

Results and Discussion

A 150 mm epi-ready n-type 4H-SiC substrate with a C-face orientation obtained from SOITEC, was used as the initial substrate for epitaxial growth. Subsequently, a 10 μm SiC epilayer was grown with C-face termination as visualized in Fig. 1(a).

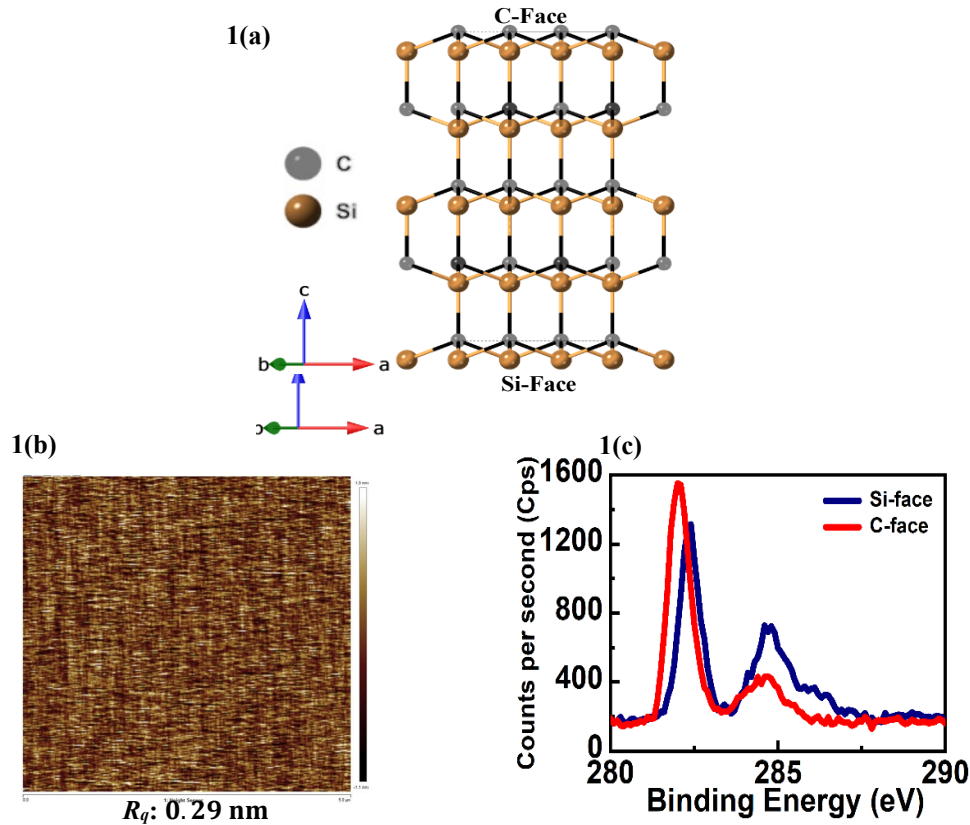


Fig. 1. (a) C-face 3D Crystal Structure, (b) Atomic Force Microscopy (AFM) image showing the surface morphology of the C-face epitaxial layer, (c) XPS analysis (C1s peak to peak ratio).

This growth utilized a standard buffer layer of approximately 0.5 μm and was performed in a commercial hot-wall chemical vapor deposition (CVD) system. Low surface roughness of the epitaxial layer with an R_q value of approximately 0.3 nm was obtained from atomic force microscopy (AFM) as shown in Fig. 1(b). To confirm the termination of the grown epitaxial layer, X-ray photoelectron spectroscopy (XPS) analysis revealed an increase in the carbon, peak-peak ratio of the two C1s peaks, indicating C-face termination outlined in Fig. 1 (c). This ratio was higher in comparison with another Si-face terminated grown epilayer. SBDs were fabricated as shown in Fig. 2 (a) with a Ti/Al metal contact. A sacrificial oxide layer was deposited on the frontside of the sample to ensure the interface remains clean when processing the backside Ni ohmic contact. A Ni ohmic backside contact was formed through PMDA at 950 $^{\circ}\text{C}$. The sacrificial oxide layer on the frontside was then stripped with dilute hydrofluoric acid (DHF) followed by subsequent metallization right after. This maintained the integrity of the MS interface prior to metallization. SiO_2 was then removed with DHF, followed by Ti/Al deposition in a commercial physical vapour deposition (PVD) chamber right after. The thickness and integrity of the metal-SiC (MS) interface was observed with TEM as shown in Fig. 2 (b). An atomically smooth Ti/SiC interface layer was observed. A Ni ohmic contact was formed on the backside of the device after post-metal deposition annealing (PMDA) at 950 $^{\circ}\text{C}$, prior to Ti/Al Schottky contact deposition [5].

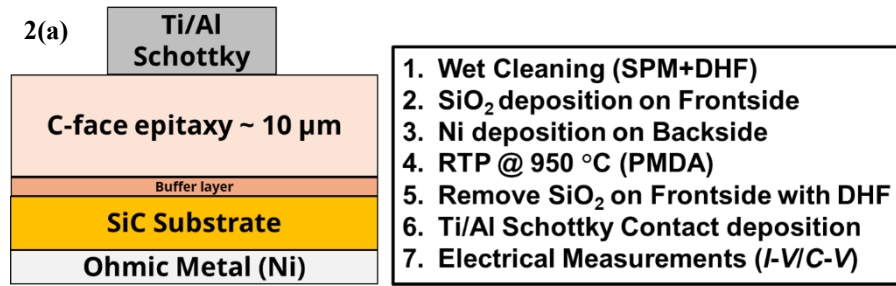


Fig. 2. (a) Schematic of the Schottky Barrier Diode fabrication process, highlighting the Ti/Al metal contact and post-metal deposition annealing steps.

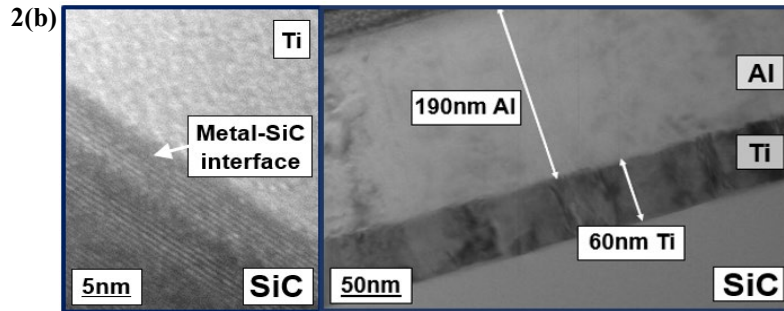


Fig. 2. (b) Transmission Electron Microscopy of Metal-SiC Interface.

The doping concentration ($9.6 \times 10^{15} \text{ cm}^{-3}$) of the C-face epilayer was extracted electrically from the measured C - V of SBDs in Fig. 3 (a-b) [6]. C - V was measured at 1 MHz on radius 100 μm devices. From the linearity of the $1/C^2$ vs V plot, uniform doping can be deduced across the 150mm wafer. Table 1 shows the barrier height extracted from several SBDs using I - V techniques with good uniformity and distribution. The barrier heights correlate to the increased knee voltage (V_{knee}) observed from I - V plots shown in Fig. 4 (a-b).

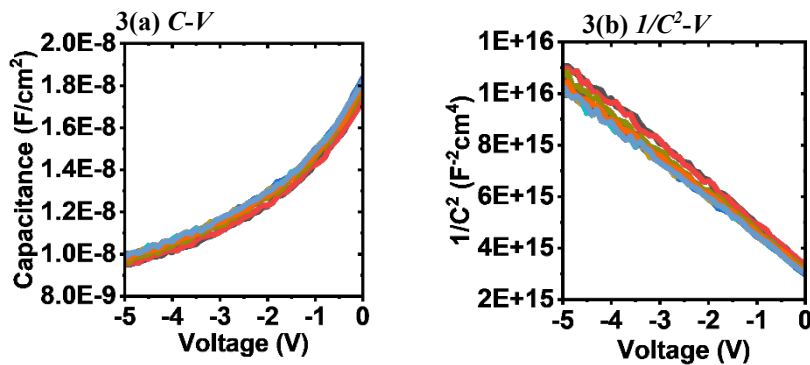


Fig. 3. (a) C - V of 5 Devices (b) $1/C^2$ vs V .

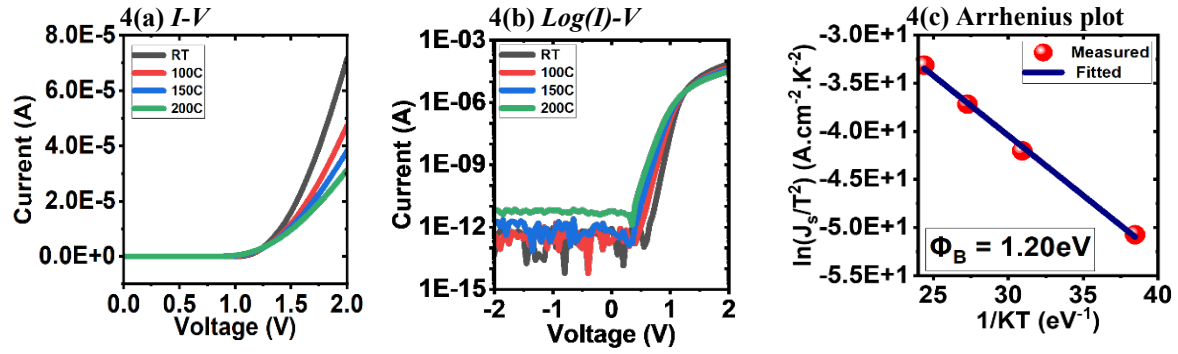


Fig. 4. (a) Linear I - V , (b) $\text{Log}(I)$ - V , (c) Arrhenius plot.

Table 1. Φ_B obtained from 5 devices, Table 2: I_s vs Temperature.

Table 1		Table 2	
As Deposited/Room Temperature	Φ_B [eV] from I - V	Temperature	Saturation Current (I_s) [A]
Device 1	1.15	Room Temperature	4.6E-14
Device 2	1.20	100°C	9.4E-14
Device 3	1.15	150°C	3.13E-13
Device 4	1.22	200°C	6.15E-12
Device 5	1.19		

Furthermore, from the SBDs I - V characterizations, we derived the barrier height from Arrhenius plots and demonstrated its strong correlation with data obtained from I - V extraction. Our findings closely matched those of a previous study (1.97 eV) for Ni-based materials, whereas this study, focused on Ti-based materials (1.15 eV) [3]. This variance can stem from the use of different metal stacks and doping concentrations of the C-face epi layer, which would influence the barrier height. The SBDs fabricated on C-face epitaxial layers demonstrated significantly low leakage current, less than 6pA, even at elevated measurement temperatures up to 200 °C as shown in Table 2. Forward current was observed to be lowered with increased temperature in Fig. 4(a). This change in the forward current could be caused by increased phonon scattering at high temperatures. The strong bonding force promotes large lattice vibrations, making excitation of donors difficult. Current enhancement in the subthreshold region as seen in Fig 4(b) could indicate that the thermal emission is encouraging this change. We observed a remarkable immunity to reverse leakage increase with temperature, which is superior to 6.5 kV JBS diodes fabricated on Si-face 4H-SiC [1].

Conclusion

In this work, we have demonstrated the electrical characteristics of SBDs on C-face epitaxy substrates with excellent mobility and slight increase in barrier height with temperature. Immunity against temperature dependent reverse leakage current was observed and attributed to the high quality C-face epitaxial grown layer as well as the clean metal-semiconductor interface before metallization. Lowered forward current with increasing temperature as a possible result of increased phonon scattering with high temperature was also observed and discussed. This work demonstrates the viability of implementing Schottky diodes on C-face epitaxial layers to exploit its excellent intrinsic material properties in comparison with Si-face devices.

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