

Investigation on Bipolar Degradation Caused by In-Grown Stacking Fault in 3.3 kV SiC-MOSFET

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Abstract. This study investigates the role of in-grown stacking faults (SF) in the bipolar degradation of 3.3 kV SiC-MOSFETs, emphasizing their significant contribution to both on-resistance (V_{DSon}) and leakage current (I_{DSX}) degradation. A high current stress was applied to over 1,500 chips, resulting in 72 degraded devices, with 45 exhibiting notable I_{DSX} degradation. A detailed analysis revealed that most I_{DSX} degraded chips contained bar-shaped in-grown SFs, suggesting a correlation between these defects and leakage current degradation. These findings indicate that peculiar basal plane dislocations associated with in-grown SFs may be critical contributors to I_{DSX} degradation, indicating the need for further research to elucidate the mechanisms behind this degradation in SiC-MOSFETs.

Introduction

For many years, bipolar degradation has been one of the most important reliability issues in SiC-MOSFETs [1-3]. In this phenomenon, Shockley-type stacking faults (SSFs) expand from basal plane dislocations (BPDs) during bipolar operation. For SiC-MOSFETs, this occurs during conduction through the body diode (BD), which leads to an increase in the on-resistance or forward voltage drop (V_{DSon} of the MOSFET and V_{SDon} of the BD) and/or the leakage current during blocking mode (I_{DSX}) [4]. Most studies have focuses on V_{DSon} degradation, with very few addressing I_{DSX} degradation [4-7]. I_{DSX} degradation does not always occur when SSFs expand, and its origin remains unclear.

Recently, expanded SSFs from BPDs gliding out from micropipes have been found to cause I_{DSX} degradation after stressing more than 1,500 MOSFETs and analyzing degraded chips [8]. Indeed, all the I_{DSX} degradations were attributed to SSFs originating from micropipes; they did not occur in SSFs from commonly observed BPDs within the substrate. A similar phenomenon has been observed in a few studies on I_{DSX} degradation, which occurred in PiN diodes with half-loop arrays or BPDs owing to implantation damage [5, 6]. Therefore, I_{DSX} degradation appears to occur in SSFs originating from some peculiar BPDs, such as interfacial dislocations or half-loop arrays, but not from SSFs expanding from BPDs inside the substrate.

Although peculiar BPDs may be the cause of I_{DSX} degradation, the question remains as to whether other defects may cause it. In this study, we identify defects causing I_{DSX} degradation in addition to known ones, such as micropipes. High-current stress was applied to the BD of 3.3 kV SiC-MOSFETs, and chips with bipolar degradation were identified. These degraded MOSFETs, especially the I_{DSX} degraded MOSFETs, were analyzed in detail, and the crystal defects responsible for this degradation phenomenon were identified.

Experimental

Figure 1 (a) shows the planar-type 3.3 kV SiC-MOSFET fabricated on an n^+ -type 4H-SiC substrate prepared in this study. The size of the MOSFET was approximately $9 \times 8 \text{ mm}^2$. A different substrate vendor was used compared to the one in the previous study [8]. As the types and densities of crystal defects within the substrate differed by vendor, there is a higher possibility of obtaining new insights into the degradation phenomenon. During device fabrication, defect inspection using photoluminescence (PL) was performed after epitaxial growth and activation annealing. Figure 1 (b) illustrates the experimental flow of this study. After the device fabrication, an initial chip test was conducted to select “good” chips for the BD experiment. These “good” chips exhibited no abnormal I - V characteristics or signs of degradation. Subsequently, a high DC current stress of 300 A/cm^2 at $\sim 175^\circ\text{C}$ was applied to the BD of each chip. In the following chip test, chips with increased leakage current compared to the initial test were characterized as “ I_{DSX} degraded chips,” while those showing only an increase in V_{DSon} (without I_{DSX} degradation) were characterized as “ V_{DSon} degraded chips.”

For the failure analysis of V_{DSon} degraded chips, PL imaging was performed after removing the electrodes and gate structures to analyze the expanded SSF. For I_{DSX} degraded chips, the points of abnormal leakage were first identified using photoemission microscopy from the backside of the chip after removing the backside electrode. PL imaging was then performed after removing the frontside electrode and gate structures to analyze the expanded SSF. The results of photoemission microscopy and PL imaging were overlaid to identify the crystal defects causing abnormal leakage. For both types of degraded chips, the defect inspection results from the device fabrication process were reviewed, and the crystal defects responsible for the degradation were determined.

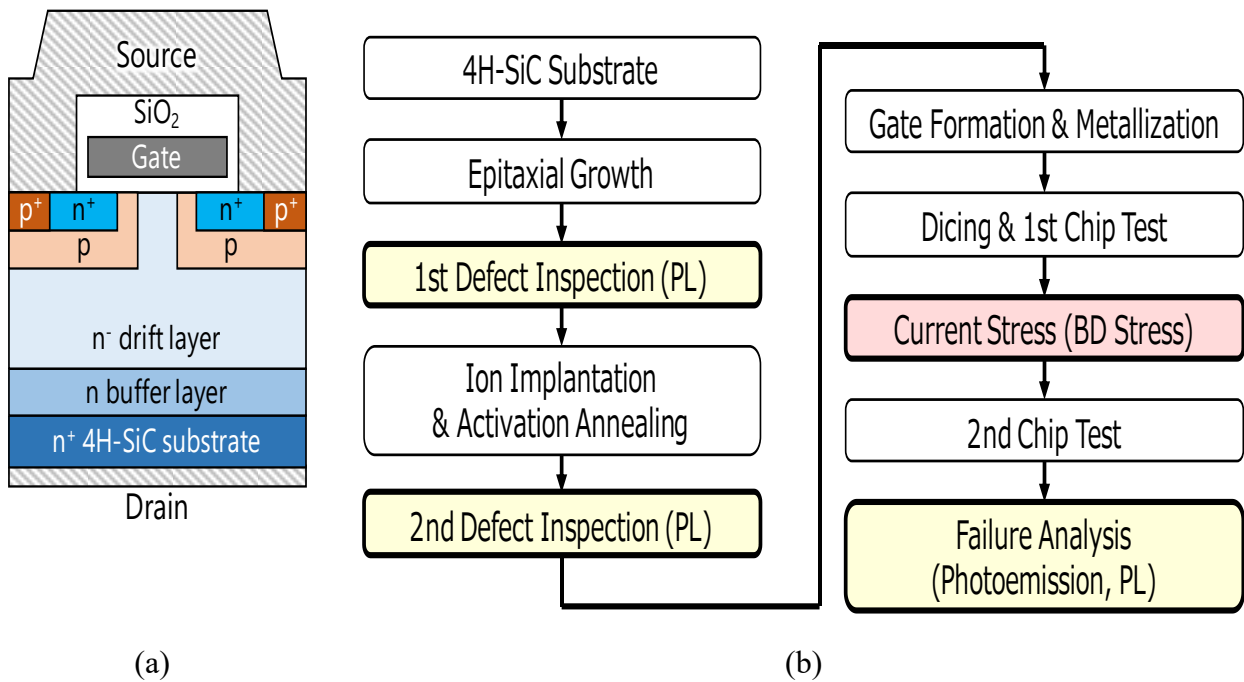


Fig. 1. (a) Schematic cross-section of the planar-type 3.3 kV SiC-MOSFET investigated in this study. (b) Flow-chart of the experimental procedure. During failure analysis, photoemission microscopy and PL imaging were conducted to identify the crystal defects.

Result of Body Diode Stress Test

In this study, body diode stress was applied to more than 1,500 chips, and 72 were found to be degraded: 27 chips exhibited V_{DSon} degradation with no I_{DSX} degradation observed, and 45 chips exhibited I_{DSX} degradation. Figure 2 shows the I - V characteristics of some of the I_{DSX} degraded chips, where an abnormal leakage current can be observed. Failure analysis was conducted on these degraded chips to identify the origin of the degradation.

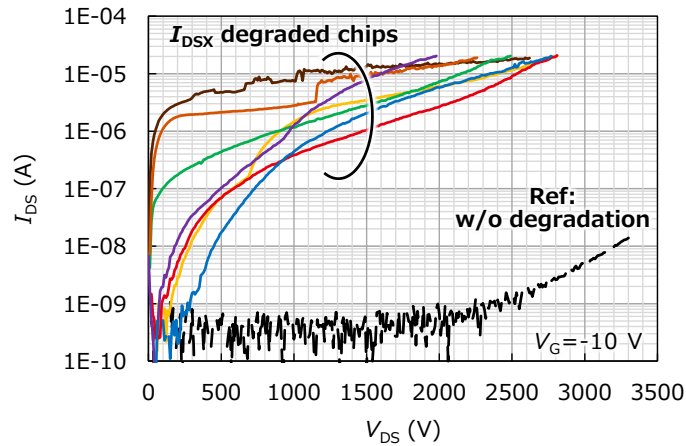


Fig. 2. Leakage current characteristics of I_{DSX} degraded chips. The compliance current in the measurement was set to 20 μ A.

Analysis of Chips with Bipolar Degradation

V_{DSon} Degraded Chips.

PL imaging was conducted on all V_{DSon} degraded chips, and the origin of the expanded SSFs was analyzed. Some of the PL images are presented in Fig. 3. Although most SSFs were caused by BPDs within the substrate (Fig. 3 (a)) or micropipes (Fig. 3 (b)), approximately 18% of the SSFs were attributed to in-grown stacking faults (SFs) (Fig. 3 (c)). In the PL image, the black SFs represent the in-grown SFs, while the white SFs represent the expanded SSFs. Such an expansion from an in-grown SF has been reported in recent years, where a BPD included in an in-grown SF became the nucleation source of SSFs [9]. The proportion of SSFs caused by in-grown SFs is significant and is a major contributor to V_{DSon} degradation.

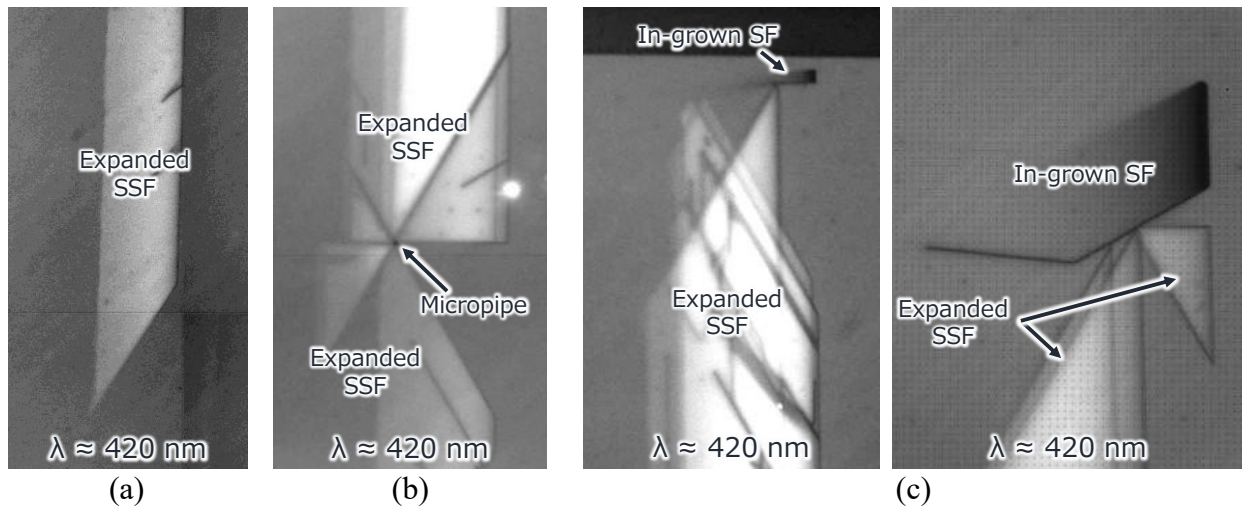


Fig. 3. PL images of V_{DSon} degraded chips with various origins of SSF. (a) SSF caused by BPDs within the substrate. (b) SSF caused by micropipe. (c) SSF caused by in-grown SF.

I_{DSX} Degraded Chips.

Initially, the defect inspection results were reviewed to select chips for detailed analysis. Table 1 list the defect inspection results for each I_{DSX} degraded chip. Notably, most chips did not contain micropipes, as in a previous study [8], yet I_{DSX} degradation still occurred. Upon closer examination, most chips were found to contain a bar-shaped in-grown SF, as shown in Fig. 4 (a). For those chips without bar-shaped in-grown SFs, triangular in-grown SFs were still present, as shown in Fig. 4 (b), suggesting in-grown SF has also caused the I_{DSX} degradation. Therefore, some chips with bar-shaped in-grown SFs and all chips without bar-shaped in-grown SFs were selected for analysis to confirm it.

Table 1. Defect inspection results of I_{DSX} degraded chips.

	With micropipe	2 pcs
Without micropipe	With bar-shaped in-grown SF	38 pcs
	Without bar-shaped in-grown SF	5 pcs

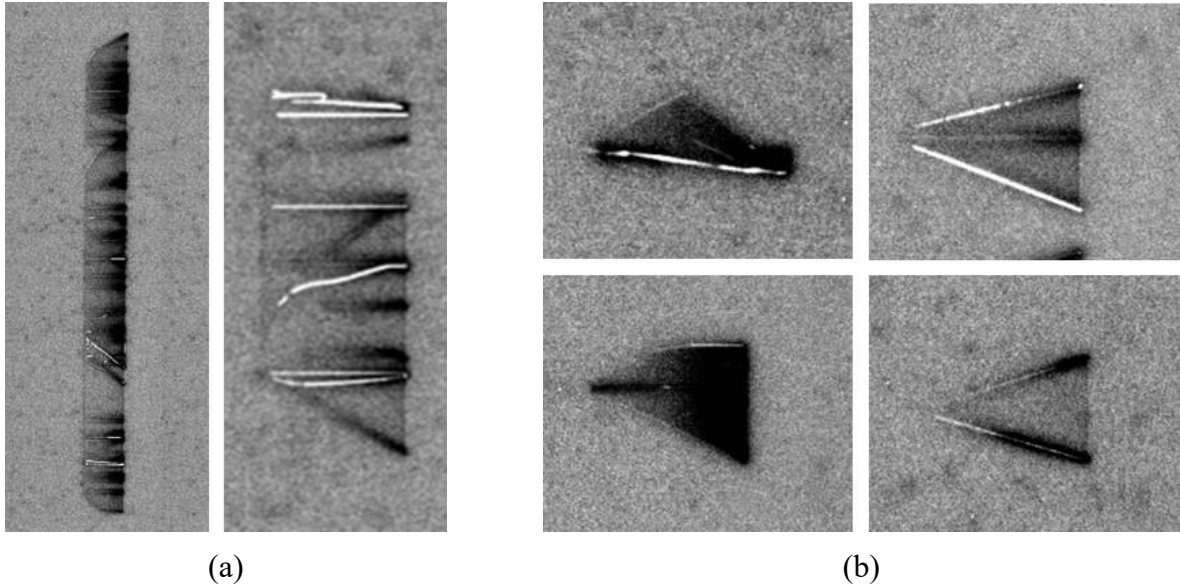
**Fig. 4.** PL images of in-grown SF obtained by the defect inspection ($\lambda > 660$ nm) during device fabrication. (a) Bar-shaped in-grown SF. (b) Triangular in-grown SF.

Figure 5 shows the failure analysis results of the I_{DSX} degraded chips. The I_{DSX} degraded chips were analyzed using photoemission microscopy and PL imaging to identify the source of abnormal leakage. In this chip, there was no micropipe, but a bar-shaped in-grown SF was present. After the BD stress, a white bar-shaped SF indicating the expanded SSFs was observed, having expanded from the bar-shaped in-grown SF. This indicates that bipolar degradation occurred because of the in-grown SF. Furthermore, the results of photoemission analysis revealed that abnormal leakage occurred along the black lines inside the bar-shaped SF, indicating that I_{DSX} degradation also occurred because of the bar-shaped in-grown SF.

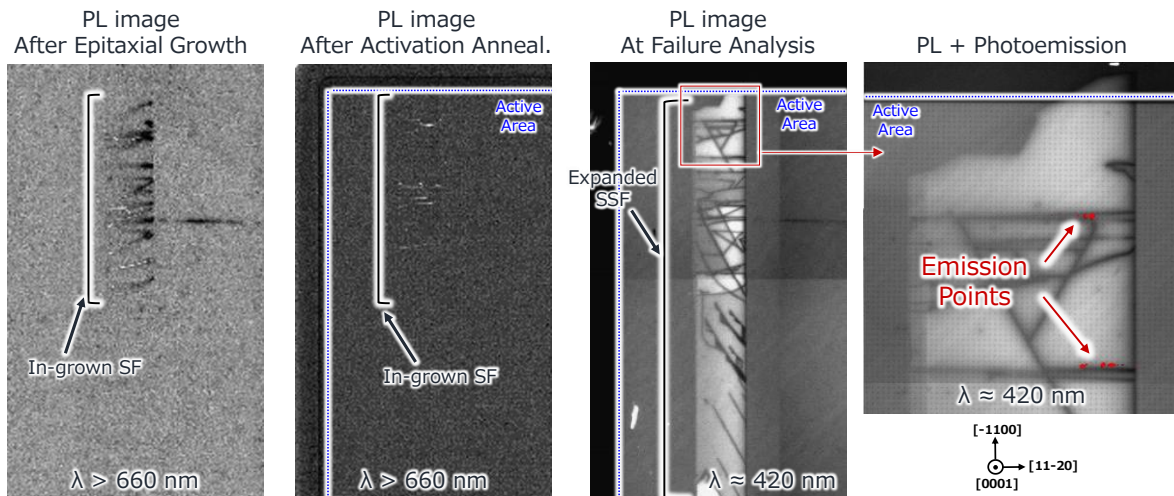
**Fig. 5.** PL images and photoemission microscopy results of I_{DSX} degraded chip with bar-shaped in-grown SF.

Figure 6 shows the analysis results of the other I_{DSX} degraded chips. As shown in Fig. 6 (a), there was a bar-shaped in-grown SF. However, after the BD stress, the long bar-shaped SSF expanding outside the in-grown SF was not observed, as shown in Fig. 5. Nevertheless, abnormal leakage occurred inside the in-grown SF. Although the bar-shaped SSF was not observed, SSFs other than the bar-shaped may have expanded inside the in-grown SF, causing the leakage current degradation for this chip. Because the expanded SSFs and in-grown SF may overlap, it was difficult to observe the SSFs. As shown in Fig. 6 (b), there was a triangular in-grown SF, but not a bar-shaped one. After the BD stress, a triangular SSF expanded outside the in-grown SF, and multiple emission points were observed inside the in-grown SF.

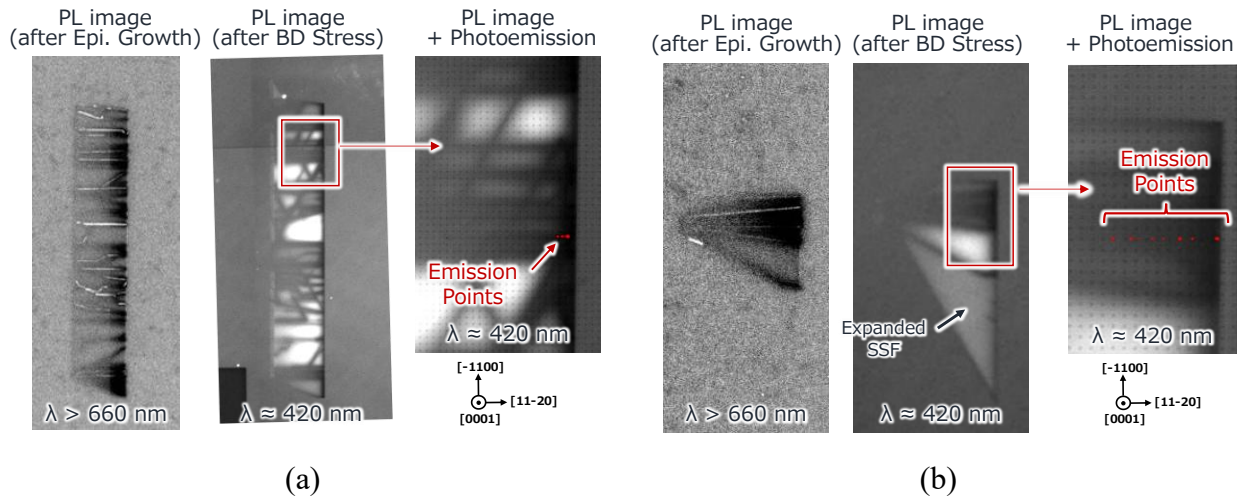


Fig. 6. PL images and photoemission microscopy results of I_{DSX} degraded chip. (a) Chip with bar-shaped in-grown SF, but without SSF expanding outside it. (b) Chip with triangular in-grown SF.

A total of 10 I_{DSX} degraded chips were analyzed. It was confirmed that all the abnormal leakage occurred from in-grown SFs in various ways, as shown in Figs. 5 and 6, regardless of the shape or expansion behaviors of the in-grown SFs and SSFs. All the chips without the bar-shaped in-grown SFs exhibited abnormal leakage from triangular in-grown SF. This indicates that most of the I_{DSX} degradation observed in this study was also due to in-grown SFs, as most of the degraded chips contained a bar-shaped in-grown SFs inside the chip. Moreover, in this study, all chips containing bar-shaped in-grown SFs exhibited I_{DSX} degradation after BD stress. By contrast, most triangular in-grown SFs did not induce I_{DSX} degradation. These results indicate that bar-shaped in-grown SFs are major contributors to I_{DSX} degradation.

Discussion

From the analysis of I_{DSX} degraded chips in the previous section, it was found that in-grown SFs can cause I_{DSX} degradation. This raises the question of whether there are similarities with previous reports. In the case of I_{DSX} degradation caused by micropipes, abnormal leakage occurred at the SF originating from BPDs gliding out of the micropipe [8], which were referred to as peculiar BPDs. Therefore, the defect inspection results of in-grown SFs causing I_{DSX} degradation were re-examined to confirm whether such BPDs existed in this study. Figure 7 shows an enlarged view of the bar-shaped in-grown SFs depicted in Fig. 5. White lines moved after activation annealing, indicating the gliding of BPDs. This suggests that peculiar BPDs, likely interfacial dislocations, were also observed inside in-grown SFs. In fact, all bar-shaped in-grown SFs of the I_{DSX} degraded chips were re-examined, and it was found that most of them contained gliding BPDs inside the in-grown SF. Therefore, SSFs originating from peculiar BPDs accompanied by the in-grown SFs may have caused

the abnormal leakage, similar to the case of micropipes. In the case of chips with bar-shaped in-grown SFs without gliding BPDs, this may be because the gliding BPDs and some portion of the in-grown SFs have overlapped, making it difficult to observe them during defect inspection. However, these results further suggest that certain peculiar BPDs are responsible for I_{DSX} degradation. More studies will be needed to identify the specific structure of these BPDs or SSFs that induced abnormal leakage to clarify the origin of the leakage current degradation.

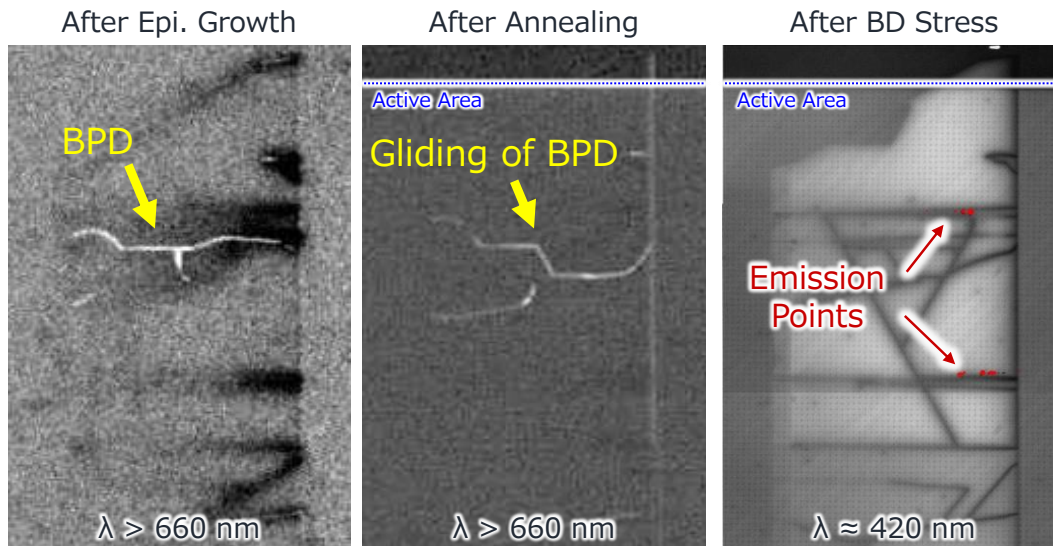


Fig. 7. Enlarged view of the bar-shaped in-grown SF causing I_{DSX} degradation shown in Fig. 5.

Summary

This study investigated the impact of in-grown SFs on bipolar degradation in 3.3 kV SiC-MOSFETs, identifying these as significant contributors to I_{DSX} degradation. A comprehensive analysis of over 1,500 chips subjected to high-current stress revealed that 72 devices exhibited degradation, with 45 specifically exhibiting I_{DSX} degradation. A detailed failure analysis indicated that most I_{DSX} degraded chips contained bar-shaped in-grown SFs, suggesting a link between these defects and abnormal leakage currents. This study highlighted the potential role of peculiar BPDs associated with in-grown SFs in the degradation process. These findings underscore the necessity of further research to elucidate the mechanisms underlying the bipolar degradation in SiC-MOSFETs.

References

- [1] A. Galeckas, J. Linnros, and P. Pirouz, Appl. Phys. Lett., vol.81 (2002), p. 883.
- [2] M. Skowronski and S. Ha, J. Appl. Phys., vol. 99 (2006), p. 011101.
- [3] K. Konishi, S. Yamamoto, S. Nakata, Y. Nakanishi, T. Tanaka, Y. Mitani, N. Tomita, Y. Toyoda, and S. Yamakawa, J. Appl. Phys., vol. 114 (2013), p. 014504.
- [4] A. Agarwal, H. Fatima, S. Haney, and S.-H. Ryu, IEEE Electron Device Lett., vol. 28 (2007), p. 587.
- [5] R. Stahlbush, Q. Zhang, A. Agarwal, and N. A. Mahadik, Mater. Sci. Forum, vol. 717-720 (2012), p. 387.
- [6] S. A. Mancini, S. Y. Jang, Z. Chen, D. Kim, J. Lynch, Y. Liu, B. Raghothamachar, M. Kang, A. Agarwal, N. Mahadik, R. Stahlbush, M. Dudley, and W. Sung, Proc. IRPS 2022, p. 62-1.

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- [7] T. Ishigaki, T. Murata, K. Kinoshita, T. Morikawa, T. Oda, R. Fujita, K. Konishi, Y. Mori, and A. Shima, Proc. ISPSD 2019, p. 259.
 - [8] H. Niwa, T. Tanaka, K. Ishibashi, H. Amishiro, A. Imai, Y. Kagawa, K. Sugawara, and T. Watahiki, Solid State Phenomena, vol. 375 (2025), p. 63.
 - [9] E. Kodolitsch, A. Kabakow, V. Sodan, M. Krieger, H. Weber, and N. Tsavdaris, J. Phys. D: Appl. Phys., vol. 56 (2023) p. 315101.