Materials Science Forum
ISSN: 1662-9752, Vol. 1190, pp 19-25
doi:10.4028/p-2nuhGa
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Submitted: 2025-09-11
Revised: 2025-12-24
Accepted: 2026-02-23
Online: 2026-05-18

Process-Dependent Photoluminescence Behavior Evolution of Stacking Faults in 4H-SiC

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Keywords: stacking faults, device failure, defect, ion implant, photoluminescence, yield.

Abstract. The yield of power electronic devices is influenced by many factors including crystal defects like stacking faults (SFs). There are different types of stacking faults but their influence on the finished device and its performance and the behavior of SF during processing is not fully understood yet. With our contribution, we shed light on the issue, showing four different optically characterized subtypes of SFs with different electrical behavior that can already be found after implantation and wafer annealing in photoluminescence (UVPL) imaging. This enables a distinction between different SF classes without the need for a finally processed device and the corresponding electrical characterization. The goal of this paper is to illustrate an alternative for subdividing SF types that would otherwise be detected as triangular defects without any distinction and to show the different effects those subclasses have on finished devices with non-destructive methods that can be used in between device manufacturing steps. These results will be used as basis for further studies to confirm the found classes and to compare them with research about the different crystal structures by spectral PL measurements. For better understanding of the effect on the finished device, the PL imaging data is correlated with I-V characteristics of trenched diodes and the defect types are evaluated on their effect on the I-V characteristic, identifying 3 defect types with detrimental influence on the reverse bias and blocking voltage while the forward bias characteristic and I-V characteristic of one type is not effected by the defects.

Introduction

Stacking faults (SFs) are well-known to be a limiting factor for the device yield of power electronic devices fabricated on SiC. They occur on 4H-SiC substrates and epitaxial layers as Shockley and Frank type stacking faults, as single or multiple stacking faults and form complexes such as the carrot defect [1,2]. Previous studies have reported [3,4] that some SF types can affect device performance and cause failure of devices, however which specific SF types cause electrical failure remains insufficiently understood. For instance, Baierhofer et al. [5] indicated that only approximately 66% of the defects identified by UVPL imaging as SFs without polytype inclusion will kill a SiC MOSFET device. Further, these defects result in different failure mechanisms. This finding indicates the necessity for a more detailed subclassification in addition to the known SF types of these defects and the investigation of process steps like implantation on the SF. This requires repeated in-line defect characterization and subsequent correlation with electrical data for better understanding of SF progression during device processing and final device performance.

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Experimental

We prepared eleven 150 mm SiC Wafers for pin diode fabrication with a standard 1200 V epitaxial layer with 13 µm thickness and a doping concentration of 9E+15 cm^{-3}. After epitaxy and trench formation, they received implantation steps. A patterned nitrogen contact (n+) as well as aluminum FFR (p+) and aluminum contact (p+) implantations with 0° was used. However, two wafer received this implantation under 17° tilt. Subsequently implant annealing was performed at 1700° for 30 min. The diodes were investigated repeatedly with various imaging methods utilizing the PL channel of the Lasertec SICA88 tool at different steps of processing. PL images were recorded on the substrates, after epitaxy and again after ion implantation and annealing. The samples were illuminated with a Hg-Xe lamp at an excitation wavelength of 313 nm. A 650 nm longpass filter was applied in front of the detector. The finished devices were then electrically characterized using I-V mapping on four different wafers. Over 30 devices of different designs and with and without defects were compared to get insight on the effect of the different defect types on device performance.

Results

PL Imaging of epilayers.

In the as grown epilayer, the SFs appear as dark triangles in the UVPL images of the PL channel of the SICA. After implantation and anneal, we observed a change in the luminescence signal. Thus, we identified four different subgroups of SF according to the UVPL signal. One example of each defect types (A-D) after epitaxy and after implant anneal are shown in figure 1.

PL Imaging after implant and anneal.

After ion implantation and annealing, type A SF can be seen as a bright triangle. Type B appears as dark triangles with a darker surrounding area. Type C defects can be described as dark triangles with partially bright luminescent segments. Group D defects appear as bright triangles with a dark surrounding field, pointing towards a combination of type A and B defects. Additionally, we were able to locate the exact position of the defects within the device which allows exclusion of these SF for electrical characterization which are not located within the active-area.

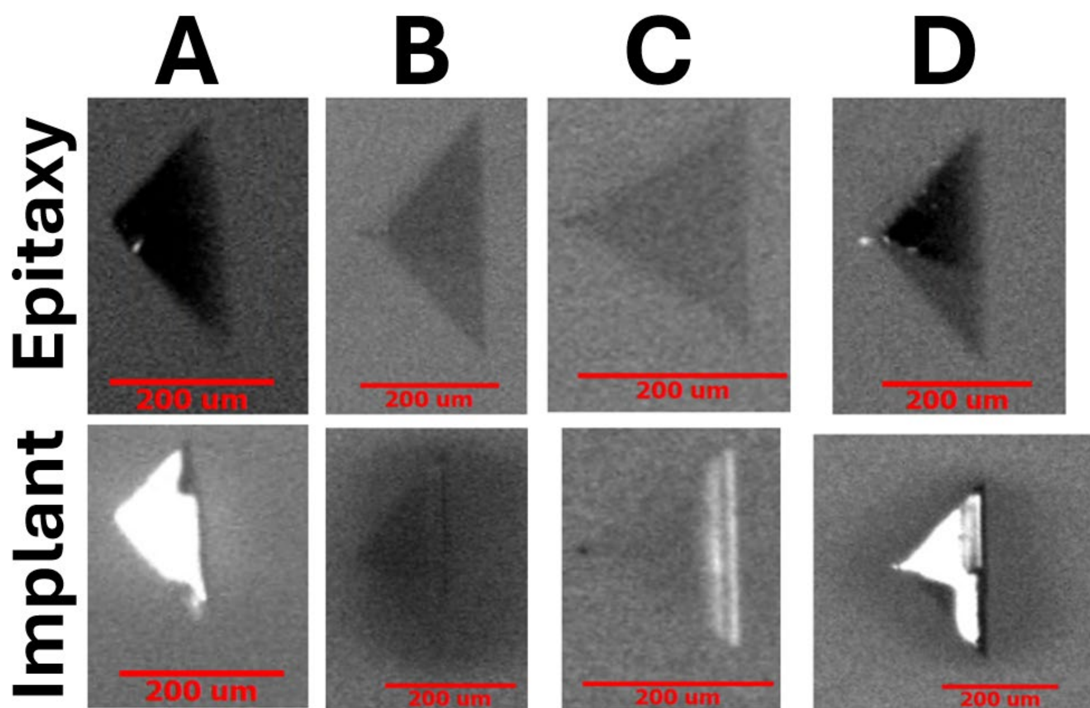

Fig. 1. PL images from the Lasertec SICA for each defect type after epitaxy as well as after implant and anneal. Each defect type shows a different luminescence signal after the anneal while after epitaxy each defect appears as a dark triangle.

To compare the quantity of each defect type on the wafers, defects were counted in the PL images and assigned to the suitable SF type based on the visual criteria that were described above. A key challenge in process-accompanying SF analysis is choosing an imaging method that allows the same SF to be consistently located at each step, even across a large defect population. Therefore, defects in the PL images taken after epitaxy were correlated to the images after implant and anneal based on the coordinates on the wafer. This was possible due to the high accuracy of the automatic wafer alignment without the need of further adjustment of the scans and data. While the total number and local distribution of defects differs from wafer to wafer, counting from 10 defects per wafer to over 100, overall, a total number of 396 defects were evaluated. The occurrence of each defect type per wafer in percent is displayed in the bar plot in figure 2. The least common defect type on all wafers is the bright triangle type A, followed by the dark defect with surrounding dark area type B and type C. On wafer 4, 5, and 7 defect type A could not be detected at all. Overall, the most common defect type is D across all wafers except wafers 6 and 8. This finding is coincidental with the implantation angle of 17° that was only used for these two wafers.

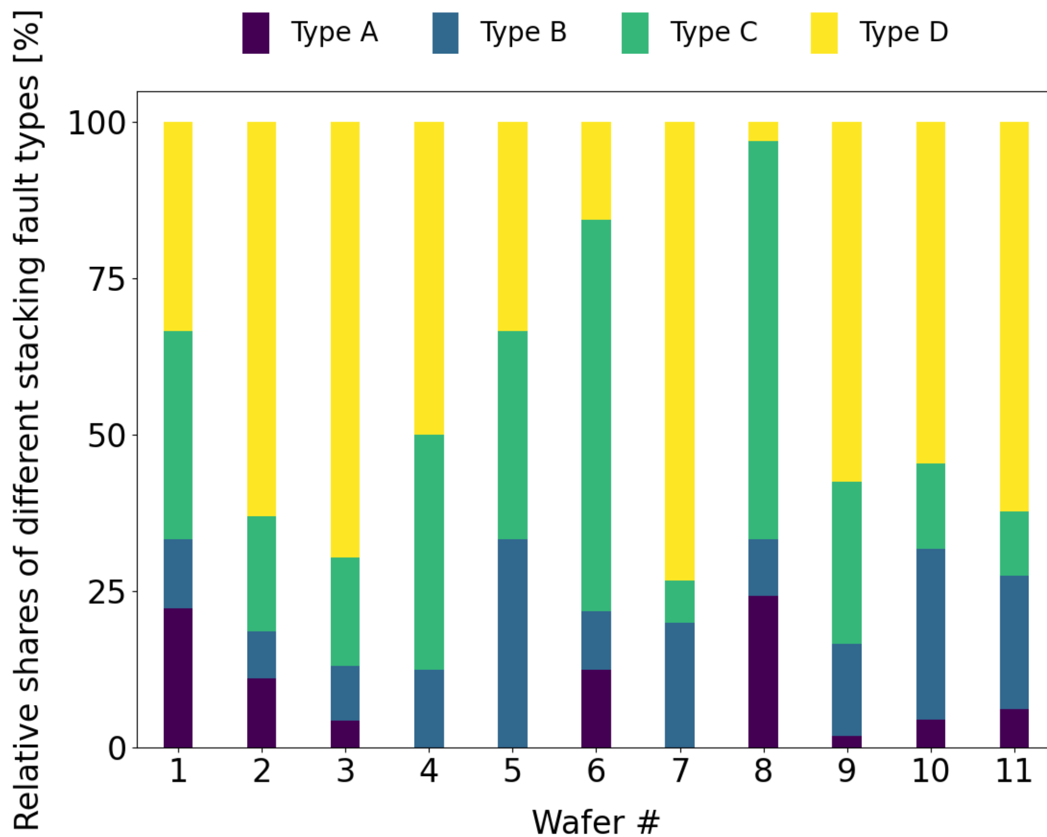

Fig. 2. Ratios of defect type A, B, C and D on eleven wafers in percent. The data was generated by counting each defect type. The absolute number of defects varied for each wafer between 10 and 100 defects per wafer.

Dark triangles with bright segments dominate as defects on wafers 6 and 8, whereas number of type D SF on these wafers was comparably low. This indicates that the implantation angle may have an impact on the formation of this defect subtype. However, given the limited number of defects and wafers, this observation lacks statistical significance. Nevertheless, in our present dataset the correlation appears too clear to be ignored. In existing studies, to the influence of the implantation an angle of 17° degree is connected to the implantation along the $[1\bar{1}23]$ direction of the silicon carbide lattice resulting in channeling and higher implantation depths.[6] We therefore plan additional studies to improve the statistical foundation, but also to investigate other parameters like different implantation angles, temperature, ion energy and dose.

Electrical Characterization

To investigate effects associated to the different SF types on the device performance we characterized electrically the wafers by measuring I-V characteristics of each device. We analyzed I-V curves for almost 100 devices with defects and compared them to defect free devices. The remaining defects were removed from the statistics because they were not located in active device area. Future analysis of more defects and devices will provide more statistical support for these results. In figure 3 the reverse bias characteristic is shown for all four defect types and four reference devices without any SF. Curves of the reference devices typically are within the range of the plotted characteristics of the three examples. For forward bias, the characteristics from devices with or without defects were similar and did not show any differences or noteworthy effect. Devices that contained a visible SF of type A, B and D in the PL images showed a much lower breakdown voltage compared to devices without SFs (black curves). Defectfree devices upheld up to a voltage of about 700 V, while those with a SF exhibit a break down below 100 V reverse bias. The most detrimental effect on the breakdown voltage was observed for devices with type D SFs with an almost instant breakdown under reverse bias. Type C SFs did not appear to influence the breakdown voltage, as the I-V characteristics of devices with and without this defect type overlapped.

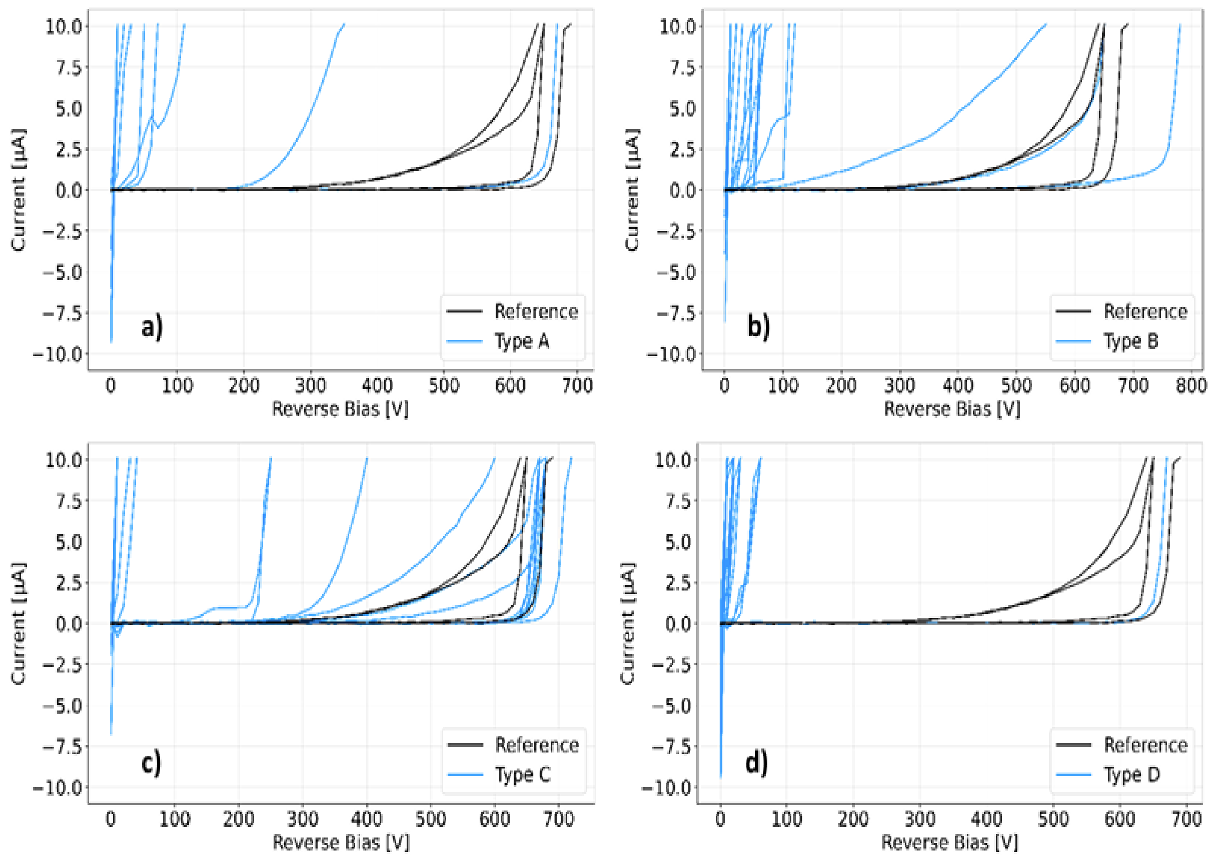

Fig. 3. I-V reverse bias characteristics for type A (a), type B (b), type C (c) and type D (d), each with reference measurements of devices without defects (black lines).

Based on these diagrams the breakdown voltage under reverse bias was determined and is seen in figure 4. The boxplot shows that the breakdown voltages for defect types A, B, and D cluster within a narrow range at low reverse-bias voltages. In contrast, type C spans a broader voltage range and has a higher median than the other defect types. Type D, despite having the largest sample size n, exhibits the tightest distribution and the lowest breakdown voltage.

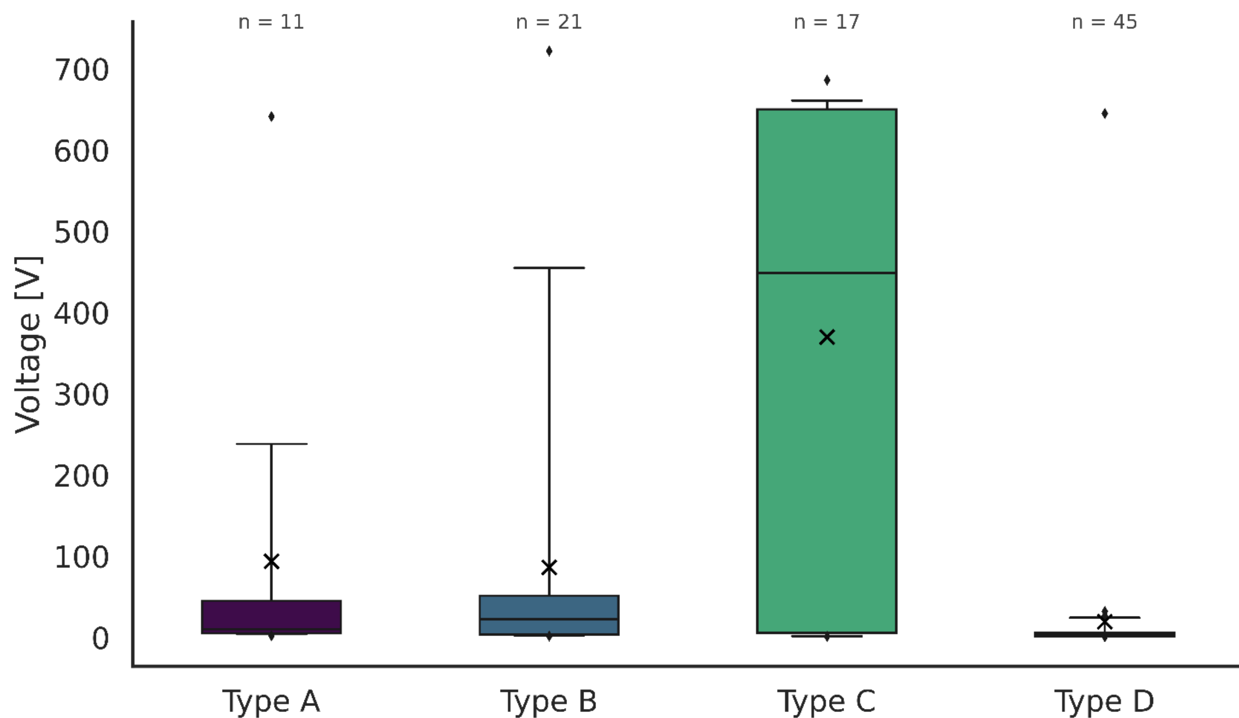

Fig. 4. The boxplot shows the distribution of breakdown voltage under reverse bias for the different defect types. The mean value is marked by a small cross, and n denotes the number of defects per type.

Outlook: PL Device Characterization

For more detailed investigation of the structure of SFs in devices, Trench-MOSFETs were reprocessed to the pre-metal and pre-oxide state to be examined with UVPL. Initial testing of one of the reprocessed devices with a SF and different illumination sources and filters can be seen in figure 5. The sample was uniformly illuminated with 305 nm and examined with three different detector filters. A 430 nm bandpass filter, a 550 nm short pass and a 650 nm long pass filter were applied to examine the SFs in different luminescence ranges. The SF is visible in all of the shown images, but the details and fine structure varies for each filter and illumination source combination. Additional to the signal from the stacking faults, we observed dark vertical lines, especially at the bottom of images b) and c). In panel a) and b) the SF appears as a dark triangle while a thick black line appears on the right side of the SF when illuminated with 305 nm and with the BP and the shortpass filter. Panel c) shows the SF as a bright triangular shaped form with the black line again on the right side of the triangle. The combination of illumination sources and different filters allows a more detailed investigation of the SF and energy states in the crystal surrounding the defect. The configuration in panel c) is similar to the SICA, so the SF is probably a type A or D defect as it appears as a dark triangle in the image. The different filters could possibly help to investigate the SF PL types further and understand the origin of the different effects the types have on the finished devices.
For as grown epitaxy layers different PL wavelengths can be used for subclassification of stacking fault types. [7,8] Since the implantation changes the contrast and brightness of the SF as can be seen in figure 1, the SF cannot be classified after this process step by evaluating the PL emission images in dependence on the excitation wavelength.
The black vertical lines that are visible especially in the images b) and c) all seem to originate in the edge termination of the device. A possible reason for this could be degradation by the electrical testing that was conducted before the reprocessing of the devices, through propagation of defects caused by electrical stress as reported by Hatta et al. [9] The appearance of these lines as well as SF behavior in stressed devices need further investigation.

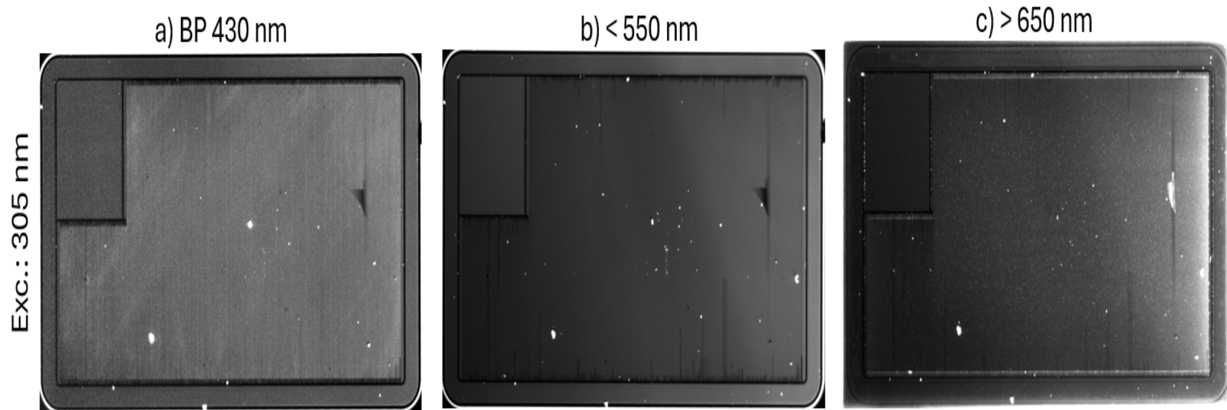

Fig. 5. UVPL Images of a reprocessed MOSFET device with stacking faults. With 305 nm excitation source, a 430 nm bandpass, a 550 nm shortpass and a 650 nm longpass filter were applied to show the luminescence signal in different wavelength ranges.

Summary

This study indicates that SFs change the appearance of the PL signal during device processing, particularly related to implantation steps. From the PL signal after implant and anneal different subtypes can be classified with indications that the subtype may correlate with implant parameters. This will be examined in further studies and will be cross referenced with PL spectroscopy to confirm the SF types and classification and if necessary, lead to process optimization. Importantly, the subtypes exhibit different impacts on device performance: while Types A, B, and D significantly degrade the reverse blocking capability of diodes, Type C shows no measurable effect on breakdown voltage. PL imaging can also be used for characterization of finished devices after electrical testing and to investigate the SF in more detail by the application of a range of filters. In addition, with spectral PL, this method will be used in further investigation of the origin of the subtypes and SF induced degradation.

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