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Challenges in 1SSF Detection in 4H-SiC Epilayer and Related Failure

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Abstract. Basal plane dislocations (BPDs) represent one of the most detrimental defects in 4H-SiC epitaxial wafers, causing forward voltage degradation in bipolar and power FET devices through the formation and expansion of Shockley-type stacking faults (SSFs). This expansion is driven by the recombination-enhanced dislocation glide (REDG) mechanism during forward bias operation. Despite efforts to mitigate BPD effects by converting them into threading edge dislocations (TEDs) via buffer layer engineering, throughout the epitaxial growth SSFs can still nucleate and propagate, particularly under high current injection. This work presents a comprehensive analysis combining electrical characterization, fault localization technique, Scanning Electron Microscopy (SEM) and micro-photoluminescence (μ-PL) to investigate SSF formation, crystallographic features, and their impact on device performance. The results underscore the critical role of advanced diagnostics and epitaxial process optimization in controlling SSF-related degradation and improving the reliability of SiC power devices.

Introduction

All BPDs are considered one of the most harmful defects in SiC epitaxial wafers. They cause forward degradation, which manifests as an increased forward voltage drop, in SiC bipolar devices and body diodes junction within power MOSFET when they occur in the active region. During forward bias in a SiC pn junction, BPDs can lead to SSFs due to the injection of minority carriers. This expansion of stacking faults is driven by the electron-hole REDG process [1-2]. This phenomenon was initially observed as causing degradation in the forward characteristics of high-voltage SiC pin diodes, with its primary source identified as stacking faults expanding within the voltage-blocking region. SSF expansion from BPDs occurs during forward bias operation in 4H-SiC, leading to forward voltage drift in minority carrier SiC devices [3]. Additionally, SSF expansion has been linked to reverse bias breakdown voltage degradation [4]. To reduce the impact of these SSFs in the active drift layer, a highly doped buffer layer was developed to convert most BPDs into threading edge dislocations (TEDs) [5]. It is seldom observed that nominal current density degradation is generally not impacted. However, at exceptionally high current levels, the increased density of minority charge carriers can penetrate deeper into the buffer region, potentially triggering stacking fault growth at deeply embedded crystal defects within the buffer or even the n^+ substrate. In the case of unipolar devices during each turn-off event of a SiC MOSFET, the body diode is subjected to forward bias, which may induce the propagation of stacking faults within the n-type drift layer. The expanded stacking fault introduces a potential barrier that contributes to an increase in the on-resistance of the device. An increase in the drain leakage current after the current stress is expected [6].

Experimental

In this experiment, 4H-SiC planar MOSFETs, fabricated on an epitaxial layer of almost 13 μm thickness with a doping concentration of about 1×10^{16} cm^{-3}, were used.
Sample prepation from backside was performed with MultiPrep™ Precision Polishing System (Allied High Tech Products) aimed to remove package frame and to reach SiC substrate. PHEMOS1000 Emission microscopy (Em.Mi.) was used to identify the coordinates of point of failure induced by electrical stress. Focused ion dual beam (FIB) -Helios 5UC – was employed to mark the position and identify the region to investigate. LabRam Odyssey Raman spectrometer equipped with a λ=320 nm (74x objective) wavelength and 600 gr/mm grating was adopted to perform the 1SSF PL map.

Results and Discussion

Sample analyzed in this work didn't exhibit any indicators of impending failure, offering no warning of electrical issues at the Electrical Wafer Sorting test (EWS). After assembly process, sample was subjected to Early Life Failure Rate (ELFR) test flow, not exhibiting any anomalous current trend. Following ELFR, some electrical parameters have been additionally tested in order to confirm the goodness of the piece. As shown in Fig. 1, electrical test for this device revealed a slight increase in drain leakage current at high bias (850 nA at 1200V) (Fig.1a) if compared to other parts subjected to the same test cycle in which IDSS value is lower than 200 nA (Fig 1b).

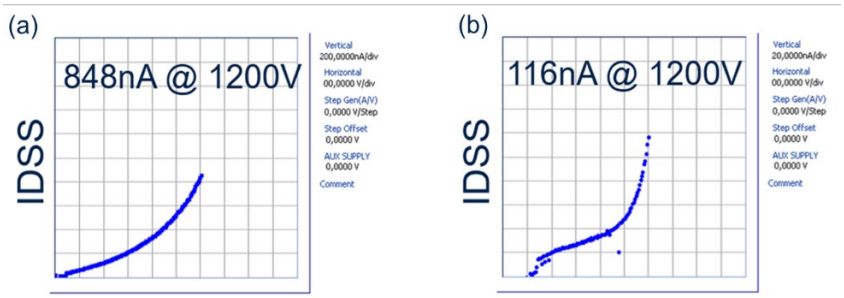

Fig. 1. Drain leakage current (IDSS) trends for sample analyzed in this work (left) and a device subjected to same trials (EWS + ELFR + Final test) (right). NOTE: vertical scale in the two graphs is different, current values at 1200V are reported for easy of reference.

After the above described preparation, the device was subjected to fault localization analysis, Sample was appropiately powered in IDSS configuration to identify the region in which current leakage is concentrated, Emitted photons where clearly detected and shown in Fig. 2 as pink spots. These emissions are in correspondence to a defect, well visible as dark line with IR camera.

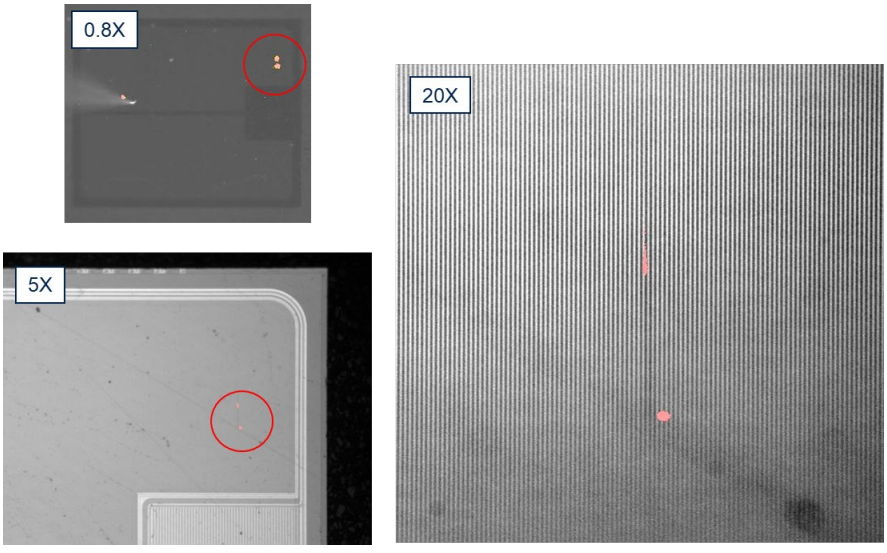

Fig. 2. Fault Localization by photon emission from backside.

To better investigate the defect region was identified from backside to. Decapping of the package and total delayering steps allowed the observation of the failure region at the epitaxial level under the SEM. As shown in Fig. 3, some depressions on epitaxy surface are well visible in correspondence of hot spot region, crossed by the dark line visible in Fig. 2.

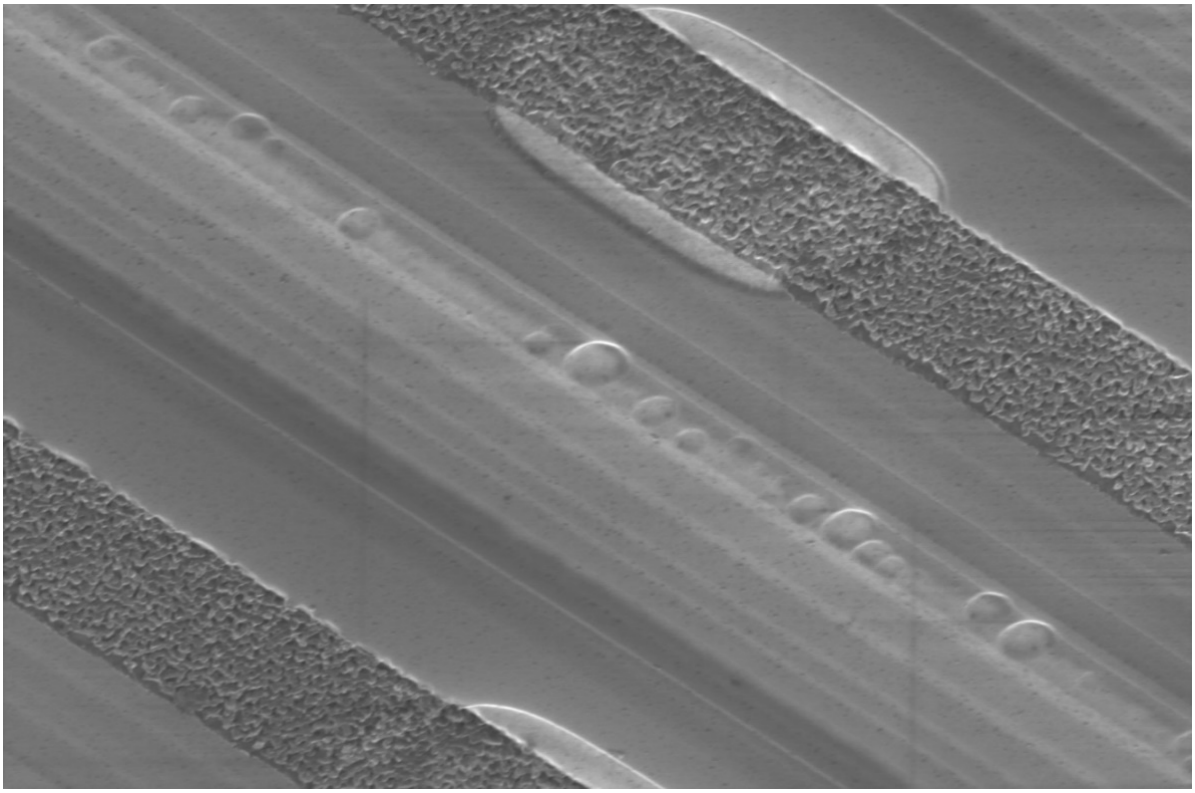

Fig. 3. SEM image perfomed with FIB Helios 5UC showing depression on epitaxial layer and responsible to IDSS leakage.

Following the Emission Microscopy investigation and spatial localization of the failure with SEM, μ-PL analysis was performed to examine stacking faults extended within the 4H-SiC epilayers.

Fig. 4a presents the map obtained by centering the acquisition on the spectral region corresponding to stacking fault emission, revealing a characteristic triangular morphology. The spectral data reported in Fig. 4b highlights two distinct regions: region 1 corresponding to the μ-PL acquisition within the stacking fault area, showing SF layer emission at λ=424 nm, thereby identifying it as a single stacking fault (1SSF) and region 2, exhibiting only band-to-band emission with a peak at λ=389 nm [7].

Considering the 4° off-axis angle and the 1SSF length of approximately 150 μm, it can be inferred that the stacking fault originates from a BPD located just above the BPD-to-TED conversion zone, likely formed during the initial stages of epitaxial growth and subsequently propagated during electrical testing. Indeed, Lendenmann et al. reported a voltage drop occurring during forward operation [8], attributing it to BPDs acting as sources of SSFs. Specifically, a BPD dissociates into two partial dislocations with SSF forming between them. The expansion of the SSF is driven by the glide of these partial dislocations through the REDG mechanism. When a sufficiently large amount of excess carriers are injected, the Si-core partial dislocation starts to glide, which leads to 1SSF expansion. Both bipolar and unipolar SiC devices exhibit forward degradation when a BPD propagates along the active direction. Various types of stacking faults have been identified using UV-based PL mapping, revealing over 15 distinct SSF shapes in the active regions of degraded SiC devices following electrical stress testing. These SSF shapes have been categorized into multiple forms, including rectangular, triangular, and rhombic geometries [9-10-11-12-13-14]. The expansion of SSFs primarily takes place in the n-type region and is confined between the p^+–n^- and n^-–n^+ junctions. Notably, Si-core partial dislocations are mobile, whereas C-core partial dislocations remain immobile. Stahlbush et al [15] suggested that the observed expansion patterns are closely linked to

the Burgers vector and direction of the BPDs. Ijima [16] elucidates the relationship between the morphologies of expanded SSFs and the configurations of BPD segments in 4H–SiC epilayers. It was demonstrated that, considering three types of Burgers vectors, 2 varieties of PD loops, and 12 line directions, there exist 72 distinct crystallographic BPD structures. The specific shapes of the expanded SSFs were predicted by analyzing the glide behavior of the PDs. Through g·b analysis, the predicted SSF shapes were confirmed to correspond well with experimental results and a total of 38 different expanded SSF shapes were identified. This established correlation enables the determination of the Burgers vectors and line directions of the original BPD segments based on the observed shapes of the expanded SSFs.

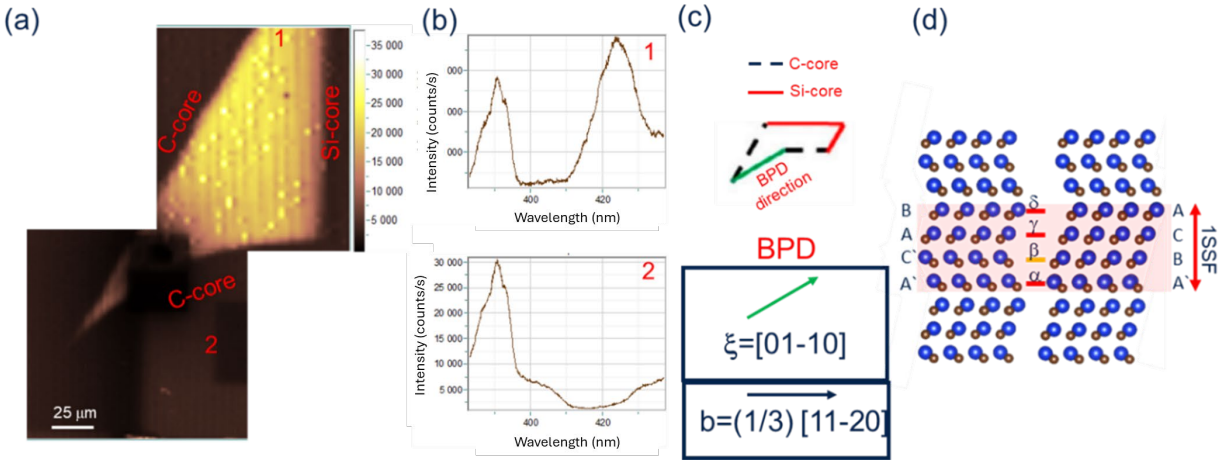

Fig. 4. a) 1SSF imaging through m-PL intensity map centred at λ=424 nm; b) PL spectra within (1) and outside (2) the 1SSF; c) BPD evolution modeling, with initial direction and burger vector at at the beginning of the expansion of 1SSF d) Vesta 1SSF lattice simulation reporting the lattice stacking in correspondence of the fault.

The characteristic morphology of the SSFs provides insight into the nature of the dislocations that bound them. From the µ-PL analysis, it can be inferred that the dislocation direction is [10-10] with a Burgers vector of (1/3)[11-20] [16] as schematized in Fig. 4c where SSF starting shape is reported. A BPD can possess any of six possible Burgers vectors; however, due to the symmetry of the crystal, only three Burgers vectors (1/3)[11-20], (1/3)[1-210], and (1/3)[-2110] need to be considered when analyzing 1SSF expansion. The dislocation line itself typically aligns with one of the six ⟨11-20⟩ crystallographic directions. In this study after repeated laser irradiations, the SSF does not exhibit any further lateral enlargement. This behavior strongly suggests that the SSF is confined by C-core dislocations both above and below, effectively limiting its expansion. Furthermore, the intensity variations observed from left to right correspond to the defect's emergence toward the surface along the crystallographic direction [11-20]. This directional extension is governed by the presence of Si-core dislocations at the leading edge, which defines the expansion front of the stacking fault according to the PD loop model[17]. Using Zhdanov's notation, the stacking sequence of the SSF is expressed as (1,3), and that of perfect SiC is (2,2). In the reported stacking representation of the bond configuration near the edge of a SSF in SiC (Fig. 4d), the left and right sides correspond to the perfect SiC crystal structure and the SSF region, respectively. Four slip planes, designated as α, β, γ, and δ, are identified. SSFs may form along these dislocation slip planes. For the specific 1SSF defect shape considered, according to the basal plane dislocation loop model [16], the C-core partial dislocations oriented along the [-1-120] and [11-20] crystallographic directions, are consistently located on the right side of the SSF, as reported in [18]. Consequently, the dislocation loop forms when the slip occurs on either the α or β slip planes. The Fig. 4d exemplifies the structural evolution from the perfect crystal stacking sequence, transitioning from an A′C′AB stacking to an A′BCA configuration through slip along the β plane.

Conclusion

This study highlights the critical role of BPDs and the associated formation of 1SSF in 4H-SiC epitaxial wafers, which can influence device performance through forward degradation mechanisms. Advanced diagnostic techniques, particularly μ-PL mapping, provide detailed spatial and spectral insights into the morphology and crystallographic nature of 1SSF within the epitaxial layers. The μ-PL analysis effectively identifies and characterizes stacking fault expansions originating from BPDs, enabling precise localization and understanding of defect propagation. These insights are essential to guide epitaxial growth optimization and process control strategies, including thermal and oxidation treatments, to mitigate SSF-related degradation and enhance the reliability of SiC power devices. The integration of electrical testing with μ-PL and complementary microscopy techniques forms a comprehensive approach for monitoring stacking fault dynamics and improving wafer screening procedures.

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