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Depth-Dependent Suppression of Bipolar Degradation in 4H-SiC Diodes via Proton Implantation and Evaluation of Safe Operating Current Density Range

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Abstract. This work explores the role of implantation depth in suppressing bipolar degradation of 4H-SiC PiN diodes through proton implantation. Targeting depths aligned with active basal plane dislocations (BPDs) effectively reduces stacking-fault expansion, as confirmed by electroluminescence imaging [1,2]. From these observations, we quantified the effective range of suppression in both depth and safe operating current density. Room-temperature proton implantation (170keV, 1×10^{16} cm^{-2}) into the buffer reduced forward-voltage drift ΔV_F by 97% at 600A/cm^2. The implanted diode extended the safe operating current range to 1300A/cm^2, ~200A/cm^2 higher than the reference, confirming effective suppression of bipolar degradation. Once the suppression barrier, defined as a critical excess hole density threshold, was exceeded, the proton-implanted diode exhibited explosive basal plane dislocation activity, leading to the formation of multiple bar-shaped stacking faults. These active BPDs are located deeper than the proton-implant tail, at a depth of around 11.4μm; however, the threshold hole density required for their activation remains approximately the same (~ 4×10^{16} cm^{-3}) [3].

Introduction

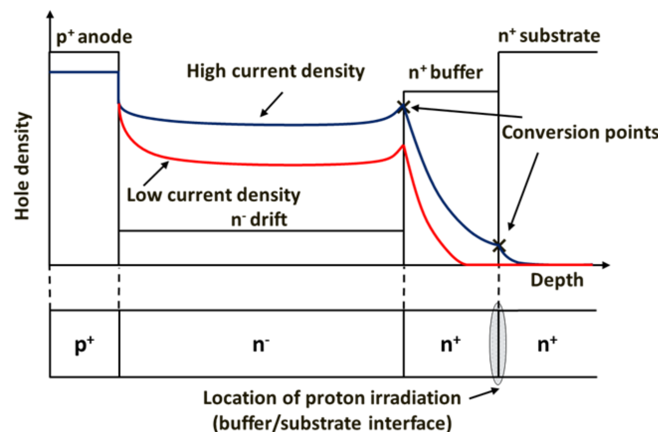

Fig. 1. Hole density distribution of the 4H-SiC PiN diode

One critical issue in the long-term reliability of 4H-SiC power MOSFETs is its body diode's V_F (forward voltage drop) increase from the unique phenomenon of bipolar degradation. This is caused by the expansion of stacking faults (SFs) which originate from basal plane dislocations (BPDs) in the sublimation grown SiC substrate. Inserting a n$^+$ buffer layer with a short carrier lifetime is currently

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the standard method in preventing electron-hole recombination from triggering SFs growth [4]. However, at higher current densities, the hole concentration can be substantial and reach the buffer/substrate interface where BPD-TED (threading edge dislocation) conversion points are present.

Fabrication

An epitaxial layer, with a nitrogen doping concentration of 9×10^{15} cm^{-3} and a thickness of 10μm, was grown by the CVD method with a high growth rate of 30μm/hr. BPD density was further decreased by fast epitaxy and by adding a buffer layer with a thickness of 1μm and a doping concentration of 2×10^{18} cm^{-3}. Proton irradiation (1×10^{16} cm^{-2} at 170 keV, room temperature) was applied to the buffer layer prior to epitaxial growth to suppress stacking fault expansion with a non-implanted diode fabricated in parallel as a reference. To achieve high current density stress in the fabricated comb-shaped PiN diodes, surface doping at the anode was enhanced using a 30 nm Al capping layer. This approach shifted the first Al implantation peak closer to the surface, increasing the peak concentration near the metal–semiconductor interface to facilitate thin depletion tunneling (Fig.2 (a)). As a result, a heavily doped p-type anode region with a peak concentration of 4×10^{20} cm^{-3} was formed through high-temperature Al implantation at 400 °C, followed by activation annealing at 1700 °C for 30 minutes. A low-temperature Ti-Pd based metallization stack (Ti/Pd/Ti/Pt =2 nm/25 nm/40 nm/150 nm), annealed at 700 °C for 1 min in Ar ambient, was employed for comb-shaped electrodes, achieving both precise pattern integrity and ultra-low specific contact resistance ($\rho_C = 7.06\times10^{-5}$ $\Omega\cdot cm^2$) required for EL emission analysis (Fig. 2(b)).

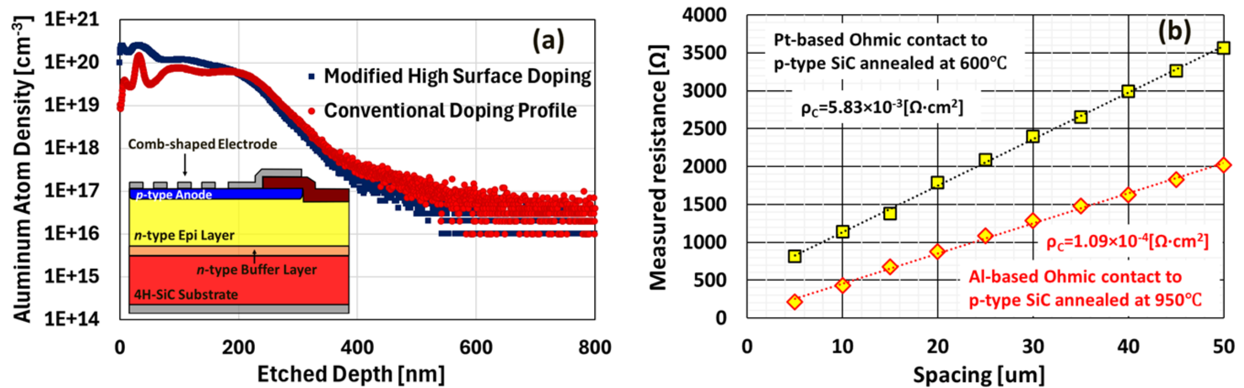

Fig. 2. (a) Anode region SIMS profile and (b) Al vs Ti-Pd TLM contact evaluation comparison

Simulation and Numerical Analysis

To accurately determine the threshold hole density at which bipolar degradation initiates in both reference and proton-implanted 4H-SiC PiN diodes, TCAD simulations were first calibrated against the *I–V* and *C–V* characteristics of simultaneously fabricated Ti-Pd-based circular diodes and subsequently extended to the comb-shaped electrode structure. During model validation, a slight deviation in the simulated I–V characteristics was observed, attributed to current-carrying limitations within the narrow electrode fingers of the comb-shaped layout rather than to contact resistance. EL analysis was then employed to identify the current density at which the initial onset of stacking fault (SF) expansion occurs, and to measure the maximum width W of a bar-shaped SSF. The high pulsed current required for this evaluation is limited primarily by the probe tip diameter rather than the anode contact resistance. To overcome this limitation, two probe tips were used on separate individual pads, each covering separate halves of the diode's conduction area.

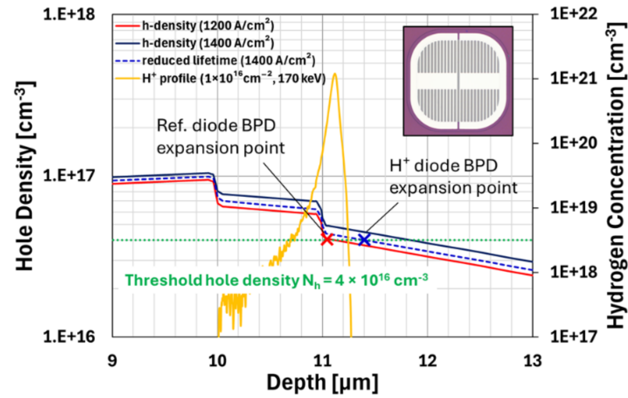

Fig. 3. TCAD simulation of hole density and H^+ profile at 1200-1400 A/cm^2, showing delayed BPD activation beyond the implant tail edge

Fig. 3 shows the simulated hole density profiles superimposed against the hydrogen implant distribution under current stress levels of 1200 A/cm² and 1400 A/cm². In the reference diode (no proton implantation), basal plane dislocation (BPD) expansion begins when the hole density exceeds the threshold of approximately 4×10^{16} cm^{-3} near the buffer/substrate interface. In contrast, the H^+-implanted diode exhibits a delayed activation, with the BPD expansion point shifting deeper into the epilayer, just beyond the implantation tail edge (~11.4 μm). This delay arises because the proton-induced damage region locally reduces carrier lifetime (from 181 ns to 23.5 ns) [5,6], creating a lower-injection zone that temporarily suppresses the minority-carrier density below the critical threshold.

Depth-Resolved Electroluminescence Analysis and Experimental Correlation with Implantation Profile

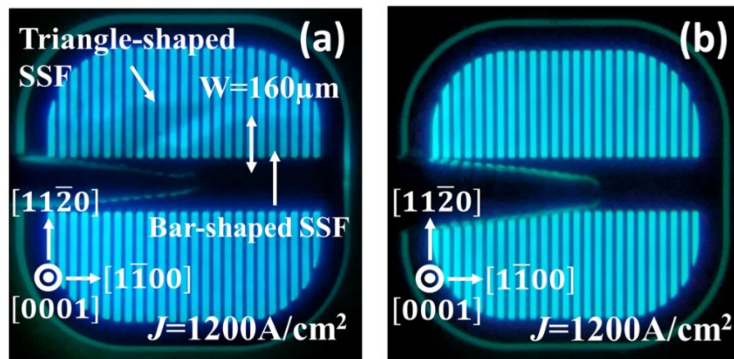

Fig. 4. EL images of (a) reference diode and (b) H^+- implanted diode stressed at an equivalent current density of J=1200A/cm^2

After the comb-shaped PiN diode had been fabricated, a bias stress of 400-μs-long 8.5V voltage pulse, equivalent to stress-current density of J=1200 A/cm^2, was injected at a frequency of 3.33 pulses/s for 20 min to observe the stacking fault expansion. Once the initially expanded dark region was observed, the bias stress was switched to DC to capture the time-evolution EL images at a current density of J=200 A/cm^2 for an additional 20 min. For the reference diode (Fig. 4 (a)), both triangle-shaped and bar-shaped SSFs (Shockley-type stacking faults) were seen expanding along the $[1\,\bar{1}\,0\,0]$ direction. To estimate the depth of the most active basal-plane dislocations (BPDs), the measured maximum width of a single stacking fault (W) was used in the geometric relation: $d = W \cdot \tan\theta$, where d is depth of the expansion point and θ is the actual off-cut angle. From the EL image in Fig. 4(a), a maximum stacking-fault width of approximately 160 μm was observed. This corresponds to a depth of about 11.15 μm, calculated using the wafer off-cut angle of 4°. The proton-implantation energy of 170 keV was therefore chosen so that the hydrogen peak would appear at this depth, matching the

location of the most active basal-plane dislocations near the buffer/substrate interface. As shown in the fabrication sequence below, the proton implantation step was introduced after the buffer layer growth and before the epitaxial growth, enabling a sufficiently high implantation dose and penetration depth to reach the targeted BPD-active region. The effectiveness of this approach is evident in Fig. 4(b), where the implanted diodes show no stacking-fault expansion even under the same current density conditions.

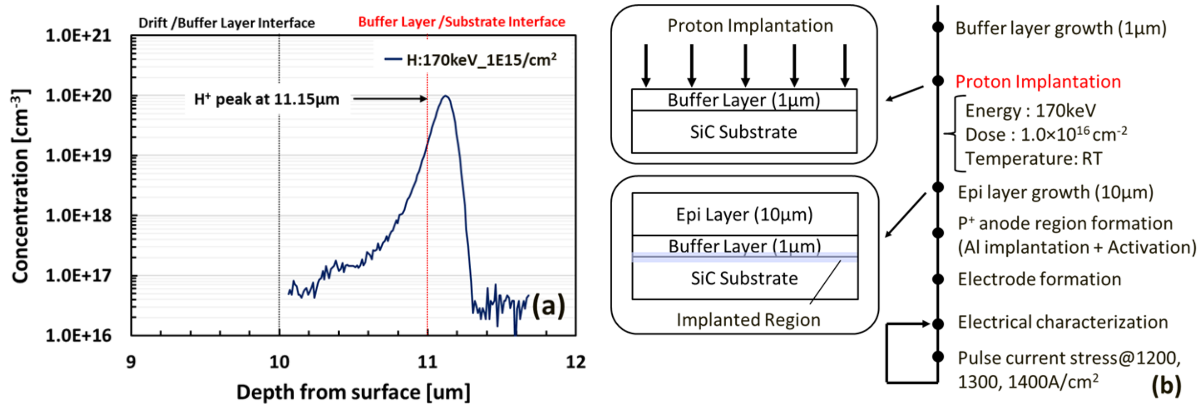

Fig. 5. (a) SIMS hydrogen (H^+) depth profile for 170 keV, 1×10^{15} cm^{-2} implantation showing a peak concentration at 11.15 μm within the buffer/substrate interface region. (b) Proton implantation step integrated into the 4H-SiC PiN diode fabrication sequence, illustrating the buffer layer position and subsequent process flow

Finally, although the proton-implanted diodes initially showed no stacking-fault expansion under equivalent current densities, expansion was eventually observed at higher stress levels and longer operation times. This behavior defines the limit of the effective bipolar-degradation suppression range and highlights the need to further investigate the safe operating window of proton-implanted SiC diodes, where the devices do not exhibit bipolar degradation due to dislocation pinning [7,8] and carrier-lifetime reduction, thereby ensuring long-term reliability.

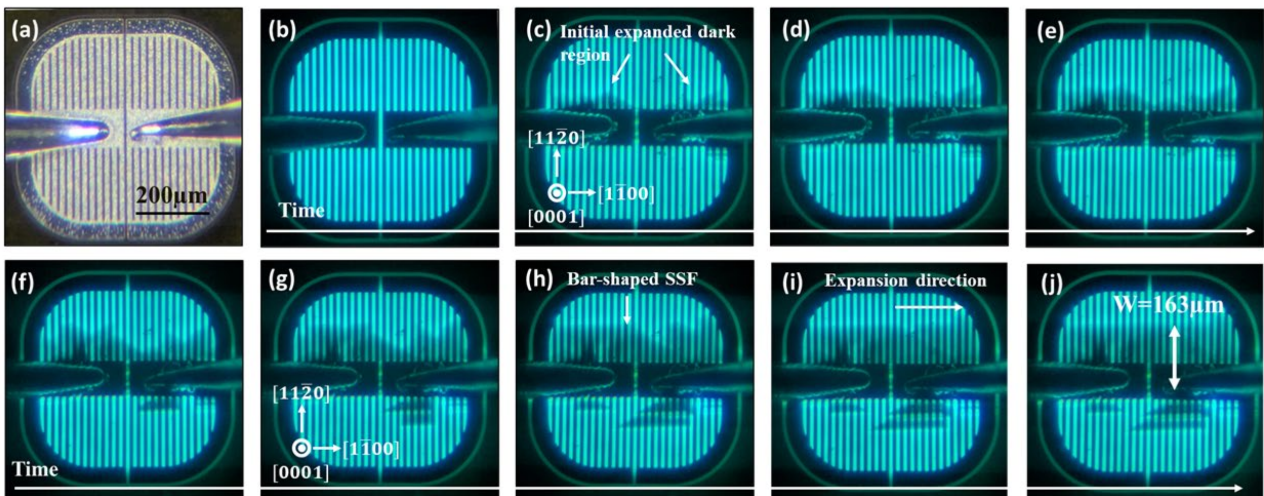

Fig. 6. Time evolution of electroluminescence microscopy images under bias stress in the proton-implanted 4H-SiC PiN diode. Abrupt bar-shaped stacking faults (SFs) emerge at higher stress levels (J=1400 A/cm^2), indicating the upper limit of the bipolar-degradation suppression window

To correlate the simulated carrier-density threshold with the experimental onset of stacking-fault expansion, electroluminescence (EL) imaging was performed under incremental current stress.
The observed width of 163μm in the fully expanded bar-shaped SSF in Fig. 6, image (j) suggests that SF expansion initiates just below the proton implantation tail depth of 11.4μm. This unpinning is triggered when minority carrier injection becomes sufficient to overcome the reduced-lifetime region

introduced by the implantation damage. This release occurs abruptly above ~1400A/cm^2 with bar-shaped SFs appearing more frequently than the reference diode, indicating an explosive activation of BPDs once the proton-induced barrier, defined by an excess hole density threshold, is overcome.

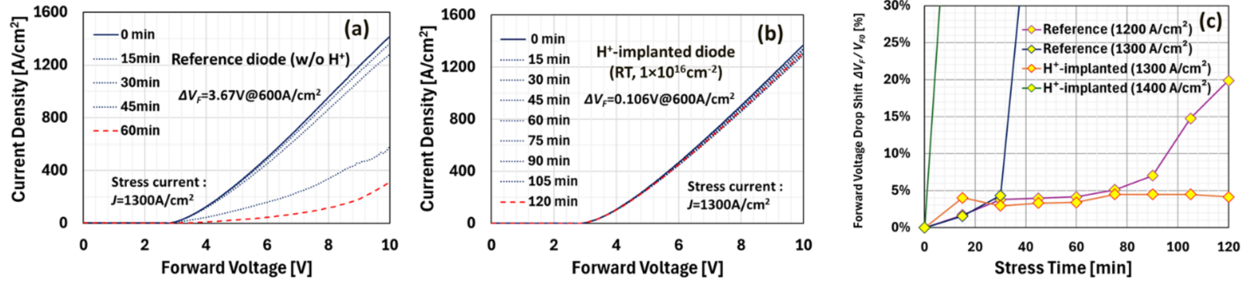

Fig. 7. (a) *I–V* characteristics of reference and (b) H^+-implanted diodes. Reference diode shows ΔV_F drift under stress (J=1300 A/cm^2), while H^+-implanted diode remains stable (c) Summary of V_F shift in reference and H^+-implanted PiN diodes under various current stress

As shown in Fig. 7, room-temperature proton implantation (1×10^{16} cm^{-2}) into the buffer reduced forward-voltage drift ΔV_F by 97% at 600A/cm^2. Proton-implanted diode demonstrated an extended safe operating current range, withstanding up to 1300 A/cm², an increase of 200 A/cm² compared to the non-implanted reference diode.
These observations, together with the TCAD-extracted threshold hole density of 4×10^{16} cm^{-3}, support a consistent mechanism: proton-induced lifetime reduction within the buffer region pins BPDs and keeps the local minority-carrier density below the threshold near the buffer/substrate interface, thereby delaying SF activation until regions deeper than the proton-implant tail (~11.4 µm) under elevated stress. As a result, the implanted diodes exhibit stable forward characteristics and no EL-visible SF expansion up to ~1300A/cm^2; beyond this level, the abrupt emergence of bar-shaped SFs indicates barrier overrun and defines the upper limit of the safe operating window.

Summary

Proton implantation suppresses BPD-driven bipolar degradation in 4H-SiC diodes by reducing carrier lifetime and pinning dislocations within the implanted profile region, thereby shifting SF activation deeper beyond the implant tail. TCAD fitted with literature-calibrated lifetimes (τ = 181 ns for the reference, τ = 23.5 ns for 1×10^{16} cm^{-2} at 170 keV implantation) indicates that, although the implanted diode exceeds the SF threshold at the buffer/substrate interface, proton-induced pinning prevents expansion, delaying activation until deeper beyond the implant tail. Implanted diodes remained stable up to 1300A/cm^2 (~ 200A/cm^2 higher than reference), with no ΔV_F drift and no bar-shaped SFs observed in EL imaging. These results confirm that lifetime engineering via proton implantation selectively into the buffer layer is an effective approach to extend the safe-operating current density of 4H-SiC PiN diodes without significantly reducing minority-carrier injection or conduction efficiency.

Acknowledgements

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