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Evaluation of Oxide Processing Steps in SiC Technology Using Contactless Corona-Based CV Measurements

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Abstract. An area of increasing interest for SiC device processing is the processing and qualification of silicon oxides. In this article a contactless corona CV (CnCV) measurement procedure is evaluated as a way to gain more knowledge about the different processes related to oxides. A 21-point measurement pattern is used to gain information about uniformity of oxide properties. Two different types of oxides have been considered, low pressure chemical vapor deposited (CVD) oxides using tetraethylorthosilicate (TEOS) and thermally grown oxides. The two different groups have received different combinations of pre- and post-processing steps prior to measurements. As expected, low pressure CVD (LPCVD) and thermally grown SiO_2 without any post oxidation annealing (POA) showed significantly different electrical characteristics compared to the wafers that did get a POA. This difference could clearly be distinguished by CnCV, meaning that individual process steps can be analyzed without the fabrication of any test structures on the wafers. As the individual process steps can be analyzed, the uniformity of the individual steps can be accessed. Using a 21-point pattern it was possible to show that there is a non-uniformity in the LPCVD process used prior to the POA. This makes the CnCV technique suitable for in-line characterization and process monitoring.

Introduction

As silicon carbide technology continues to mature, higher demands are put on each of the processing steps. One area where increased monitoring is desired is that of different oxide layer formation steps that take place during device fabrication. This is due to the wide variety of different oxides that are used. This could be chemical vapor deposition (CVD) oxide to be used as hard mask [1], a thermal oxide to be used as a gate oxide for SiC MOS devices [2], or an atomic layer deposited (ALD) oxide for special applications [3]. What further complicates oxide qualification is that additional processing might affect the properties of the final oxide. The gate oxide quality of a MOS transistor is, e.g., also dependent on the surface quality of the substrate, implying that gate oxide optimization also depends upon the activation anneal after the ion implantation. So, if certain oxide properties are desired, a good understanding of the processing steps and their effect on the oxide is required. Hence, inline control measurements for oxide properties are needed which are quick and do not require any test structure. This study aims to investigate the influence of different processing steps on oxide characteristics using a contactless corona-based capacitance voltage (CnCV) technique to characterize the oxides [4]. The CnCV technique uses a corona spot charging device and a Kelvin probe to perform a CV measurement of the oxidized wafers. From these measurements it is possible to extract the equivalent oxide thickness (EOT), total dielectric charge (Q_{tot}), flatband voltage (V_{FB}), and the distribution of interface trap densities (D_{it}) which can be calculated up to about 0.8 eV from the band edge. The CnCV technique can be used on bare oxides and does not require any test structures. This makes CnCV a strong candidate for inline process monitoring as the contactless nature enables fast measurements without the need of manufactured test structures and the wafers can be returned into the processing line afterwards. The CnCV technique is explained in detail in reference [4].

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Experimental

Six 150 mm 4H-SiC homoepitaxial wafers with epitaxial layer thickness between 10.8-12.3 µm have been considered in this work. The epitaxial layers are doped using nitrogen to a net doping concentration of $8.4\text{-}8.9 \cdot 10^{15}$ cm^{-3}. The wafers received one of two types of oxides, either a silicon oxide realized by a low-pressure chemical vapor deposition (LPCVD) process using TEOS followed by a densification step in inert atmosphere at 900 °C or a thermally grown dry oxide. The LPCVD TEOS deposition took place at a temperature of about 700 °C and the thermal dry oxides were grown at about 1300 °C. The wafers received different combinations of pre- and post-oxide treatments. The pretreatment was a time coupled HF dip where the wafer is dipped in HF immediately prior to loading into the LPCVD reactor or furnace. The post process was a post oxidation anneal (POA) at 1300 °C in a nitrogen monoxide (NO) atmosphere. All processes generated oxides with a thickness between 50-60 nm. The wafer processing is summarized in Table 1.

Table 1. Summary of the wafer processing used in this work. The first column is the wafer "Wafer" identification number. The second column "Time coupled HF dip" indicates whether the wafer got the time coupled HF dip pre-oxide treatment or not. The third column "Oxide" indicates what type of oxide the wafer received. The fourth column "Post oxidation anneal" indicates whether the wafer received the post oxidation anneal in NO atmosphere or not.

Wafer	Time coupled HF dip	Oxide	Post oxidation anneal
1	Yes	LPCVD TEOS	No
2	Yes	LPCVD TEOS	Yes
3	No	LPCVD TEOS	Yes
4	Yes	Thermal dry oxide	No
5	Yes	Thermal dry oxide	Yes
6	No	Thermal dry oxide	Yes

Reproducibility of Measurements

The wafer used in this study on reproducibility is a wafer that got the same oxide processing steps as wafer 4 in Table 1. The initial voltage (V_{init}) measurement by the Kelvin probe depends on the potential of the surface. V_{init} is obtained without applying any charge to the wafer. Thus, it is possible to map V_{init} without affecting later measurements that involve charging the wafer. V_{init} can change drastically depending on what the wafer has been exposed to prior to the measurement, such as charge left on the surface from a previous CnCV measurement or surface absorbed contaminants from water or isopropyl alcohol. The lack of control of the surface absorbed contaminants makes it difficult to reproduce a surface condition. This causes variations in the measured V_{init}. In the following section a demonstration of the reproducibility is shown without perfect restoration of the wafer surface between measurements. To fairly assess the reproducibility of the measurements, the wafer was partially dipped in deionized water and then dried on a hotplate at 95°C for 10 minutes before each consecutive measurement. In Figure 1 an example is shown; the lower part of the wafer has been dipped in deionized water and the measurement point is marked. A ten-time repeat of the measurement is presented in Table 2. From Table 2 V_{init} was measured between 0.13-0.29 V. This uncertainty adds to the uncertainty of Q_{tot} as Q_{tot} is the amount of charge required to reach V_{FB} from V_{init}. To compare Q_{tot} between the different measurements the Q_{tot} values have been corrected to the V_{init} of the first

measurement. These are the Q_{tot} values that we will consider in this paper. Q_{it} differs from the more widely used D_{it} in that D_{it} is evaluated at a specific position in the bandgap, in this case at an energy level of 0.3 eV below the Fermi level (E_F) (see Figure 2). Q_{it} is obtained by integrating the D_{it} spectrum between 0.05-0.3 eV and for the evaluation of the reproducibility of the measurements Q_{it} has been considered instead of the more widely used D_{it}. In Figure 2 the D_{it} spectra for each consecutive measurement overlap almost perfectly. Notice that the D_{it} spectra in Figure 2 has been translated to represent the energy below the conduction band, the D_{it} at E_F-0.3eV values in Table 2 can be found at about 0.49eV (0.3eV+E_F) below the conduction band in Figure 2. In Table 2 the sigma/mean values for the different properties can be seen. For V_{FB} sigma/mean value is 1.56%, for Q_{it} 2.18 %, and for EOT it gives 0.15%. Later in this paper it will be shown that these sigma/mean results are sufficient to resolve most of the processes considered.

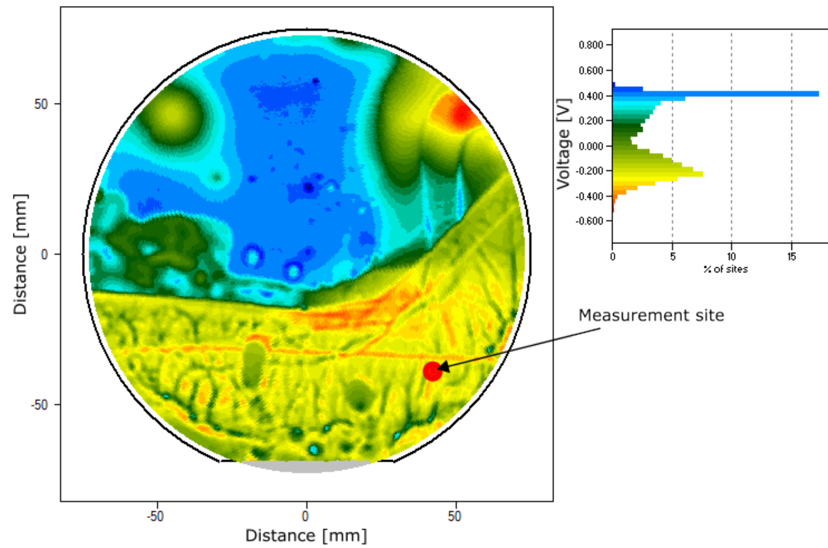

Fig. 1. A map showing the distribution of V_{init} of the wafer used in the reproducibility test.

Table 2. Summary of the ten consecutive measurements done to test the reproducibility.

Measurements:	V_{init} [V]	V_{fb} [V]	D_{it} at E_F-0.3eV [10^{11}cm^{-2}eV^{-1}]	Q_{it} [10^{11} q/cm²]	Q_{tot} [10^{11}q/cm²]	Q_{tot} corr. to same V_{init} [10^{11}q/cm²]	EOT [Å]	N_d [10^{15} cm^{-3}]
1	0.18	2.13	3.01	1.99	-6.18	-6.18	540	9.93
2	0.24	2.16	3.42	2.08	-6.23	-6.26	537	10.1
3	0.21	2.14	3.13	1.99	-6.22	-6.21	540	10.1
4	0.17	2.15	3.12	2.01	-6.29	-6.23	540	9.88
5	0.25	2.11	3.24	2.02	-6.04	-6.18	539	10.0
6	0.16	2.19	3.39	2.14	-6.47	-6.28	539	10.0
7	0.22	2.10	3.27	2.07	-5.99	-6.17	540	9.87
8	0.29	2.22	3.33	2.05	-6.09	-6.22	539	9.83
9	0.14	2.15	3.18	2.01	-6.31	-6.19	539	9.96
10	0.13	2.18	3.00	2.00	-6.56	-6.32	539	9.92
Average:	0.20	2.15	3.21	2.04	-6.24	-6.22	539	9.96
Standard deviation:	0.05	0.03	0.141	0.0444	0.172	0.0470	0.79	0.0785
1σ/Mean:	24.61%	1.56%	4.40%	2.18%	2.76%	0.76%	0.15%	0.79%

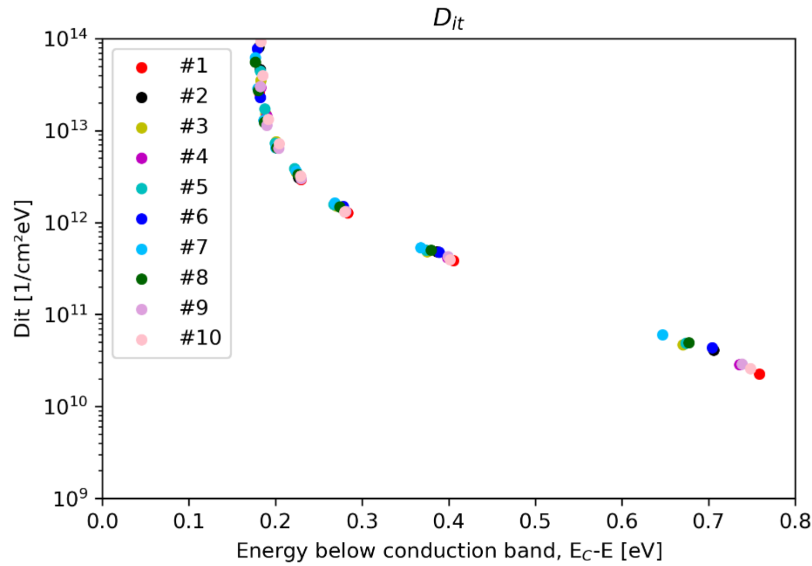

Fig. 2. D_{it} spectra for all of the consecutive measurements numbered #1-#10. The measurements have been made at the site marked in Figure 1.

Measurements

The measurements of the six wafers have been performed in a 21-point pattern as shown in Figure 3. This allows for analysis of the uniformity of oxide properties across the wafers. In Figure 4 the V_{FB} values for each wafer have been plotted for each measurement point. One of the LPCVD TEOS and one of the thermal oxide wafers exhibit significantly higher V_{FB} values than the other four wafers. These are the two wafers that did not get the POA, i.e., wafers 1 and 4. Among the other four wafers it can be seen in the insert that the LPCVD TEOS group together, wafer 2 and 3, and the thermal oxide wafers group together, wafers 5 and 6. But no significant systematic difference is detected between wafers 2 and 3, and wafers 5 and 6. In Figure 4 b) an outlier can be seen at the center of wafer 6. This comes from accidental charge left at this measurement spot during the experimental setup.

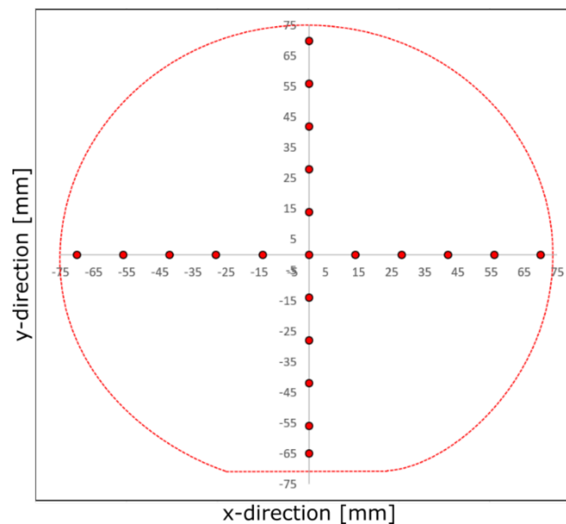

Fig. 3. Explanation of the measurement pattern used for all measurements.

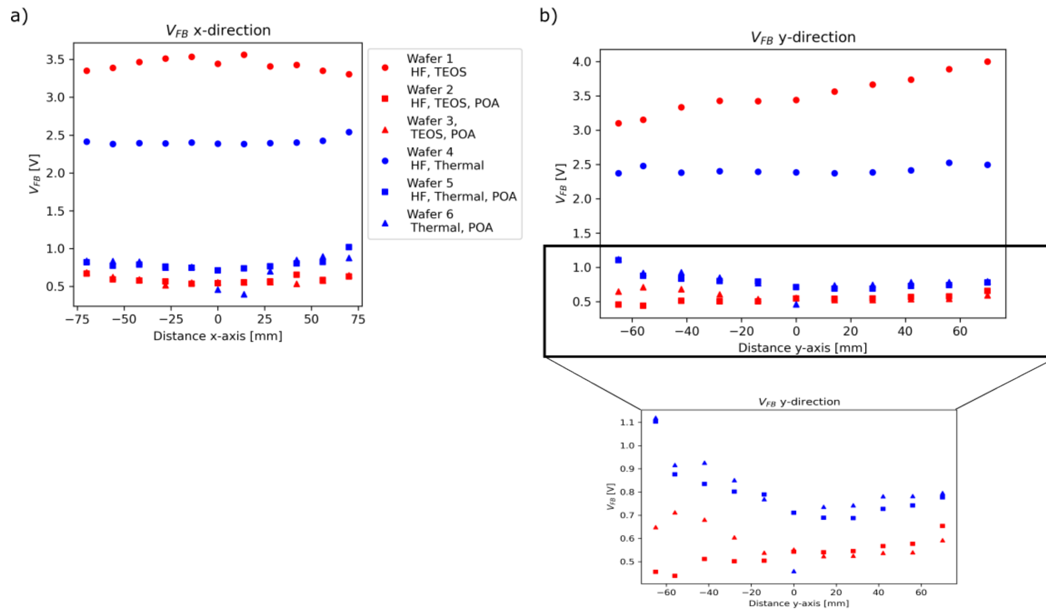

Fig. 4. The flatband voltage, V_{FB}, of all six wafers. a) measurements along the x-axis, b) measurements along the y-axis.

In Figure 5 the EOT data is presented, exhibiting several similarities with the results presented in Figure 4, namely, that the two outlier wafers are wafer 1 and 4, the two wafers that did not receive the POA. This increase in EOT for the other wafers is expected as the POA is performed in a NO atmosphere that slightly adds to the EOT thickness. Another similarity between Figure 4 and 5 is that the two LPCVD TEOS wafers 2 and 3 group together and the two thermal oxide wafers 4 and 5 also group up together. One interesting observation is that the LPCVD TEOS process used resulted in concave thickness profiles, both along the x- and y-axis. This is different from the thermally grown oxides that resulted in convex thickness profiles. The shape of the oxide thickness profiles was not changed significantly with the processing steps considered in this work.

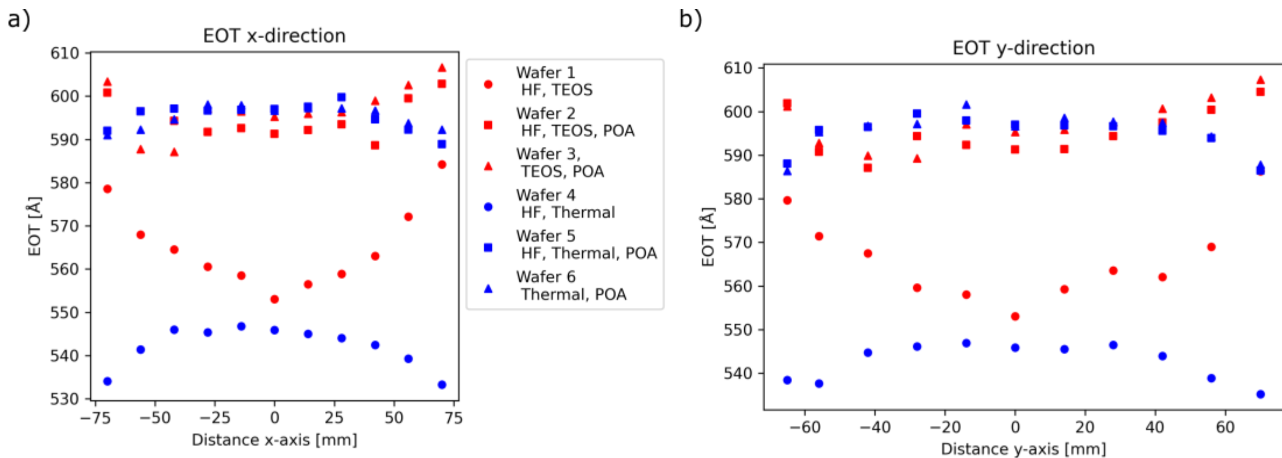

Fig. 5. EOT of all six wafers, a) along the x-axis, b) along the y-axis.

Figure 6 contains the Q_{it} results across the wafers. The trends are much the same as in Figure 4 and 5, the two outlier wafers are wafer 1 and 4, the two wafers that did not receive the POA. This is in line with current understanding of POA in NO atmosphere, as it is densifying the oxide and reducing the density of interface traps [5]. Once again, the other two LPCVD TEOS wafers, 2 and 3, do not have any systematic difference from each other. The same is true for the two remaining thermally oxidized wafers, 4 and 5.

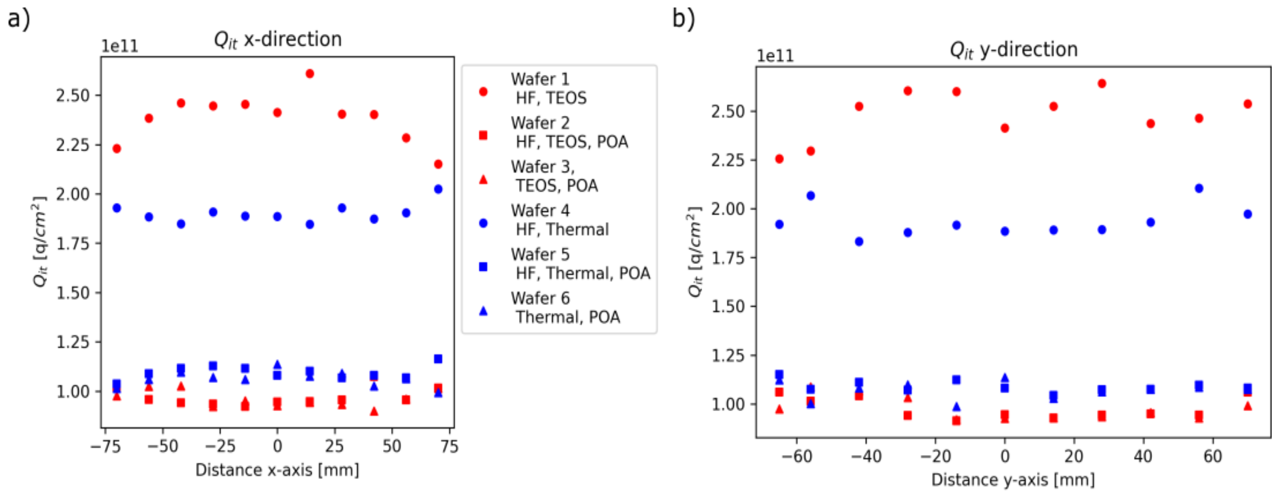

Fig. 6. Q_{it} of all the six wafers, a) along the x-axis, b) along the y-axis.

Figure 7 shows a collection of D_{it} spectra from wafers 1 and 5. Every color used is a separate D_{it} spectrum for each measurement site in Figure 3. All the spectra overlap very well and indicate that the interface traps are very uniformly distributed across the wafers.

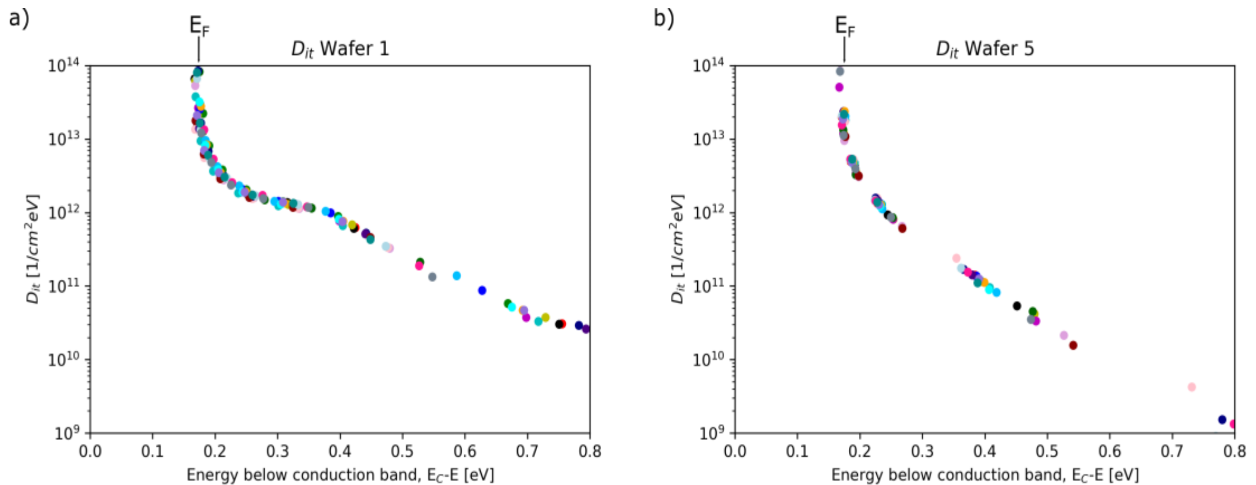

Fig. 7. D_{it} spectra of all the 21 measurement points plotted in the same graph. Every color corresponds to a different measurement site. a) wafer 1, b) wafer 5.

Summary

Six 150 mm homoepitaxial SiC wafers received silicon oxide layers through different combinations of processing steps. These wafers were measured at 21 points using the CnCV measurement technique. The resulting profiles for V_{FB}, EOT and Q_{it} were discussed and although there are a lot of similarities, significant differences became evident. Outlying wafers are always the two wafers that did not receive the POA. This is expected as the POA is supposed to have a large impact on the enhancement of oxide properties. The LPCVD TEOS and the thermal oxides show differences that can be resolved in these measurements. An example is the behavior of the EOT values across the wafers in Figure 5, where the LPCVD TEOS oxides show a concave shape and the thermal oxides show a convex shape even with the pre- and post- processing steps considered in this work. When looking at the wafers that differ only on whether they received the time coupled HF dip or not (wafers 2 and 3 for the LPCVD TEOS case and wafers 5 and 6 for the thermally grown oxides), these wafers could not be systematically distinguished from each other. This could mean that the time coupling between the HF dip and the oxidation is less strict than previously expected, or that the oxide processes considered in this work are not very sensitive to any natural oxide formed prior to the oxide process. A big benefit of the large number of measurement sites, i.e., 21points, is that a lot of

information about uniformity is gained. Looking at the LPCVD TEOS oxides in Figure 4 for example, the V_{FB} of wafer 1 has a weak concave profile along the x-axis, while V_{FB} is lowest closest to the wafer flat and highest at the opposite side of the wafer along the y-axis. As the measurement method is contactless, this enables the wafers to be returned to production after measurement. In the future more processing steps should be considered to see if this method is suitable to either monitor oxide processing or process development.

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