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Effects of 673K Temperature Anneal on a 4H-SiC CMOS NOT Logic Gate

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Abstract. The effects of 673K temperature anneal on a 4H-SiC CMOS NOT logic gate have been investigated. After an annealing at 673K for 30 minutes in ambient atmosphere, a shift of threshold logic voltage, VM, towards higher input voltage by 6.67%, and a hysteresis reduction are observed. Both effects can be related to MOSFETs electrical behavior after the same thermal annealing. The threshold voltage of NMOSFET, VTH, N, increases by 6.67%, whereas PMOSFET one reduces by 11.15%, allowing the VM increase. NMOSFET shows a reduction of its trans-characteristic hysteresis, ΔVH, by -33.3%, as well as PMOSFET one, that is by -20.4%, explaining the hysteresis reduction of NOT gate. Moreover, a more reproducible NOT transfer characteristics is obtained after the 673K annealing.

Introduction

Wide band-gap semiconductors are suitable for harsh environment thanks to their intrinsic physical properties [1]. Among them, 4H polytype of Silicon Carbide, 4H-SiC, has emerged, with the development of lateral devices and integrated circuits, ICs [2]. JFET and BJT based technologies have been demonstrated for high temperature applications with several integrated circuits [3,4]. However, the process easiness allows the CMOS technology to emerge. This one has proven promising with complex ICs able also to operate up to 773K [5-7], with the integration of novel devices [8] or conventional lateral temperature sensors [9,10].

Although demonstration of circuits and devices up to very high temperature, i.e. 773K, have been already done, there is still a lack of knowledge about the reliability of circuit performance, like the repeatability of the results after different temperature anneals.

In this paper, we investigate the static room temperature performances of a 4H-SiC CMOS NOT logic gate after several temperature anneals, which have been heated in ambient atmosphere environment at 673K for 30 minutes. In addition, we relate the NOT gate electrical behavior after thermal annealing to MOSFET one.

Device Structure and Experimental Set-Up

NOT logic gate has been fabricated in 4H-SiC CMOS Fraunhofer IISB's Technology [7]. The process starts with the epitaxial grow of a 10^{15} cm^{-3} n-type layer on a 4H-SiC n-type 350 μm 4° off-axis (0001) substrate. Aluminum and Nitrogen ion implantation, followed by 1973K, 30 minutes, thermal annealing is performed for n-type and p-type doped regions. A doping concentration of 10^{17} cm^{-3} and 10^{16} cm^{-3} is obtained for p-well and n-well regions, respectively. Whereas a doping concentration of $5 \cdot 10^{19}$ cm^{-3} is for high doped p^+ and n^+ regions. A 55 nm thick gate oxide is thermally grown at 1300°C and a post-oxidation annealing is performed at 1300°C in NO

environment to reduce the SiO2/4H-SiC interface state density. All these process steps result in gate oxide capacitance, Cox=62.8nF/cm^2. Gate electrode is made by depositing a 500 nm thick n-type PolySilicon. NiAl and Ti/Al are used for n-type and p-type contact respectively, whereas a Ti/Pt metal layer stack is used for the two lines of metal interconnections. More detailed information regarding process steps is in [7].
The NOT logic gate is made by a NMOSFET with channel width, WN=6µm, and a PMOSFET with channel width, WP=44µm, both with channel length, L=6µm.
Measurements have been made at room temperature, i.e. T=298K, with a Keithley SCS-4200, a SUSS PM5 probe station and with Signatone Corporation manipulators. Each temperature anneals consists of heating the devices in ambient atmosphere at 673K for 30 minutes with a 630W G.Maier Elektrotechnick GmbH hotplate.

Results and Discussion

NOT logic gate Characteristics.

The NOT logic gate is supplied by V_{DD}=20V and transfer characteristics at T=298K after multiple 673K temperature anneals are reported in Fig.1.a). It can be observed that after first 673K temperature anneal, a shift of threshold logic voltage, V_M, of +6.67% and a reduction of hysteresis voltage, from ΔV_H = 0.2V to ΔV_H = 0.15V, are observed, as shown in Fig.1.a)-b). Moreover, a reduction of High Noise Margin, NM_H, of -6.74% and an increase of Low Noise Margin, NM_L, of +6.95%, can be calculated (see Fig.1.c)). Whereas, after the second 673K temperature anneal, almost the same values of V_M and NM_L are reached, with a variation of 0.94% and 1% with respect to the first 673K anneal, and the same value of NM_H is observed in Fig.1.c).
Then, a 673K thermal annealing shows an improvement of NOT performances and a more stable and repeatable transfer characteristic.

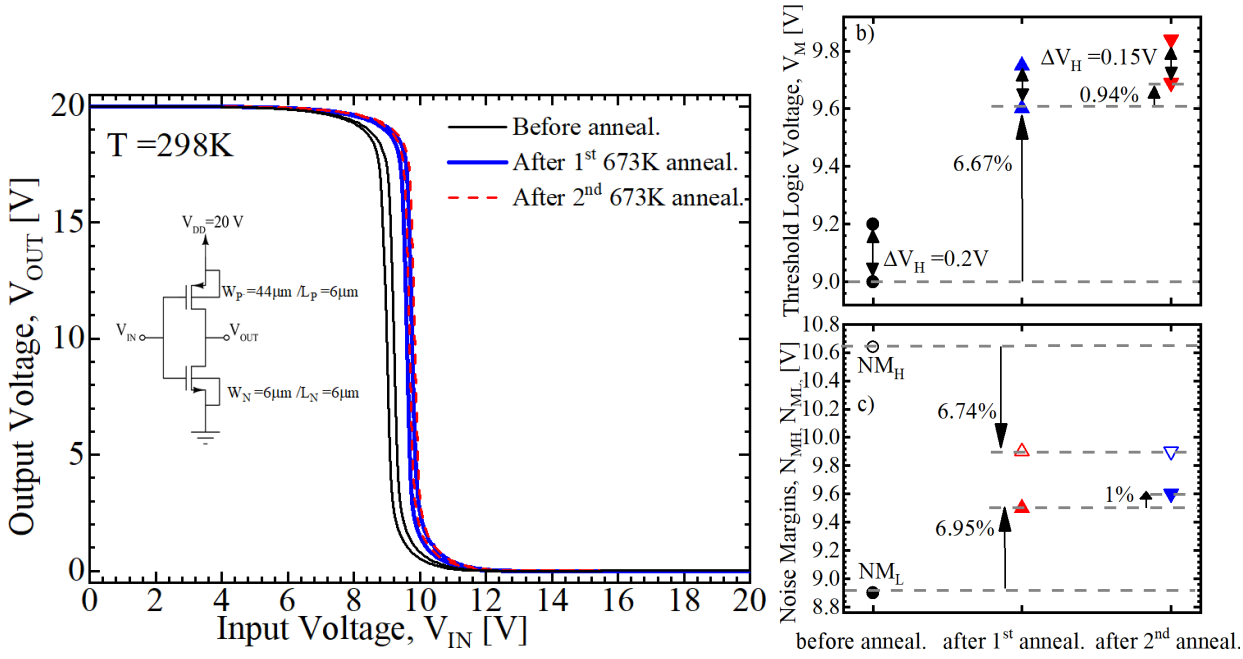

Fig. 1. a) NOT logic gate transfer characteristic before and after 673K temperature annealing, at T=298K and V_{DD}=20V. b) Threshold logic voltage and c) Noise Margins variations.

The effects of the thermal annealing on NOT gate, i.e. shift of its transfer characteristics towards higher voltage and its hysteresis reduction, are related to electrical behaviors of individual devices. Indeed, we analyzed the transfer characteristics in linear region of a NMOSFET and a PMOSFET.

MOSFETs Characteristics.

Trans-characteristics, at $|V_{DS}|$=0.1V, of NMOSFET and PMOSFET, both with W=18µm and L=6µm, before and after the first 673K temperature anneal are in Fig.2.a) and in Fig.3.a), respectively. After the thermal annealing, we observe an increase of NMOSFET threshold voltage, $V_{TH,\,N}$, extracted according to the extrapolation in linear region method [11], by 6.93% and a reduction of PMOSFET threshold voltage, $V_{TH,\,P}$, by -11.15%. This phenomenon can be related to the release of fixed oxide charge, allowing a shift of the flat band voltage towards higher values. Moreover, a reduction of the hysteresis of NMOSFET and PMOSFET characteristics by - 33.3% and -20.4%, respectively, can be observed, which agrees with the reduction of the NOT gate hysteresis. In this case, thermal energy supplied by 673K annealing could reduce the density of acceptor like slow border traps [12], leading to the hysteresis reduction.
Subthreshold Slope, SS, is obtained from the slope of $I_{DS} - V_{GS}$ curves, under subthreshold conditions at V_{DS} =0.1V [13] and same SS is observed for NMOSFET, (see Fig.2.c).
Finally, field effect channel mobility is extracted from trans-characteristics in Fig.2.a) and Fig.3.a) according to [14]:

$$\mu_{CH} = \frac{dI_{DS}}{dV_{GS}}\Big|_{V_{DS}=0.1V} \frac{L}{V_{DS} C_{ox} W} \tag{1}$$

and, also in this case, same maximum channel mobility, $\mu_{CH,\,N\,peak}$=19.4 cm^2/Vs, was observed (see Fig.2.d). In contrast, the PMOSFET shows a SS reduction of -23.8% and an increase of the channel mobility maximum, $\mu_{CH,\,P\,peak}$ of 4.1% (see Fig. 3.c and d)), which can be related to a reduction of SiO_2/4H-SiC interface defects density [15] and, therefore, to a decrease of the associated scattering [16].
Moreover, substituting extracted NMOSFET threshold voltage values before and after thermal annealing, see Fig. 2.b) and Fig.3.b), and the channel mobility peaks, see Fig.2.d) and Fig.3.d), in the following equation of V_M [17]:

$$V_M = \frac{V_{TH,N} + r\,(V_{DD} - |V_{TH,P}|)}{1+r} \tag{2}$$

where:

$r = \sqrt{\frac{\mu_{CH,\,P\,peak} C_{OX} \frac{W_P}{L}}{\mu_{CH,\,N\,peak} C_{OX} \frac{W_N}{L}}}$, we obtain a ΔVM = 0.84V, almost near to the experimental one of 0.6V, Fig.1.b), allowing to explain the V_M shift towards higher value.

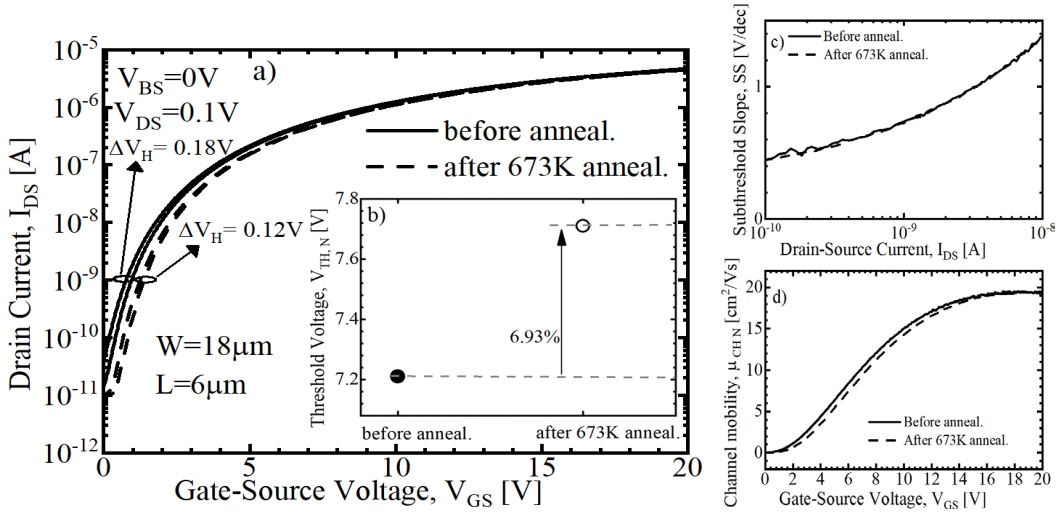

Fig. 2. a) Trans-characteristic of NMOSFET before and after 673K temperature anneal. b) The inset shows the extracted $V_{TH,N}$. In c) Subthreshold Slope and d) field-effect channel mobility.

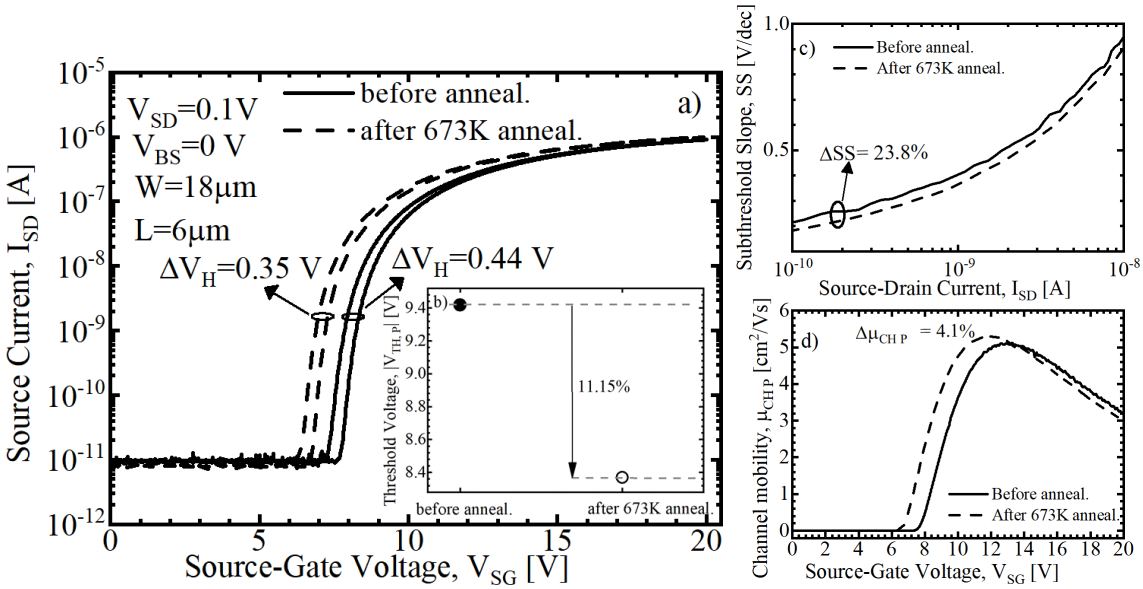

Fig. 3. a) Trans-characteristic of PMOSFET before and after 673K temperature anneal. b) The inset shows the extracted $V_{TH,P}$. In c) Subthreshold Slope and in d) field-effect channel mobility.

Summary

Analysis of NOT logic gate transfer characteristics after multiple 673K temperature anneals have been done and its electrical behavior linked to single lateral MOSFETs ones. In particular, the V_M shift towards a higher input voltage value is due to the $V_{TH,N}$ increase by 6.93% and $V_{TH,P}$ decrease by 11.15%. Whereas the NOT transfer characteristics hysteresis reduction can be related to both MOSFETs' hysteresis reduction after the thermal annealing. Then, a 30 minutes 673K thermalannealing seems to improve the overall devices and circuits performances, improving, also, the repeatability of NOT gate characteristics after multiple temperature anneals.

Author Contributions

Conceptualization, N.R and L.D.B; methodology N.R.; validation N.R., L.D.B, L.B and A.M; formal analysis N.R. and L.D.B; investigation N.R., L.D.B, M.R, and L.B; data curation N.R. and L.B.; writing-original draft N.R, L.D.B.; M.R., R.L., and G.D.L; writing-review and editing, N.R, L.D.B., M.R., R.L, and G.D.L; project administration A.R. and M.R.; funding acquisition A.R. All authors have read and agreed to the published version of the manuscript.

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