Materials Science Forum
ISSN: 1662-9752, Vol. 1191, pp 61-67
doi:10.4028/p-S3kheK

Submitted: 2025-09-12
Revised: 2025-12-19
Accepted: 2026-02-26
Online: 2026-05-19

Carbon Vacancy Engineering on High-Temperature Annealing as a Cost-Effective Approach for Reverse Recovery Suppression in SiC-MOSFETs

Minori Matsuoka[1,a*], Daiki Soda[1,b], Kosuke Miyazaki[1,c],Toshikazu Tanioka[1,d], Kazuya Tojima[1,e], Akira Kiyoi[2,f], Yasuhiro Kagawa[1,g] and Tetsuya Nitta[1,h]

[1]Power Device Works, Mitsubishi Electric Corporation,1-1-1 Imajuku-higashi, Nishi-ku, Fukuoka-shi, Fukuoka, 819-0192, Japan

[2]Advanced Technology R&D Center, Mitsubishi Electric Corporation, 8-1-1 Tsukaguchi-honmachi, Amagasaki-shi, Hyogo, 661-8661, Japan

[a*]Matsuoka.Minori@db.mitsubishielectric.co.jp, [b]Soda.Daiki@dc.MitsubishiElectric.co.jp, [c]Miyazaki.Kosuke@dw.MitsubishiElectric.co.jp, [d]Tanioka.Toshikazu@eb.MitsubishiElectric.co.jp, [e]Ishibashi.Kazuya@ak.MitsubishiElectric.co.jp, [f]Kiyoi.Akira@ay.MitsubishiElectric.co.jp, [g]Kagawa.Yasuhiro@cj.mitsubishielectric.co.jp, [h]Nitta.Tetsuya@ea.MitsubishiElectric.co.jp

Keywords: MOSFET, body diode, activation annealing, carbon vacancy, reverse recovery charge, electrical characteristics.

Abstract. A body diode is commonly employed as a free-wheeling diode to reduce costs of SiC components instead of an external Schottky barrier diode. However, one of the key issues is higher reverse recovery loss due to bipolar charge contribution to reverse recovery charge. In this study, we investigated the impact of high-temperature annealing on the characteristics of MOSFETs as a cost-effective approach to introduce minority carrier lifetime killers. The trap densities of $Z_{1/2}$ center and $EH_{6/7}$ center can be controlled by activation annealing temperature. Q_{rr} of 1900°C measured at 150°C was significantly decrease by 67% compared to that of 1750°C attributed to the 89% suppression of Q_{BIP}. However, reverse leakage current increased adversely with the activation annealing temperature. R_{on} and V_{th} increased with the activation annealing temperature. The trade-off of the annealing temperature worsened slightly compared to that of the doping concentration. It is still possible that high-temperature annealing represents a cost-effective approach to improve the reverse recovery characteristics of the body diode.

Introduction

Silicon carbide (SiC) is a suitable material for power devices due to its superior properties such as wide bandgap, high critical electric field, and high thermal conductivity. A body diode is a parasitic p-n diode within a MOSFET structure. In typical switching applications, a body diode is commonly employed as a free-wheeling diode to reduce costs of SiC components instead of an external Schottky barrier diode. The use of the body diode can contribute to cost reduction in SiC components and system miniaturization. However, there are several issues related to the use of the body diode. One of the key issues is a higher reverse recovery loss due to the contribution of bipolar charge (Q_{BIP}) to the reverse recovery charge (Q_{rr}). The recovery current when using the body diode is larger than that when using an external Schottky barrier diode. This is attributed to the fact that Q_{BIP} is significantly large due to the body diode being a bipolar device. One measure to reduce the reverse recovery loss is introducing minority carrier lifetime killers. It is known that $Z_{1/2}$ center is the most representative carrier lifetime killer in n-type 4H-SiC [1]. $Z_{1/2}$ center and $EH_{6/7}$ center [2] are identified as traps caused by carbon vacancies [3]. Methods for generating carbon vacancies include electron irradiation [4,5], proton irradiation [6,7], and high-temperature annealing [8]. Electron irradiation and Proton irradiation need additional processes and equipment, while high-temperature activation annealing can potentially introduce carrier lifetime killers without additional processes or equipment, making it cost-effective. This is because the activation of the ion implantation layers needs annealing at temperatures above 1600°C, allowing for the simultaneous introduction of lifetime killers [9]. Few

studies have reported on the reverse recovery loss of the body diode related to high-temperature activation annealing. Therefore, we investigated the effect of the activation annealing temperature on electrical characteristics of SiC-MOSFETs.

Experiment

Figure 1 shows the cross-sectional schematics of fabricated SiC planar MOSFETs with 1.7 kV-rating on n-type 4H-SiC (0001) wafer. The off-cut angle of the wafer is 4°. Figure 2 illustrates the MOSFETs fabrication processing flow. After the ion implantation process, these MOSFETs were annealed in Ar atmosphere with a carbon cap. The processing temperatures were set at 1750°C, 1800°C and 1900°C, respectively. The duration at the set temperature was the same. Subsequently, the gate oxidation and the metallization were carried out. The fabricated MOSFETs were evaluated for the trap density of $Z_{1/2}$ center and $EH_{6/7}$ center around the PN junction measured by deep level transient spectroscopy (DLTS). Afterwards, we measured the reverse recovery characteristics, reverse leakage current characteristics, and on-state characteristics of the MOSFETs. Typical data were plotted for each activation annealing temperature in the following Figs. 3-8 ,10.

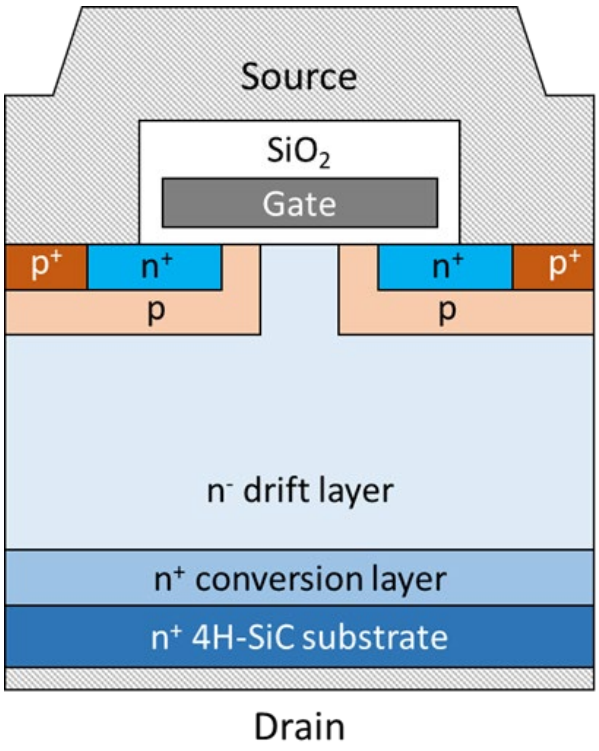


Fig. 1. Cross-sectional schematic diagram of the planar SiC-MOSFET.

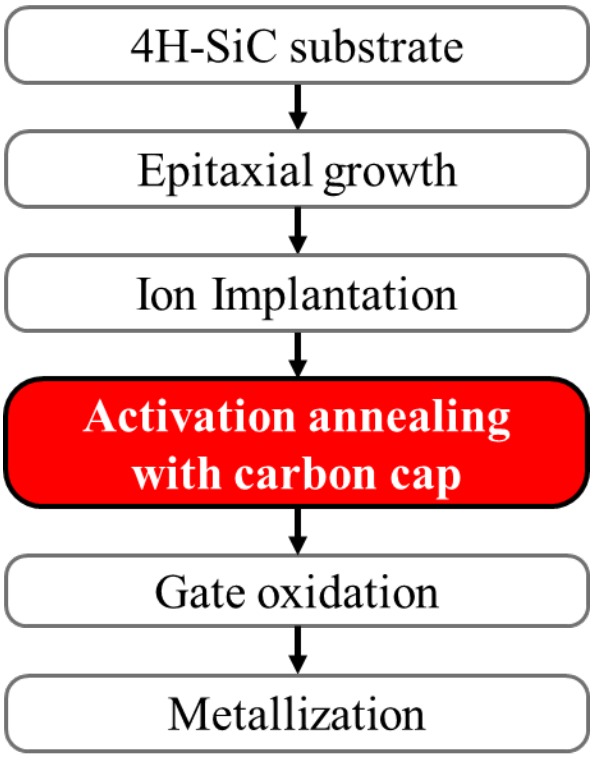


Fig. 2. The MOSFETs fabrication processing flow. The activation annealing temperatures were set at 1750°C, 1800°C and 1900°C, respectively.

Results and Discussion

Figure 3 shows the trap densities of $Z_{1/2}$ center and $EH_{6/7}$ center calculated from DLTS spectra. DLTS measurement conditions are as follows: reverse bias of -30 V, pulse bias of -15 V and a rate window of 192 ms, with G-S shorted. The DLTS spectrum has two peaks at positions of 300 K and 678 K, which are related to the $Z_{1/2}$ center and $EH_{6/7}$ center. The defect densities at 1900°C are significantly increased compared to 1750°C and 1800°C. Figures 4 shows the dependence of trap densities on the activation annealing temperature. The trap densities of both $Z_{1/2}$ center and $EH_{6/7}$ center increase exponentially with the activation annealing temperature, reaching approximately 10^{14} /cm^3 at 1900°C. These results suggest that the trap densities of $Z_{1/2}$ center and $EH_{6/7}$ center can be efficiently controlled by adjusting annealing temperature.

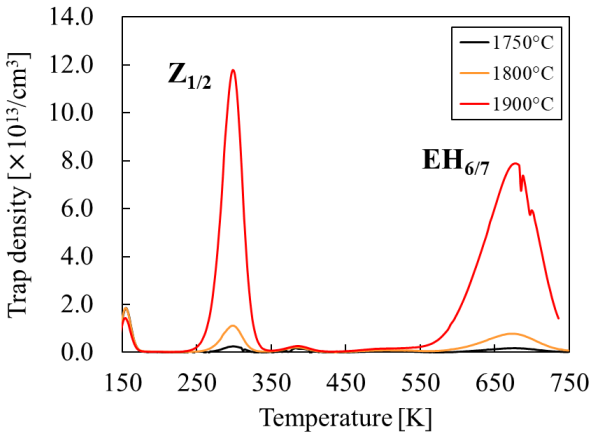


Fig. 3. Trap density calculated from DLTS spectrum.

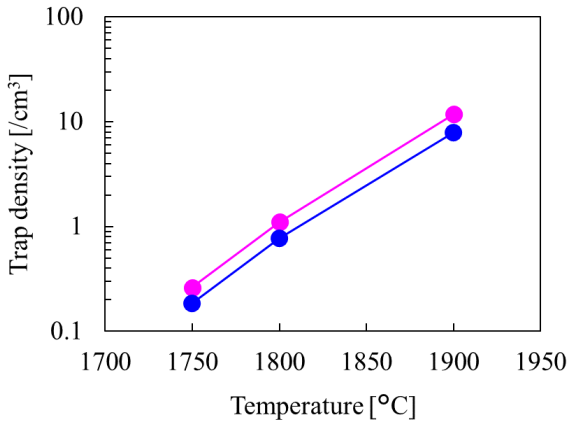


Fig. 4. Dependency of activation annealing temperature on trap density.

Figures 5(a) and 5(b) show the typical reverse recovery waveforms at 25°C and 150°C. The reverse recovery characteristics were measured with the double pulse testing method, and the supply voltage and switching drain-source current are 900 V and 265 A/cm^2, respectively. The gate voltages of the upper arm and the lower arm are −7 V and −7/+15 V, respectively. At 25°C, there is almost no difference among the three waveforms, and the reverse recovery currents are independent of the activation annealing temperatures. On the other hand, at 150°C, the reverse recovery current decreases dramatically from 176 A/cm^2 to 131 A/cm^2 between 1750°C and 1900°C. The reverse recovery charge (Q_{rr}) is defined in accordance with JEP201 published by JEDEC as follows,

$$Q_{rr} = Q_{BIP} + Q_{OSS} \tag{1}$$

$$Q_{rr} = -\int_{t_0}^{t_1} J_{bd}\, dt \tag{2}$$

where t_0 is defined as the moment when the current density reaches zero, and t_1 is defined as the point when the drain voltage reaches 98%. The reverse recovery charge (Q_{rr}) was then calculated from the current density between these two time points.

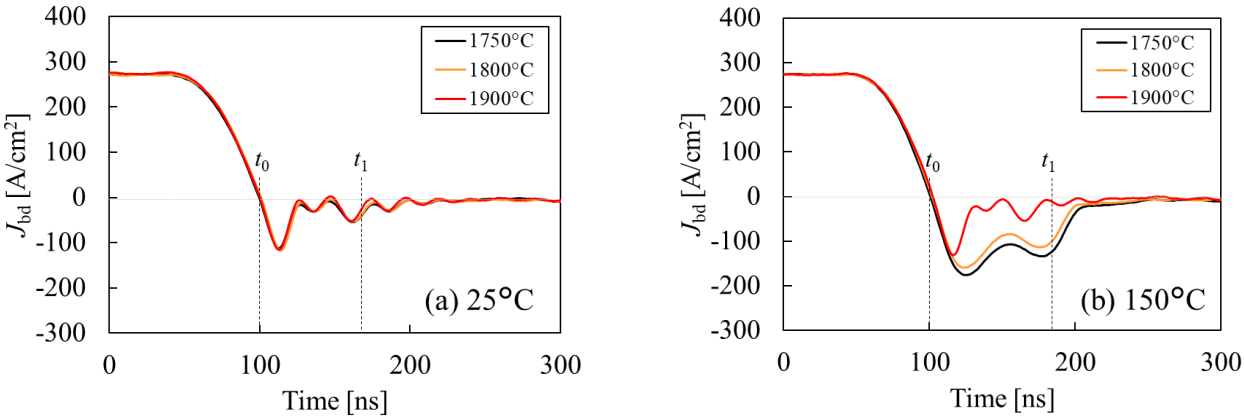


Fig. 5. Typical reverse recovery waveforms of the body diode current J_{bd} (a) at 25°C and (b) at 150°C.

Figures 6(a) and 6(b) show the composition of Q_{rr} for each annealing temperature (a) at 25°C and (b) at 150°C. The capacitive charge (Q_{OSS}) is independent of the activation annealing temperature. At 25°C, Q_{rr} and Q_{BIP} of 1900°C is reduced by 13% and 51% compared to that of 1750°C, respectively. At 150°C, Q_{BIP} is reduced significantly with the activation annealing temperature. Q_{rr} of 1900°C is reduced by 67% compared to 1750°C attributed to the 89% suppression of Q_{BIP}. This suggests that the carrier lifetime of 1900°C is significantly decreased at 150°C. Therefore, high-temperature annealing represents an effective method to improve the reverse recovery characteristics of the body diode.

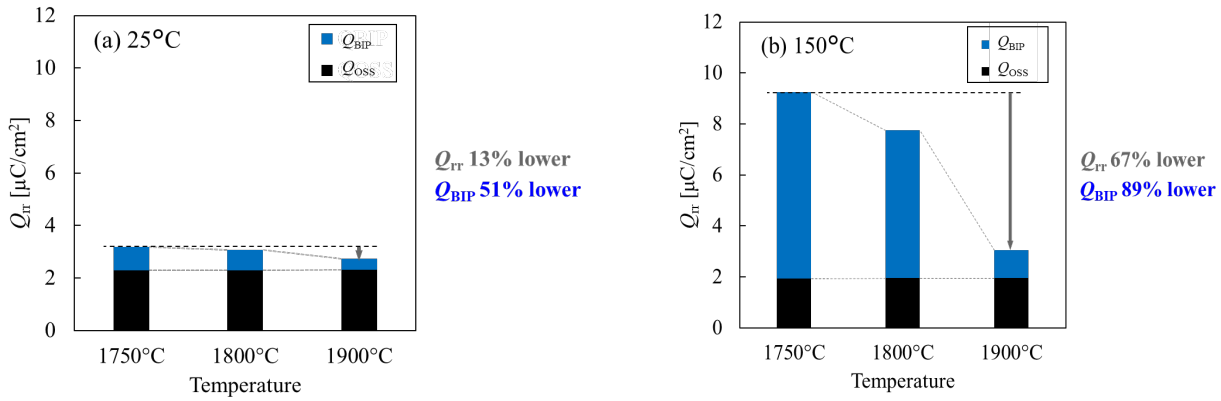


Fig. 6. Composition of Q_{rr} for each annealing temperature (a) at 25°C and (b) at 150°C.

Figures 7(a) and 7(b) show the typical reverse leakage waveforms at 25°C and 150°C. A source-gate voltage (V_{GS}) of -7V is applied. The reverse leakage current increases adversely with the activation annealing temperature both at 25°C and 150°C. The reverse leakage current characteristics are nearly the same at 1750°C and 1800°C, while the reverse leakage current at 1700 V increases by an order of magnitude at 1900°C.

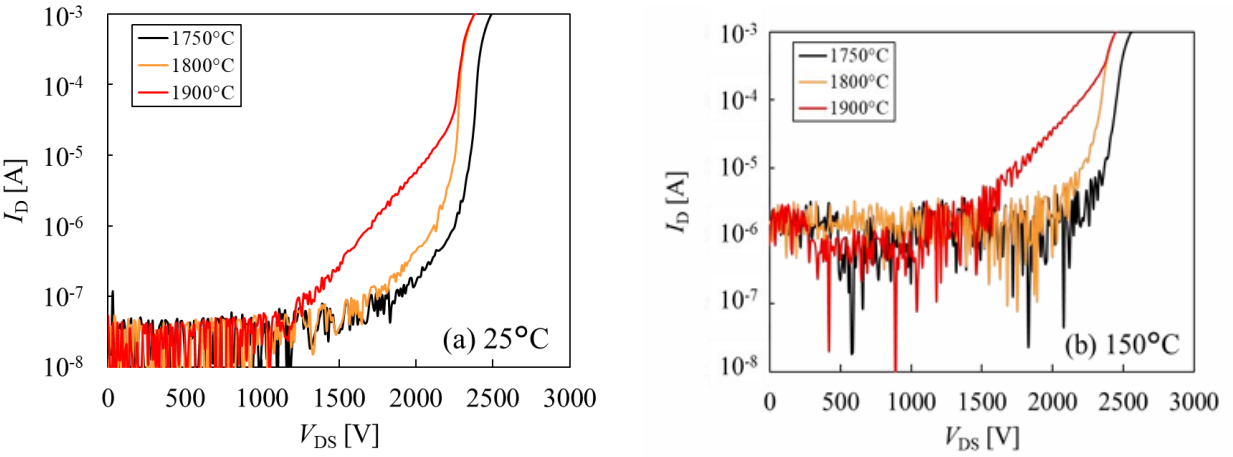
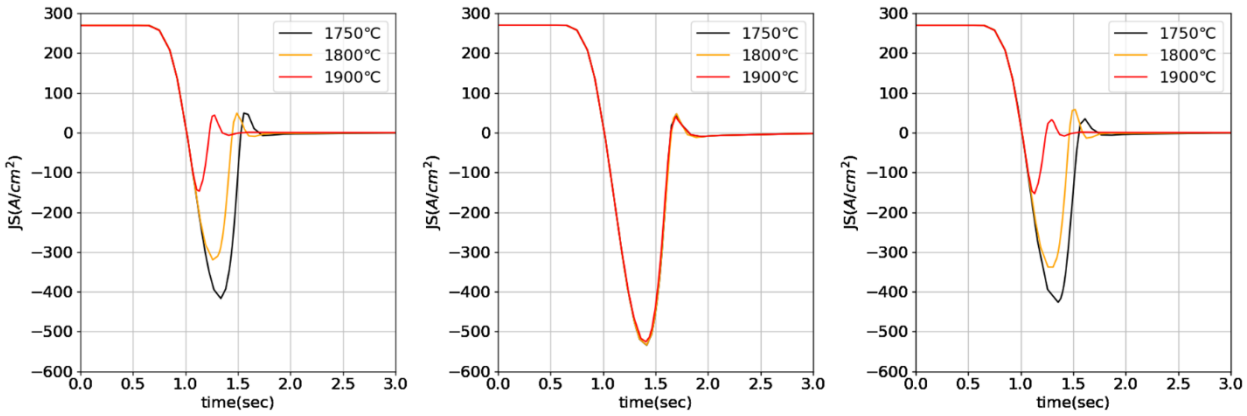


Fig. 7. Typical reverse leakage characteristics for the SiC-MOSFETs with various activation annealing temperature of V_{GS}= -7 V (a) at 25°C and (b) at 150°C.

To confirm the impact of the $Z_{1/2}$ center and $EH_{6/7}$ center on the reverse recovery characteristics, TCAD simulations were conducted in three different cases. Figure 8(a)-(c) show simulation results of reverse recovery waveform at 150°C (a) with only $Z_{1/2}$ center, (b) with only $EH_{6/7}$ center and (c) with both $Z_{1/2}$ center and $EH_{6/7}$ center. The trap density, energy and cross-section obtained from DLTS are utilized to simulation parameters as shown in Table 1. In the simulation utilizing with only $Z_{1/2}$ center (Fig. 8(a)), both the reverse recovery current and the reverse recovery time decrease with increasing the activation annealing temperature. The reverse recovery current and the recovery time in the simulation utilizing only $EH_{6/7}$ center (Fig. 8(b)) show no significant dependence on the activation annealing temperature. In the simulation utilizing $Z_{1/2}$ center and $EH_{6/7}$ center (Fig. 8(c)), the reverse recovery waveforms exhibited a trend similar to those obtained with the $Z_{1/2}$ center. This trend is also consistent with the measured reverse recovery characteristics. Therefore, we speculate that reverse recovery current is strongly dependent on the density of $Z_{1/2}$ center.

Table 1. Simulation parameters obtained by DLTS.

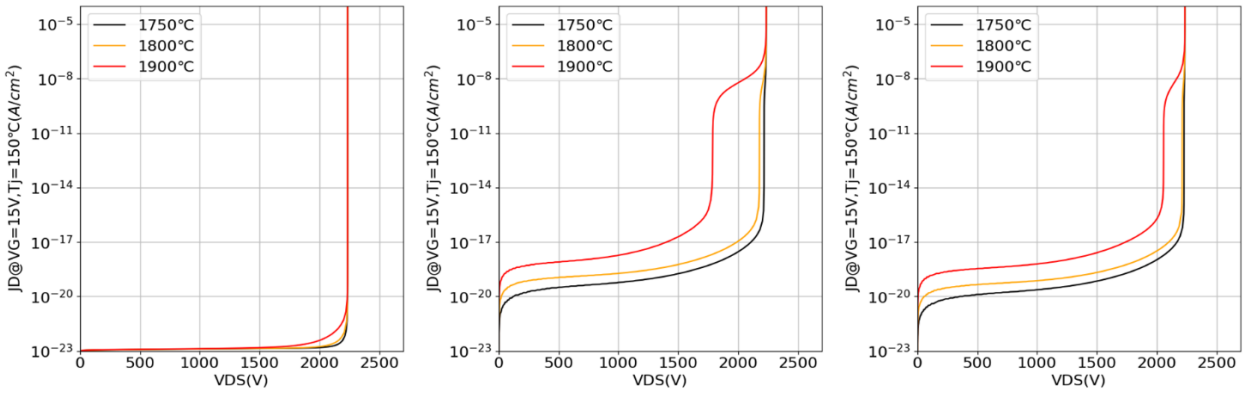
trap	Energy [eV]	σ_e [cm^2]
$Z_{1/2}$	E_C-0.63	1.66e^{-15}
$EH_{6/7}$	E_C-1.44	3.39e^{-16}



(a) with $Z_{1/2}$ (b) with $EH_{6/7}$ (c) with $Z_{1/2}$ and $EH_{6/7}$

Fig. 8. Simulation results of reverse recovery waveform at 150°C (a) with $Z_{1/2}$ center, (b) with $EH_{6/7}$ center and (c) with $Z_{1/2}$ center and $EH_{6/7}$ center.

Figure 9(a)-(c) show the simulation results of the reverse recovery waveform at 150°C (a) with $Z_{1/2}$ center, (b) with only $EH_{6/7}$ center and (c) with both of $Z_{1/2}$ center and $EH_{6/7}$ center. In the simulation utilizing only $Z_{1/2}$ center (Fig. 9(a)), the reverse leakage current shows slightly dependence on the activation annealing temperature. The reverse leakage current in the simulation utilizing only $EH_{6/7}$ center (Fig. 9(b)) increases with activation annealing temperature. In the simulation utilizing $Z_{1/2}$ center and $EH_{6/7}$ center (Fig. 9(c)), the reverse leakage current exhibit a trend like those obtained with the $EH_{6/7}$ center alone. This trend is also consistent with the measured reverse leakage current characteristics. Therefore, we speculate that the reverse leakage current is strongly dependent on the density of $EH_{6/7}$ center.



(a) with $Z_{1/2}$ (b) with $EH_{6/7}$ (c) with $Z_{1/2}$ and $EH_{6/7}$

Fig. 9. Simulation of off-state I-V characteristics at 150°C (a) with $Z_{1/2}$ center, (b) with $EH_{6/7}$ center and (c) with $Z_{1/2}$ center and $EH_{6/7}$ center.

Figure 10(a) and (b) shows trade-off between on-resistance R_{on} and threshold voltage V_{th} of 25°C (a) at 25°C and (b) 150°C. R_{on} and V_{th} increase with high-temperature annealing because the net accepter concentration increases. However, there is a slight difference between the trade-off of the activation annealing temperature and that of doping concentration. It suggests that there are other factors that contribute to the increase in on-resistance.

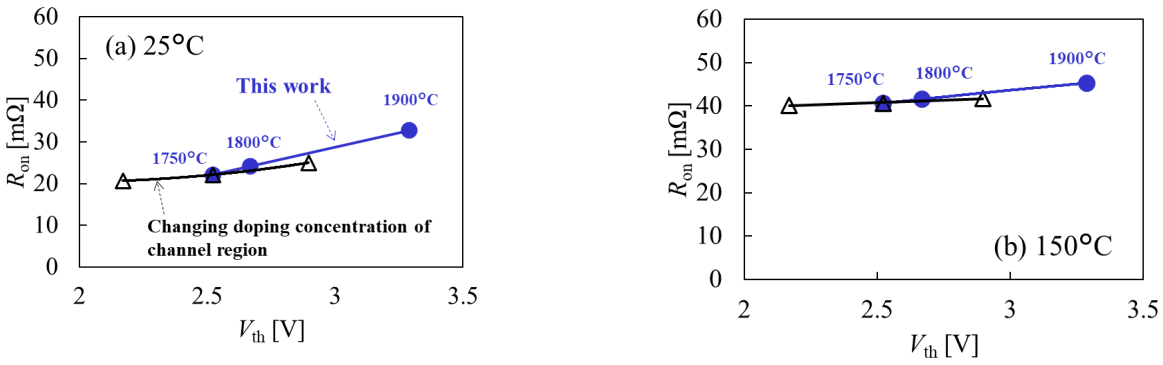


Fig. 10. Trade-off of activation annealing temperature and doping concentration between threshold voltage V_{th} at 25°C and on-resistance R_{on} (a) at 25°C and (b) at 150°C.

Summary

We investigated the impact of high-temperature annealing on the characteristics of MOSFETs as a cost-effective approach to introduce carrier lifetime killers for reverse recovery suppression. The trap densities of $Z_{1/2}$ center and $EH_{6/7}$ center were controlled up to approximately 10^{14} /cm^3 through the activation annealing temperature. Q_{rr} of 1900°C was reduced compared to that of 1750°C, attributed to the significant suppression of Q_{BIP}. However, the reverse leakage current increased adversely with the activation annealing temperature. The trade-off between R_{on} and V_{th} of annealing temperature worsened slightly compared to that of doping concentration.

References

[1] K. Danno, T. Hori and T. Kimoto, Impacts of growth parameters on deep levels in n-type 4H-SiC, J. Appl. Phys. 101, 053709 (2007).

[2] N. T. Son, X. T. Trinh, L. S. Løvlie, B. G. Svensson, K. Kawahara, J. Suda, T. Kimoto, T. Umeda, J. Isoya, T. Makino, T. Ohshima, and E. Janze, Negative-*U* System of Carbon Vacancy in 4*H*-SiC, Phys. Rev. Lett. 109, 187603 (2012).

[3] G. Alfieri and T. Kimoto, Resolving the level in 4H-SiC by Laplace-transform deep level transient spectroscopy, Appl. Phys. Lett. 102, 152108 (2013).

[4] P. Dong, Y. Qin, X. Yu, X. Xu, Z. Chen and L. Li, Electron Radiation Effects on the 4H-SiC PiN Diodes Characteristics: An Insight from Point Defects to Electrical Degradation, IEEE Access. 7, 170385 (2019).

[5] T. Kimoto and K. Danno, Lifetime-killing defects in 4H-SiC epilayers and lifetime control by low-energy electron irradiation, phys. stat. sol. (b) 245, 1213 (2008).

[6] A Castaldini, A Cavallini and L Rigutti Assessment of the intrinsic nature of deep level Z_1/Z_2 by compensation effects in proton-irradiated 4H-SiC, Semicond. Sci. Technol. 21 (2006) 724–728.

[7] P. Hazdra and S. Popelka, Optimization of SiC Power p-i-n Diode Parameters by Proton Irradiation, IEEE Access. 65, 4483 (2018).

[8] E. Saito, J. Suda and T. Kimoto, Control of carrier lifetime of thick n-type 4H-SiC epilayers by high-temperature Ar annealing, Appl. Phys. Exp. 9, 061303 (2016).

[9] M. Spera, D. Corso, S. Di Franco, G. Greco, A. Severino, P. Fiorenza, F. Giannazzo and F. Roccaforte, Effect of high temperature annealing (T > 1650 °C) on the morphological and electrical properties of p-type implanted 4H-SiC layers, . Mater. Sci. Semicond. Proc. 93 (2019) 274–279.