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Effect of Varying N+ Source Implantation Depth on the Electrical Characteristics of 1.2 kV 4H-SiC MOSFETs

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Abstract. The heavily doped N+ source region in 4H-SiC MOSFETs is a critical design parameter, as its depth and the profile strongly influence contact resistivity and conduction efficiency. This work investigates the impact of varying N+ implantation depth on the electrical performances of 1.2 kV MOSFETs in both Nominal (linear cell) and Hexagonal (HEXFET) architectures. By varying implantation energy at a fixed dose, three junction depths were obtained: 0.22 µm (shallow), 0.24 µm (moderate), and 0.27 µm (deep). Transfer Length Method (TLM) measurements revealed a significant reduction in source contact resistivity with increasing depth, from 3.91×10^{-5} Ω·cm² (shallow) to 1.22×10^{-6} Ω·cm² (deep). For Nominal MOSFET design, electrical measurements confirmed a corresponding decrease in specific on-resistance ($R_{on,sp}$), from 3.05 to 2.89 mΩ·cm². However, deeper implants introduced greater lateral straggle, shortening the effective channel length and reducing the threshold voltage (V_{th}) from 2.25 V to 1.96 V. The channel barrier potential lowering associated with lateral straggle increased leakage current in the blocking mode, resulting in reduced breakdown voltage (BV). For Nominal MOSFETs, BV decreased from 1610 V in the shallow split to 1470 V in the deep split, while HEXFETs exhibited sharper BV degradation due to their higher channel density. To address this limitation, optimized JFET doping was introduced, restoring the BV of the deep split to 1560 V in the Nominal architecture. These results demonstrate that although increased N+ depth improves conduction by lowering contact resistance, careful co-optimization with P-well and JFET design is necessary to suppress high leakage current during blocking mode.

Introduction

4H-SiC has emerged as the leading wide bandgap semiconductor for advanced power electronics, offering a wide bandgap of 3.26 eV, a high critical electric field of approximately 3 MV/cm, and excellent thermal conductivity. These material advantages enable MOSFETs with significantly lower conduction and switching losses compared to silicon, while also supporting high temperature and high frequency operation. Today, 4H-SiC MOSFETs are used in a broad range of automotive, industrial, and renewable energy applications, with 1.2 kV devices serving as a key voltage class for converters, motor drives, and charging systems [1-3]. To further develop these applications toward higher efficiency, it is essential to pursue an optimal and area efficient design. A primary strategy involves reducing conduction losses within a given area, commonly expressed as the specific on-resistance ($R_{on,sp}$). The $R_{on,sp}$ of a MOSFET originates from several components, including channel resistance, JFET region resistance, drift layer resistance, and contact resistance. While each constituent can be individually optimized to lower $R_{on,sp}$, careful consideration is necessary since these parameters are interdependent and often governed by trade-off relationships [4].

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The heavily doped N+ source region plays an important role in forming a low resistance ohmic contact to the source electrode. Prior studies have shown that optimizing the implantation profile and dimensions of the N+ source can reduce the overall resistance in 4H-SiC power devices [5,6]. The depth of the N+ source can be considered as an important design parameter. From a fundamental standpoint, electrical resistance is inversely proportional to the effective cross-sectional area available for current flow. Extending the N+ junction deeper into the semiconductor increases the effective current carrying cross-section beneath the source contact, which mitigates current crowding near the surface and lowers the overall contact resistance. Consequently, a deeper N+ source enhances carrier injection by widening the conduction path, thereby directly contributing to the reduction of $R_{on,sp}$. To create a deeper N+ profile, a higher ion implantation energy is used. However, by employing a higher implantation energy, the lateral straggle of the implanted region increases [7]. Although this has been shown for other implantations, the effects on the N+ source region have yet to be studied in sufficient detail. Therefore, this study undertakes a comprehensive evaluation of N+ implantation depth and its implications on electrical performance of 1.2 kV 4H-SiC MOSFETs.

In this study, 1.2 kV 4H-SiC MOSFETs were fabricated with three distinct N+ junction depths by varying the nitrogen ion implantation energy. Electrical characterization included Transfer Length Method (TLM) measurements to extract contact resistivity, as well as static characteristics measurements to assess conduction and blocking behaviors. Complementary TCAD simulations and SEM cross-sectional imaging were employed to validate the physical junction depths and to analyze the influence of lateral straggle on channel potential. Strategies such as JFET optimization are further explored with deep N+ split as a means of reducing the leakage current during the blocking mode.

Design and Fabrication

Three 4H-SiC wafers were employed for this study, incorporating both linear (Nominal) and hexagonal (HEXFET) device layouts, as shown in Fig. 1(a) and Fig. 1(b). The fabrication sequence included ion implantations to form the JFET, P-well, N+ source, P+ body, and Junction Termination Extension (JTE) regions, followed by a high-temperature activation anneal to electrically activate dopants and repair implantation induced lattice damage. All implantation parameters and subsequent process steps were kept identical across the wafers, with the only variation being the N+ source implantation depth, adjusted by implant energy to achieve shallow, moderate, and deep N+ junction profiles. Here, Fig. 2(a) shows the TCAD simulated cross section of the device structures with three N+ source depths, while Fig. 2(b) depicts the corresponding SEM cross sections from the fabricated devices with N+ split.

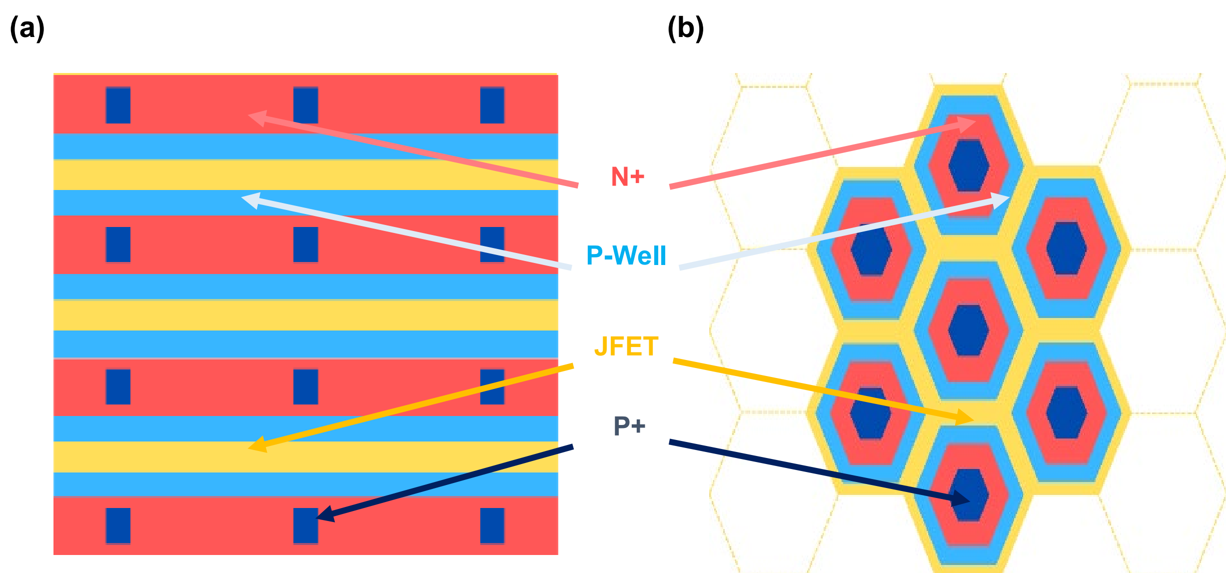

Fig. 1. Top-view of the cell layout for (a) Nominal MOSFET and (b) HEXFET device.

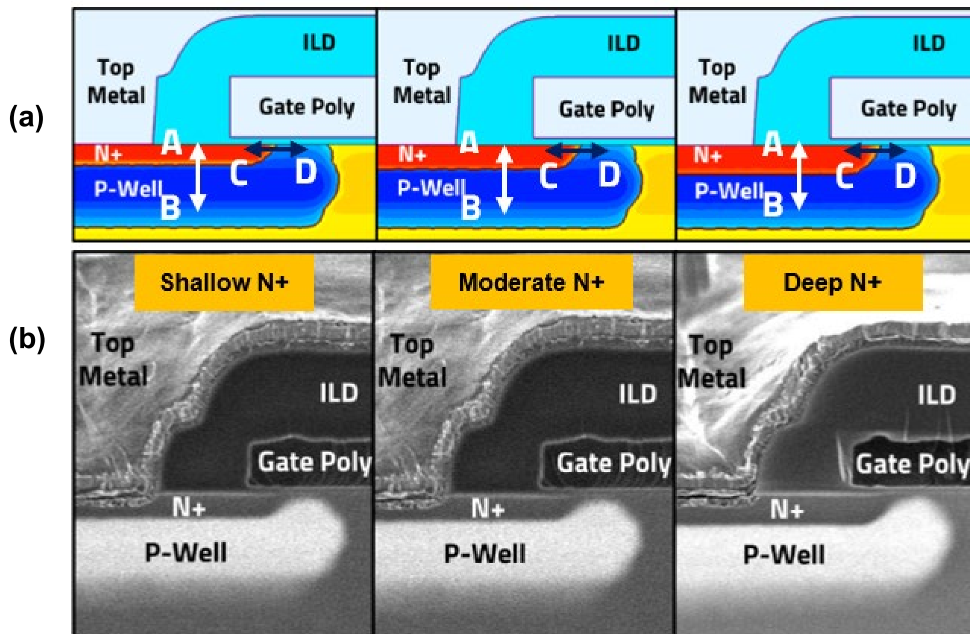

Fig. 2. (a) TCAD simulated, and (b) SEM cross-sections of shallow, moderate and deep N+ configurations. Depths: Shallow - 0.22 µm, Moderate - 0.24 µm, and Deep - 0.27 µm.

Lower implant energies yielded shallower N+ junction depths, whereas higher energies yielded progressively deeper profiles. The N+ Implant doses remained the same for all 3 wafers. Following the thermally grown gate oxide, polysilicon was deposited and patterned, after which an interlayer dielectric (ILD) was deposited. Contact etching was then performed. Nickel was subsequently deposited and annealed to form low resistance ohmic contacts through nickel silicidation. This was followed by metal deposition for interconnection, and finally a passivation layer was deposited and patterned to complete the device fabrication. The same set of photomasks was used for all three wafers, as the only variation in this study was the N+ implantation energy. The fabrication process was conducted at Clas-SiC wafer fab in United Kingdom.

Fig. 3 (a) shows the TCAD simulated vertical doping profiles extracted along the A-B cutline indicated in Fig. 2(a). The junction depths were approximately 0.22 µm, 0.24 µm, and 0.27 µm for the shallow, moderate, and deep implants, respectively. The lateral doping distribution across the channel region (C-D cutline) is shown in Fig. 3(b).

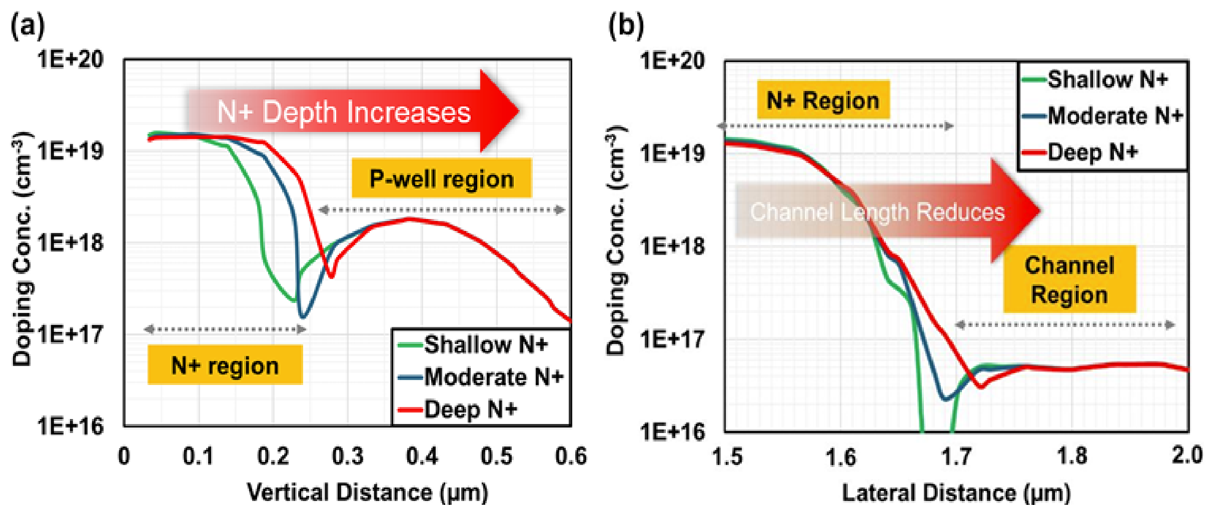

Fig. 3. (a) Vertical doping profile (across A-B cutline), and (b) Lateral doping profile (across C-D cutline) of shallow, moderate, and deep N+ source conditions.

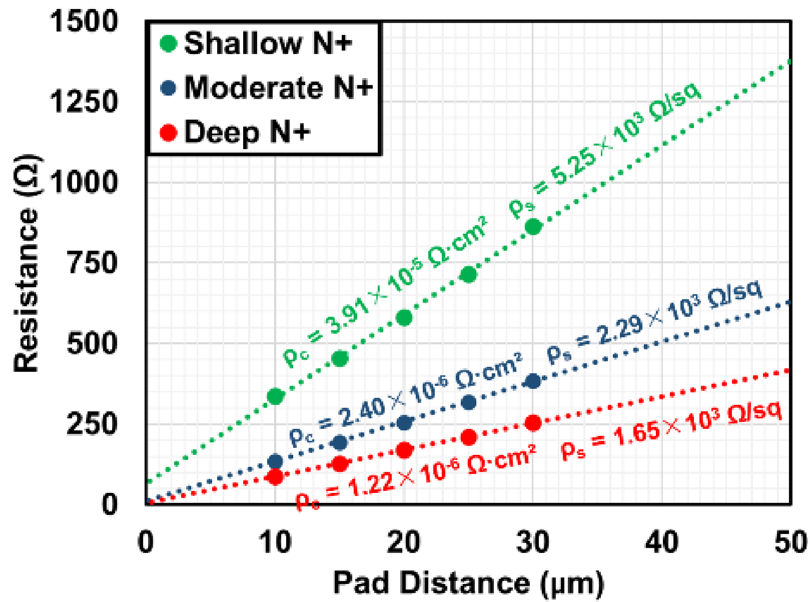

Fig. 4. Resistance versus pad spacing extracted from TLM structures for shallow, moderate, and deep N+ implant splits.

As the implantation energy (or depth) increases, the lateral spread of the doped region becomes more pronounced, resulting in the N+ junction extending further into the channel region. This progressive extension is clearly observed when comparing the shallow, moderate, and deep implant splits. This will be discussed in detail in the next section.

Results and Discussion

TLM measurements were carried out to evaluate the source contact resistivity for each N+ depth condition. Fig. 4 shows the resistance versus pad spacing plots for the shallow, moderate, and deep implant splits. A clear trend is observed, where the extracted contact resistivity decreases significantly with increasing N+ source depth. Specifically, values of 3.91×10^{-5} Ω·cm², 2.40×10^{-6} Ω·cm², and 1.22×10^{-6} Ω·cm² were obtained for the shallow, moderate, and deep splits, respectively. The observed improvement is consistent with the expectation that higher implantation energy increases the cross-sectional area with the depth, creating a more effective current carrying cross-section beneath the contact. This enhancement ultimately contributes to the reduction of the overall device resistance.

Figure 5(a) shows the trade-off relationship between $R_{on,sp}$ and V_{th} for Nominal and HEXFET architectures under different N+ depths. Here, $R_{on,sp}$ was extracted at drain to source current (I_{ds}) = 15 A and gate to source voltage (V_{gs}) = 20 V. For Nominal devices, $R_{on,sp}$ decreased from 3.05 mΩ·cm² (shallow) to 2.96 mΩ·cm² (moderate) and further to 2.89 mΩ·cm² (deep), corresponding to reductions of 3.0% and 5.3% relative to the shallow condition. For HEXFET devices, $R_{on,sp}$ decreases from 2.71 mΩ·cm² (shallow) to 2.63 mΩ·cm² (moderate) and 2.52 mΩ·cm² (deep), representing 3.0% and 7.0% reductions, respectively. The greater improvement in HEXFETs reflects their higher channel density compared to that of the nominal design. These results clearly demonstrate that greater N+ junction depth plays a decisive role in lowering $R_{on,sp}$.

Similarly, a consistent downward trend in threshold voltage is observed with increasing depth. Here, V_{th} was extracted at drain to source current (I_{ds}) = 10 mA while sweeping $V_{gs} = V_{ds}$. For Nominal devices, V_{th} decreases from 2.25 V (shallow) to 2.10 V (moderate) and 1.96 V (deep), representing reductions of 6.7% and 12.9%, respectively. For HEXFET devices, V_{th} shifts from 2.20 V (shallow) to 2.03 V (moderate) and 1.88 V (deep), corresponding to reductions of 7.7% and 14.5%. This behavior is attributed to the extension of the N+ junction toward the channel region with increasing depth, which effectively shortens the channel and reduces the required gate bias to initiate conduction through the channel. The extension of N+ happens due to a phenomenon called lateral straggle. Lateral straggle in ion implantation refers to the sideways spread of implanted ions as they penetrate

into the semiconductor. During implantation, ions undergo multiple collisions with lattice atoms, which causes their trajectories to deviate from the vertical direction. As a result, the dopant distribution extends laterally in addition to its intended vertical depth profile. In this case, the phenomenon causes the N+ source region to extend toward the channel as implant energy increases, as shown in Fig. 3(b). This lateral extension shortens the effective channel length and lowers the effective acceptor concentration near the N+ end of the channel region, which reduces the V_{th}.

Figure 5(b) shows the relationship between breakdown voltage (BV) and threshold voltage (V_{th}) for the N+ depth splits. A clear reduction in BV is observed as the N+ junction depth increases. Here, BV was extracted at I_{ds} = 100 μA and V_{gs} = 0 V. For Nominal devices, BV decreased from 1610 V in the shallow split to 1470 V in the deep split. In HEXFET devices, the degradation is more pronounced, with BV dropping from 1560 V to 1015 V. Here in both the device types, the BV was dictated by the increased leakage current rather than avalanche breakdown. This behavior is strongly correlated with the reduction in V_{th} discussed in the previous section, as both parameters are influenced by the lateral straggle. The underlying mechanism is further illustrated in the simulated channel potential distributions shown in Fig. 6.

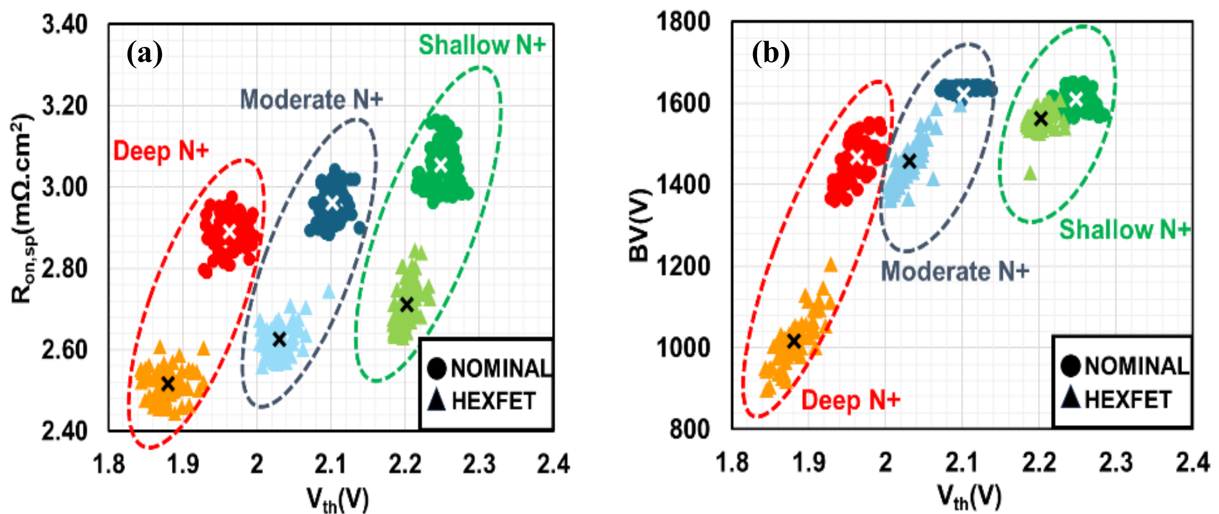

Fig. 5. Trade-off relationship between (a) $R_{on,sp}$ vs. V_{th} (b) BV vs. V_{th} of N+ depth split. The cross marks denote the average value of each population. The $R_{on,sp}$ and BV decrease with N+ depth.

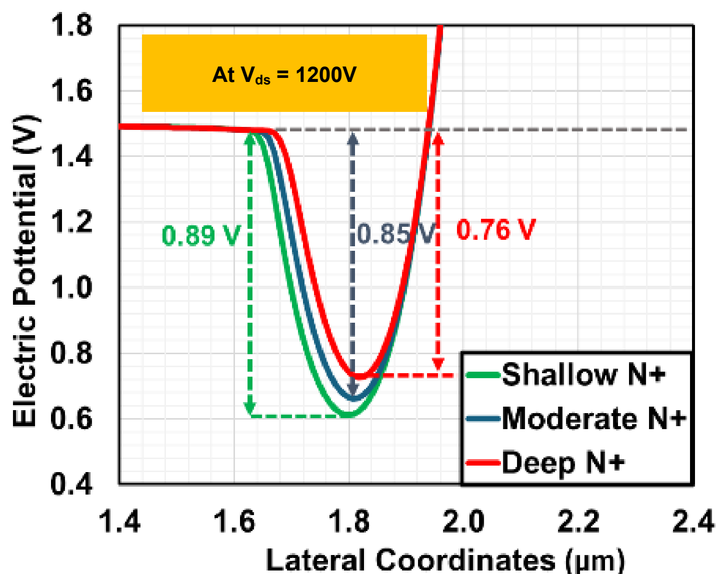

Fig. 6. Channel potential distribution at V_{ds}=1200 V of the N+ Split. The leakage current increases with barrier lowering in the channel region.

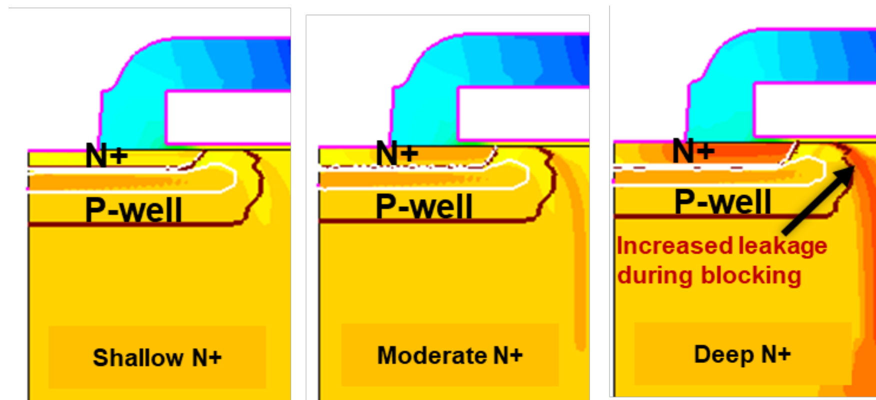

Fig. 7. TCAD simulated leakage current density during blocking mode operation (at V_{ds} = 1200 V).

With deeper implants, the N+ region extends closer to the channel, which reduces the channel potential depth (from 0.89 V to 0.76 V). This lowering of the channel potential barrier promotes increased leakage current in the off state, thereby limiting the BV of the device. The results highlight the inherent trade-off between conduction and blocking characteristics that arise when employing deeper N+ source implants. Fig. 7 shows TCAD simulated leakage current density during the blocking mode operation (at V_{ds} = 1200 V). Increased leakage with deep N+ can be clearly seen here.

To mitigate the high leakage current observed with the deep N+ condition, another wafer was fabricated with same N+ depth however, the JFET region doping was reduced this time. In this case, the shallowest JFET implant dose was reduced by 55% compared to the baseline condition. All other process parameters were identical between initial deep N+ and the new deep N+ with optimized JFET wafers. Figure 8 compares the deep N+ split before and after this adjustment. For Nominal devices, BV improves from 1470 V to 1560 V, while V_{th} increases from 1.96 V to 2.16 V. A slight increase in $R_{on,sp}$ is also observed. Average values of each wafer employed in this study are summarized in table 1.The recovery mechanism is as follows: lowering the JFET doping reduces the net donor concentration including at the surface, thereby increasing the net acceptor concentration in the channel region. This shift raises the local channel potential and restores the channel barrier, which suppresses off-state leakage and supports a higher blocking voltage. Further, co-optimization of both p-well and JFET is required to bring the $R_{on,sp}$ down to the original value or further down while maintaining the same blocking performance.

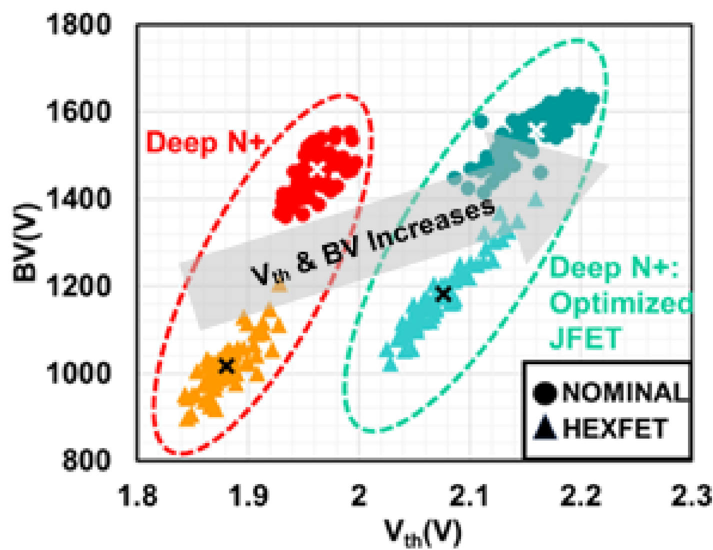

Fig. 8. Deep N+: BV vs. V_{th} comparison with optimized JFET. V_{th} and BV increase with the reduced JFET doping compared to the original deep N+ condition. Cross denotes the average of the population.

Table I. Average electrical characteristics of Nominal MOSFET and HEXFET devices.

	Implant Condition	V_{th} [V]	$R_{on,sp}$ [mΩ·cm²]	BV [V]
		$V_{gs}=V_{ds}$ I_{ds}=10mA	V_{gs}=20V I_{ds}=15A	V_{gs}=0 I_{ds}=100µA
NOMINAL	Shallow N+	2.25	3.05	1610
	Moderate N+	2.10	2.96	1620
	Deep N+	1.96	2.89	1470
	Deep N+: Optimized JFET	2.16	3.02	1560
HEXFET	Shallow N+	2.20	2.71	1560
	Moderate N+	2.03	2.63	1450
	Deep N+	1.88	2.52	1015
	Deep N+: Optimized JFET	2.07	2.65	1180

Conclusion

The impact of N+ source implantation depth on the performance of 1.2 kV 4H-SiC MOSFETs was systematically investigated through a combination of electrical measurements, TCAD simulations, and SEM cross-section validation. TLM structures confirmed that deeper N+ junctions reduce contact resistivity by nearly two orders of magnitude, which directly lowered the source contact contribution to the total device resistance. This reduction translated into measurable improvements in $R_{on,sp}$ with Nominal and HEXFET devices exhibiting decreases of approximately 5% and 7%, respectively, when comparing shallow and deep splits. The improvement is attributed to enhanced current spreading beneath the source electrode and a larger effective conduction cross-section provided by deeper implantation. In parallel, threshold voltage exhibited a reduction with increasing implant depth, decreasing from 2.25 V to 1.96 V in Nominal devices. TCAD profiles reveal that the shift originates from the extension of the N+ junction into the channel region, due to lateral straggle which shortens the effective channel length and reduces the effective acceptor concentration near the channel. BV was strongly influenced by deeper N+, decreasing from 1610 V to 1470 V in Nominal devices and from 1560 V to 1015 V in HEXFETs as the junction depth increased. Channel potential distributions confirmed that the extension of the N+ region lowers the channel barrier, which promotes higher leakage and limits blocking capability. To counteract this degradation, the JFET doping was reduced in deep N+ devices, which increased the effective P-well influence in the channel region and restored the channel barrier. This process modification successfully improved BV from 1470 V to 1560 V in Nominal devices, with only a minor increase in $R_{on,sp}$ and a modest upward shift in Vth. Overall, the results demonstrate that deeper N+ implants are highly effective in reducing contact resistance and $R_{on,sp}$, but they introduce fundamental trade-offs in Vth and BV due to dopant redistribution into the channel region. These findings highlight the importance of co-optimizing N+ source depth with P-well and JFET engineering to balance conduction efficiency with robust blocking capability. Such design strategies are essential for advancing 1.2 kV 4H-SiC MOSFET technology toward higher performance and reliability in next generation power electronic systems.

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