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# Demonstration of ALD $SiO_2$ as Gate Oxide in the 1.7kV SiC UMOSFET for High-Power and Embedded CMOS Circuit Integration

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**Keywords:** 4H-SiC, Atomic Layer Deposition, Density of interface states, Embedded CMOS, $SiO_2$, Specific on-state resistance, Trench UMOSFET

**Abstract.** This paper presents process integration of atomic layer deposition (ALD) $SiO_2$ as gate dielectric in the 1.7 kV SiC trench UMOSFET. This integration provides a solution for embedding complementary metal oxide semiconductor (CMOS) circuits into the UMOSFET power device, enabling the realization of smart power management integrated circuit (IC) functions in the future. 4H-SiC power MOSFETs have gained increased attention in medium to high power applications recently due to their wide bandgap, high breakdown electric field, and excellent thermal conductivity. The electric vehicle (EV) is one example of an application where the Tesla Model 3 utilizes SiC 650V VDMOSFETs as driving components in its inverter design. Trench MOSFETs are key to achieving these requirements to further scale down power devices while decreasing the specific on-state resistance ($R_{on,sp}$). This is challenging with thermal gate oxide on SiC trench MOSFETs due to the anisotropic thermal oxide growth rate on the sidewalls and the bottom of trench or mesa region. Therefore, we propose a novel fabrication process by integrating ALD $SiO_2$ gate oxide into trench UMOSFET. The $R_{on,sp}$ of the fabricated device can be reduced to 2.3mΩ-cm$^2$, accompanied by a very low density of interface states ($D_{it}$) of approximately $5.36 \times 10^{10}$ eV$^{-1}$cm$^{-2}$. Another feature of this ALD $SiO_2$ solution for gate oxide is the monolithic integration of the CMOS circuit with the UMOSFET, enabling the realization of smart power IC management.

## Introduction

SiC power MOSFETs are replacing Si devices in the blocking voltage range from 600 to 6500 V with substantial energy saving in various electric systems courtesy to their low on-resistance and fast switching. This trend is now often supported by trench UMOSFET. In particular significant attention has been paid to monolithic SiC power IC [1] due to its fast-switching capabilities and suitability for harsh environment applications. However, a major challenge remains in achieving a conformal gate oxide thickness on both the UMOSFET and CMOSFET. The strong crystal face dependence of the oxidation rate [2] must be carefully considered in device fabrication. The industry trend has shifted from thermal oxidation to deposition techniques, with ALD offering best quality, superior conformality and precise control of thickness at low temperatures, while also enabling interface engineering using plasma-based processes.

## Nobel Fabrication Process for Embedded CMOS and UMOSFET

In this paper, we propose a novel fabrication process for embedding the low voltage (LV) CMOS circuit and high voltage (HV) trench UMOSFET simultaneously on a SiC substrate as presented in Figure 1. Began with the RCA clean process with a nitrogen-doped ($5 \times 10^{15}$ cm$^{-3}$), 4-degree tilted epitaxial layer (15 μm) grown on a heavily doped SiC substrate. A multiple ion implantation process

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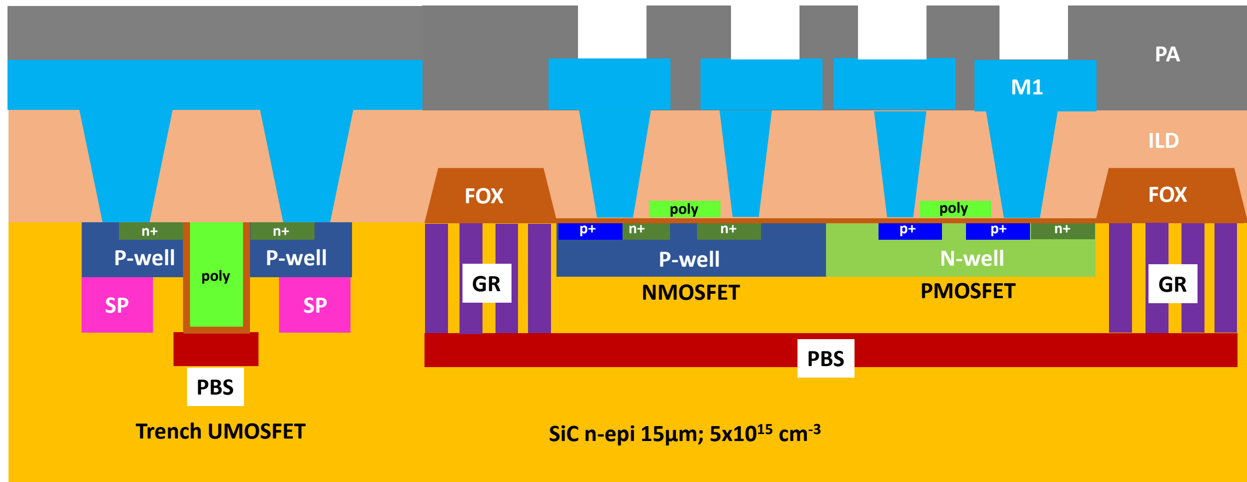


**Fig. 1.** Cross-sectional scheme for LV and HV device integration

was executed in a high-temperature (500°C) implanter, including the p-bottom shielding (PBS), p-plus ($p^+$), guard ring (GR), n-plus ($n^+$), p-well (PW), and side-wall protection (SP) implantations. Among the implantation steps, the PBS and SP processes further utilized the spacer on hard mask sidewall (SHMS) technique to precisely control the lateral doping profile, ensuring a balance between $R_{on,sp}$ and breakdown voltage (BV). An implantation hard mask was patterned for the PBS and SP layers, a side wall spacer was then formed on the lateral side wall of the hard mask. High energy ion implantation was executed to the desired junction depth to form the bottom and side wall protection structures for the PBS and SP, respectively. The implanted dopants were activated by 1750ºC thermal annealing with carbon cap. Trench formation was achieved by first patterning a hard mask on SiC, followed by reactive ion etching (RIE) to create the desired depth and profile, resulting in trenches with a width of 1µm and a depth of 1.5µm. The sacrificial oxidation followed by the deep trench etching was conducted to repair the side wall damage region induced by the trench etching. A raised CVD field oxide layer of 0.2 µm was subsequently patterned to create the isolation region within the CMOS circuit area. Gate dielectrics were formed under three different conditions for comparison: LPCVD $SiO_2$ deposition followed by nitrogen ($N_2$) annealing at 1000°C, ALD $SiO_2$ deposition with TDMAS and $O_3$ as precursors followed by nitric oxide (NO) annealing at 1250°C, and dry thermal oxidation followed by NO annealing at 1250°C. The ALD $SiO_2$ dielectric stack includes in-situ plasma preclean and a 5 nm interfacial layer deposited by advanced PEALD Atomic Layer Annealing (ALA) [3] prior a thick high-quality $SiO_2$ thermal ALD layer thus tailoring the SiC/dielectric interface, enhancing leakage current, breakdown voltage, and overall quality of the SiC/$SiO_2$ interface.

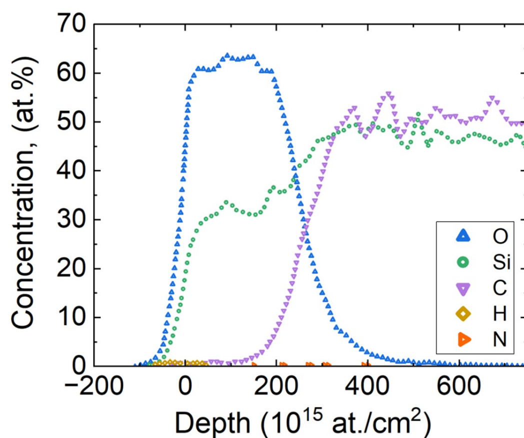


**Fig. 2.** TOF-ERDA composition analysis of the ALD $SiO_2$ stack [33.7+/-0.5 % Si, 66.2 +/-0.5 % O, < 1% C, H <0.3%, N < BDL]

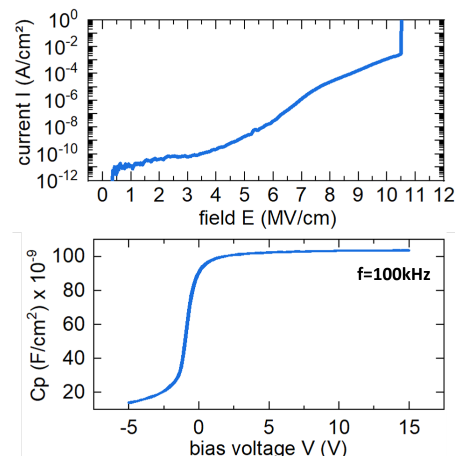


**Fig. 3.** Current density-electric field and Capacitance-voltage Plot

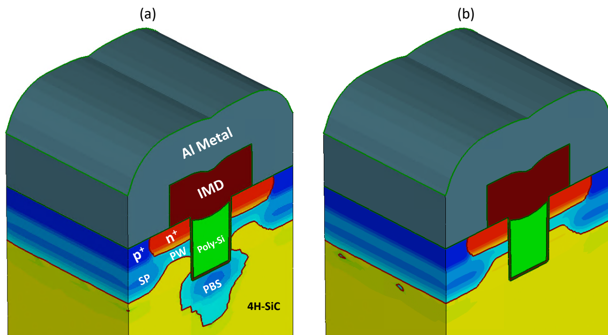


Fig. 4. (a) Simulated trench UMOSFET with PBS implantation and (b) without PBS implantation

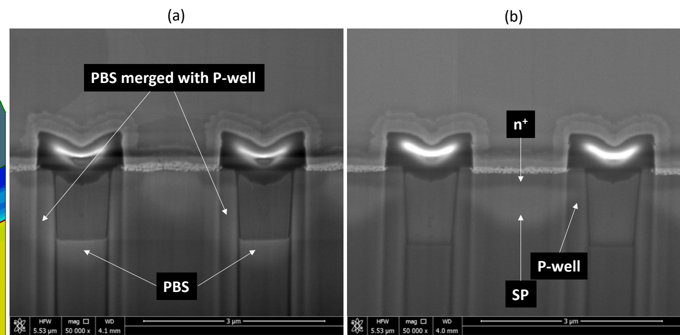


Fig. 5. SEM cross section of trench UMOSFET with (a) PBS implantation (b) without PBS implantation

High purity of the ALD $SiO_2$ dielectric stack was confirmed after NO annealing on Figure 2. Current density-electric field and Capacitance–voltage characteristics of MOS test capacitors using the ALD $SiO_2$ dielectric stack are shown on Figure 3. These characteristics are accompanied by a nearly ideal VFB of - 0.69V, a 0.1V hysteresis and - $6.6 \times 10^{10}$ $cm^{-2}$ charge trapping at the $SiO_2$/SiC interface. Heavily phosphorus-doped polysilicon with a thickness of 1 μm was formed using the deposition-etching-deposition (DED) technique to ensure effective gap filling and conductivity in both the trench UMOSFET and CMOS devices. An inter-metal dielectric (IMD) layer was deposited and subsequently patterned to define the source and gate contact regions, facilitating device interconnections. Nickel silicide (NiSi) and titanium/titanium nitride (Ti/TiN) was employed for the metal contact in the source and gate contact region, respectively. Pure aluminum (Al) was deposited and subsequently patterned to establish top metal region. Finally, a passivation layer consisting of 0.2 μm of oxide and 0.7 μm of nitride was deposited using PECVD tool. Additionally, a 10 μm polyimide layer was applied to protect the entire chip area, except for the opening region on the electrical pad for probing the power device. This completes the fabrication of the SiC trench UMOSFETs and CMOS circuits on the wafer. The simulated and fabricated UMOSFET are shown in Figures 4 and 5, respectively.

## Experimental Results and Discussion

Figure 6 presents the SEM cross-sectional image of trench UMOSFETs utilizing LPCVD $SiO_2$, ALD $SiO_2$, and thermal $SiO_2$ as gate dielectrics. The gate oxide thickness on the trench sidewall is thinnest for LPCVD $SiO_2$, attributed to its poor step coverage. In contrast, the thickness at the trench

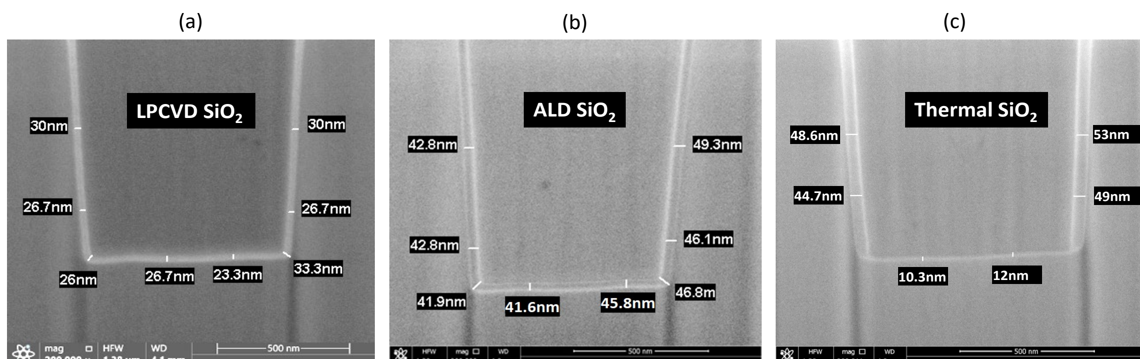


Fig. 6. SEM cross section of trench UMOSFET with (a) LPCVD $SiO_2$ (b) ALD $SiO_2$ (c) Thermal $SiO_2$

**Table 1.** Gate Oxide Thickness Comparison

| **Gate Oxide Condition** | LPCVD $SiO_2$ | ALD $SiO_2$ | Thermal $SiO_2$ |
|---|---|---|---|
| **Post Oxide Annealing** | $N_2$ 1000ºC | NO 1250ºC | NO 1250ºC |
| **Oxide Thickness@ Trench Side Wall** | 28.35 nm [SEM] | 45.3 nm [SEM] | 48.8 nm [SEM] |
| **Oxide Thickness@ Trench Bottom** | 25 nm [SEM] | 43.7 nm [SEM] | 11.1 nm [SEM] |
| **Oxide Thickness@ Trench Mesa** | 48 nm [CV] | 41 nm [CV] | 15 nm [CV] |
| **Mesa Normalized to Side Wall** | 169 % | 91 % | 31 % |

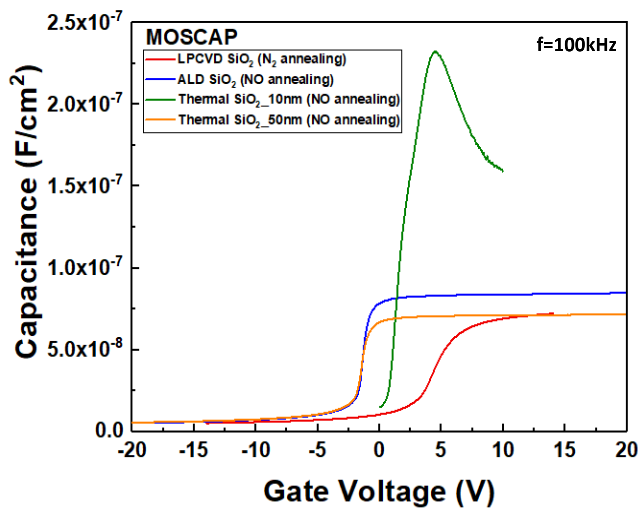


**Fig. 7.** CV characteristics of MOSCAP with different gate oxide and annealing

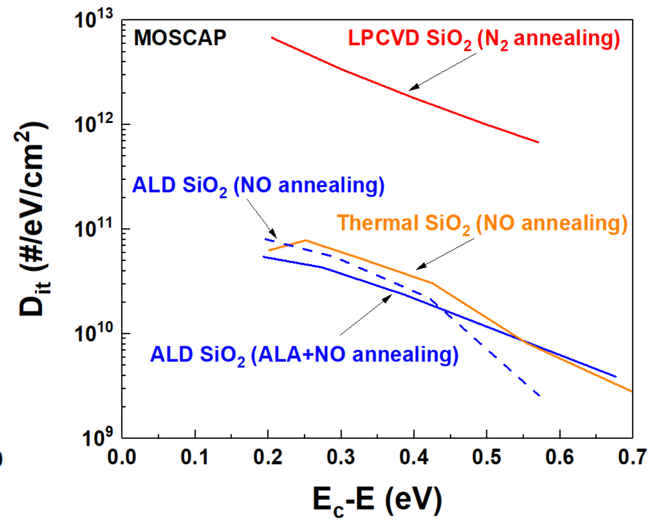


**Fig. 8.** Density of interface states versus energy distribution with different gate oxide and annealing

bottom reveals that thermal $SiO_2$ exhibits only 10 nm compared to the other two deposition methods due to the lower anisotropic thermal oxidation rate at the trench bottom. Table 1 summarizes the gate oxide thickness across three different regions surrounding the trench for the three gate oxide formation methods. ALD $SiO_2$ demonstrates the best step coverage and conformality among the options, indicating a high potential for integrating CMOS circuits into trench UMOSFET power chips. Figure 7 illustrates the CV characteristics of the planar MOS capacitor built on the mesa region under various gate oxide and annealing conditions. The ALD $SiO_2$ exhibits behavior similar to that of the thicker thermal $SiO_2$. In contrast, the LPCVD $SiO_2$ reveals a larger flat band shift and distortion, attributed to accumulated $D_{it}$ at the interface. Additionally, the thinner thermal $SiO_2$ raises significant concerns regarding leakage and reliability issues. The Hi-Lo CV method was conducted to extract the $D_{it}$ in this work. The $D_{it}$ at 0.2 eV from the conduction band edge is measured to be $5.36\text{x}10^{10}$ $eV^{-1}\cdot cm^{-2}$ for ALD $SiO_2$, $6.30\text{x}10^{10}$ $eV^{-1}\cdot cm^{-2}$ for thermal $SiO_2$, and $6.80\text{x}10^{12}$ $eV^{-1}\cdot cm^{-2}$ for LPCVD $SiO_2$, as shown in Figure 8. As expected in-situ plasma preclean and deposition of the ALA $SiO_2$ interfacial layer strongly improved $D_{it}$ of the Si-face on SiC. Figure 9 presents the transfer characteristics of the planar NMOSFET and PMOSFET utilizing ALD $SiO_2$ as the gate oxide. The extracted threshold voltages ($V_{th}$) are found to be 2 V for the NMOSFET and 5.3 V for the PMOSFET. The subthreshold swing (S.S) are 203 and 287 mV/Dec for the NMOSFET and PMOSFET, respectively. The output characteristics of the NMOSFET and PMOSFET exhibit typical linear and saturation behavior as demonstrated in Figure 10. To demonstrate the integration of the CMOS

circuits with power trench UMOSFET by utilizing the ALD $SiO_2$ as the gate dielectric, we also fabricate an inverter circuit composed of both NMOSFET and PMOSFET in this work. Figure 11 presents the transfer characteristics of the fabricated inverter circuit, showing a high noise margin (NMH) of 6.3 V and a low noise margin (NML) of 10.5 V. The observed asymmetry between NMH and NML is attributed to the $V_{th}$ mismatch between the NMOSFET and PMOSFET, as previously discussed. The PBS implantation was introduced to the thermal $SiO_2$ wafer to provide protection for the ultra-thin oxide at the trench bottom and corners. Figure 12 illustrates the transfer characteristics of the trench UMOSFET, with the $V_{th}$ determined at a gate voltage (VG) corresponding to a current

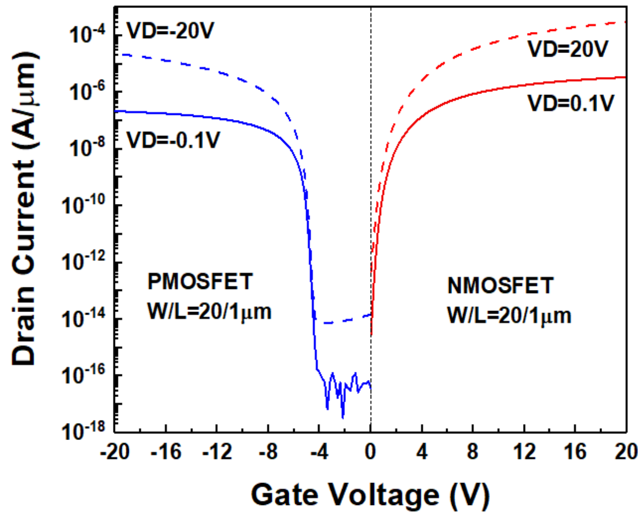


Fig. 9. Transfer characteristics of NMOSFET and PMOSFET with ALD $SiO_2$ as gate dielectric

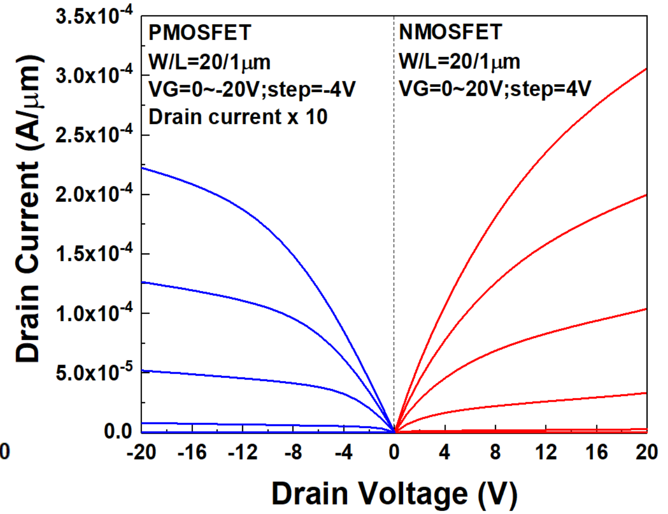


Fig. 10. Output characteristics of NMOSFET and PMOSFET with ALD $SiO_2$ as gate dielectric

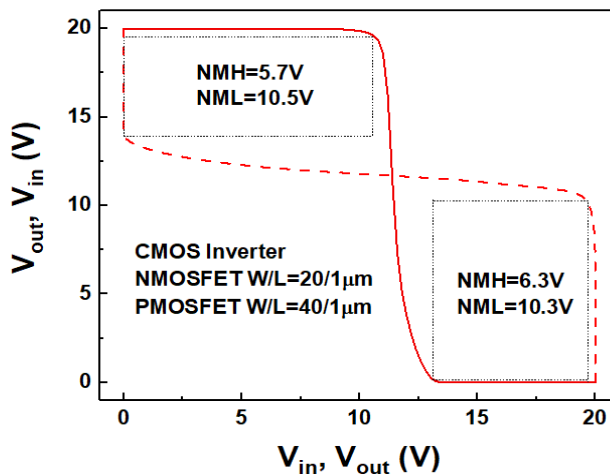


Fig. 11. Transfer characteristics of CMOS inverter with ALD $SiO_2$ as gate dielectric

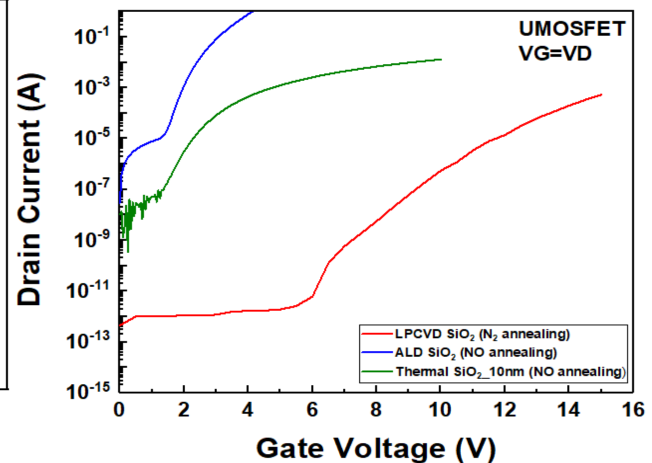


Fig. 12. Transfer characteristics of UMOSFET with different gate oxide and annealing

of 1 mA. The $V_{th}$ values are found to be 2 V for ALD $SiO_2$ and 4.8 V for thermal $SiO_2$. In contrast, the LPCVD $SiO_2$ exhibits an abnormally high $V_{th}$, attributed to the elevated $D_{it}$ accumulated at the $SiO_2$/SiC interface. In addition to the varying effects of the gate oxide, the higher $V_{th}$ observed in the trench UMOSFET with thermal $SiO_2$ is also influenced by the PBS implantation effect. The merged PBS implant profile with the p-well on the left side wall of the trench, resulting from an alignment error as depicted in Figure 5(a), contributes to the higher $V_{th}$ and the lower conduction observed current. Figure 13 shows the output characteristics of the trench UMOSFET with ALD $SiO_2$ as the gate dielectric. Finally, the benchmark comparison of our work with other studies [4~6] is presented in Figure 14, highlighting a $R_{on,sp}$ of 2.3~2.7 mΩ·cm² and a BV of 1755~2349V achieved in this study. Figure 15 presents the BV characteristics of the fabricated UMOSFET and floating GR. The

wider BV range was attributed to the leakage current originating in the UMOSFET cell region, which likely stemmed from the corner and bottom of the trench structure being inadequately protected by the SP and PBS.

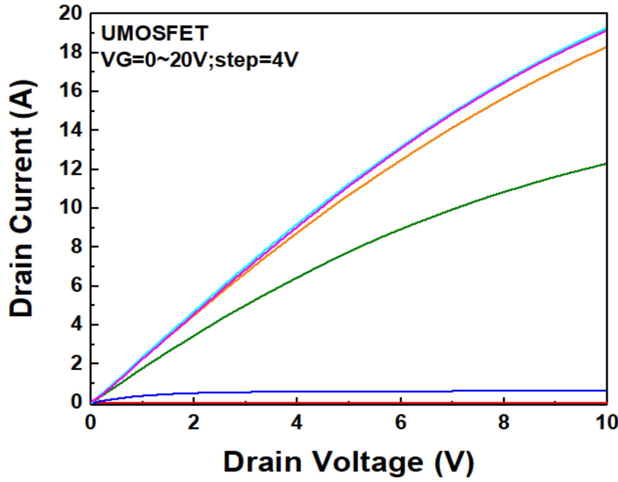


**Fig. 13.** Output characteristics of UMOSFET with ALD $SiO_2$ as gate dielectric

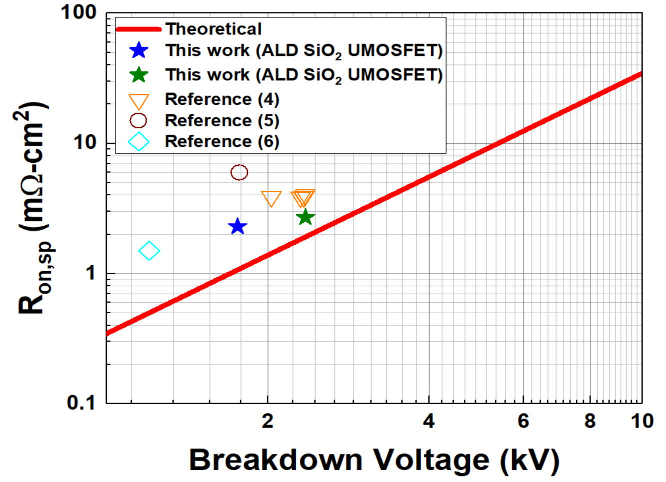


**Fig. 14.** Benchmark comparison of other studies with this work

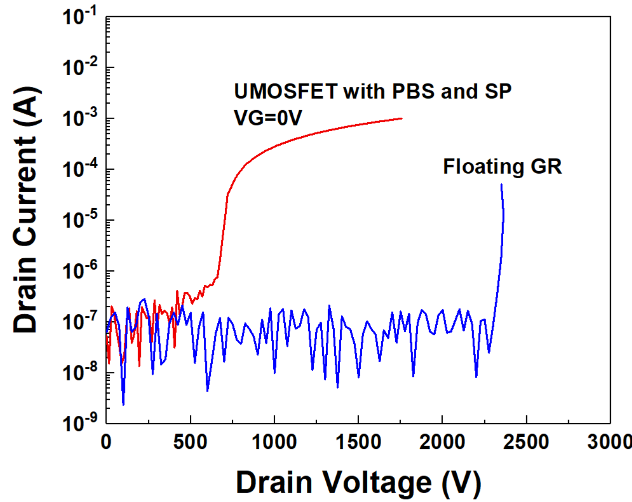


**Fig. 15.** BV characteristics of the fabricated UMOSFET and GR in this work

**Summary**

We have successfully demonstrated the monolithic integration of CMOS circuits with power trench UMOSFETs by utilizing ALD $SiO_2$ as the gate dielectric, owing to its superior step coverage and conformality. In-situ plasma preclean of the SiC surface and deposition of a 5 nm ALA $SiO_2$ interfacial layer strongly improve $D_{it}$. The $D_{it}$ of the ALD $SiO_2$ can reach $5.36\times10^{10}$ $eV^{-1}\cdot cm^{-2}$, which is comparable to or even better than that of thermal $SiO_2$ observed so far. The NMH and NML of the fabricated inverter circuit are 6.3V and 10.5V, respectively. The asymmetry between NMH and NML can be further improved through $V_{th}$ adjustment or optimization of the channel width design in future work. The $V_{th}$ of the ALD $SiO_2$ trench gate oxide UMOSFET is 2 V, and the $R_{on,sp}$ can be reduced to 2.3 $m\Omega\cdot cm^2$ due to the ultra-lower $D_{it}$ at the $SiO_2$/SiC interface. The BV of the fabricated ALD $SiO_2$ trench MOSFET and the guard ring is within 1755~2349 V, which is good enough for the 1700 V application. The enabling capability of ALD for the monolithic integration versus thermal oxide and LPCVD, which are just not capable due to conformality across the mesa and trench regions. Future work will require the optimization of the ALD $SiO_2$ process, as well as the SP and PBS implantation processes.

**Acknowledgement**

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